

POWER8 Memory Buffer Registers Specification

Advance

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Version 1.0



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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release.

Version	Revision Date	Description
1.0	07/31/14	Initial Release.

About this Document

This document describes the POWER8 registers used by both the IBM® POWER8™ Memory Buffer. These registers are referred to as "POWER8" registers. Throughout this document, the term “processor” refers to the POWER8 Processor and “memory buffer” refers to the POWER8 Memory Buffer.

To ensure you have the most current version of this document, contact your IBM technical representative or visit the OpenPOWER Connect website.

Who Should Read this Document

This manual is intended for system software and hardware developers and application programmers who want to develop products for the POWER8 memory buffer. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of reduced instruction set computer (RISC) processing, and details of the Power ISA.

Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are usually preceded by “0x,” or displayed inside single quotation marks and followed by an “x.”
  For example: 0x000000000204000D, or '000000000204000D'x.

- Binary values in sentences are usually preceded by “0b,” or displayed inside single quotation marks and followed by a “b.”

  For example: 0b1, or '1'b.

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “X” or "x."

Bit Significance

In the POWER8 documentation, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

Organization

The table of contents provides a list register names. An address map lists the registers in alphabetical order by mnemonic (see Chapter 1 on page 160). The registers themselves are arranged by their addresses. A register can have multiple addresses with a different addresses for different units. The types of access permitted can vary by unit.

Terminolgy

For definitions of the acronyms and abbreviations used in this document, see Section 8 *Glossary*.

Related Documents

The following documents can be helpful when reading this specification. They are available through OpenPOWER Connect or Power.org.

POWER8 Processor User's Manual for the Single-Chip Module
POWER8 Processor Single-Chip Module Datasheet
POWER8 Processor Registers Specification
POWER8 Memory Buffer Datasheet
POWER8 Memory Buffer User's Manual
POWER8 Memory Buffer Registers Specification
Power ISA User Instruction Set Architecture - Book I (Version 2.07)
Power ISA Virtual Environment Architecture - Book II (Version 2.07)
Power ISA Operating Environment Architecture (Server Environment) - Book III-S (Version 2.07)

1. PIB, PSV

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
DMI.DMIPLL.CWRAP.PLL_CNTRL0	0x0000000000000010	179
DMI.DMIPLL.CWRAP.PLL_CNTRL1	0x0000000000000011	180
DMI.DMIPLL.CWRAP.PLL_CNTRL2	0x0000000000000012	180
DMI.DMIPLL.CWRAP.PLL_CNTRL_SETUP0	0x0000000000000013	180
DMI.DMIPLL.CWRAP.PLL_CNTRL_SETUP1	0x0000000000000014	181
DMI.DMIPLL.CWRAP.PLL_CNTRL_SETUP2	0x0000000000000015	182
MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_0	0x00000000000FFFA0	386
MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_1	0x00000000000FFFA1	386
MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_2	0x00000000000FFFA2	386
MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_3	0x00000000000FFFA3	387
PLLMEM.PLL_CNTRL0	0x0000000000000000	176
PLLMEM.PLL_CNTRL1	0x0000000000000001	176
PLLMEM.PLL_CNTRL2	0x0000000000000002	177
PLLMEM.PLL_CNTRL_SETUP0	0x0000000000000003	177
PLLMEM.PLL_CNTRL_SETUP1	0x0000000000000004	178
PLLMEM.PLL_CNTRL_SETUP2	0x0000000000000005	179
SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_0	0x00000000000FFFB0	387
SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_1	0x00000000000FFFB1	387
SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_2	0x00000000000FFFB2	388
SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_3	0x00000000000FFFB3	388
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART0_REGISTER	0x0000000000010000	203
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART10_REGISTER	0x000000000001000A	205
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART11_REGISTER	0x000000000001000B	206
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART12_REGISTER	0x000000000001000C	206
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART13_REGISTER	0x000000000001000D	206
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART14_REGISTER	0x000000000001000E	206
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART15_REGISTER	0x000000000001000F	207
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TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART17_REGISTER	0x0000000000010011	207
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART18_REGISTER	0x0000000000010012	207
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TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART1_REGISTER	0x0000000000010001	203
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART20_REGISTER	0x0000000000010014	208
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART21_REGISTER	0x0000000000010015	208
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART22_REGISTER	0x0000000000010016	208
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART23_REGISTER	0x0000000000010017	209
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART24_REGISTER	0x0000000000010018	209
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART25_REGISTER	0x0000000000010019	209
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART26_REGISTER	0x000000000001001A	209
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART27_REGISTER	0x000000000001001B	210
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART28_REGISTER	0x000000000001001C	210
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART29_REGISTER	0x000000000001001D	210
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART2_REGISTER	0x0000000000010002	203
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART30_REGISTER	0x000000000001001E	210
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TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART34_REGISTER	0x0000000000010022	211
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART35_REGISTER	0x0000000000010023	212
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART36_REGISTER	0x0000000000010024	212
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART37_REGISTER	0x0000000000010025	212
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART38_REGISTER	0x0000000000010026	212
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART39_REGISTER	0x0000000000010027	213
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART3_REGISTER	0x0000000000010003	204
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART40_REGISTER	0x0000000000010028	213
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART41_REGISTER	0x0000000000010029	213
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART42_REGISTER	0x000000000001002A	213
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART43_REGISTER	0x000000000001002B	214
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TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART45_REGISTER	0x000000000001002D	214
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TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART47_REGISTER	0x000000000001002F	215
TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART48_REGISTER	0x0000000000010030	215
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TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART22_REGISTER	0x0000000000010056	224
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The memory buffer registers are listed in the following tables.

Register Name	***PLL Control Register***
Mnemonic	PLLMEM.PLL_CNTRL0
Address	0000000000000000 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RO	BYPMODE: Bypass Mode Selector
3	RO	BYPASS: Enable PLL Bypass, only effective if no reset and no enables are set (that is in case of a disable, HW141963) Values: OFF=>0b1 ON=>0b0
4:5	RO	CHARMODE: Testout Divide Selector
6:8	RO	CP_TUNE: Charge Pump Tune Bits
9:11	RO	DUTY_ADJ: Adjust Duty Cycle
12	RO	FBKMODE: Used by Digital Pll
13:14	RO	IREF_TUNE: IREF Process/Temperature Tune Bits
15:34	RO	JIT_CNTL: Jitter Macro Controller
35:45	RO	LOCK_TUNE: Lock Tune Bits
46:54	RO	MULT: Multiplication Factor
55:56	RO	OUTSEL: Select Between PLLOUTA and B for TESTOUT
57:58	RO	PHASEDET_TUNE: Phase Detector Tune Bits
59	RO	FBKSEL: Select between external and internal feedback clock
60:63	RO	RANGEA: Range Selector for PLLOUTA

Register Name	***PLL Control Register***
Mnemonic	PLLMEM.PLL_CNTRL1
Address	0000000000000001 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:3	RO	RANGEB: Range Selector for PLLOUTB
4	RO	REFDIV: Ref divider select
5:6	RO	A2D_TUNE_0_TO_1: Tune bits 0 to 1 for A to D converter
7:11	RO	A2D_TUNE_2_TO_6: Tune bits 2 to 6 for A to D converter
12:17	RO	ANALOGOUT_TUNE: Tune bits for Analog out ckt
18:19	RO	VREG_TUNE: Selector for Vreg
20	RO	CTST_TUNE: Cap leakage tune bit
21	RO	LOCK_SEL: Selects which lock detector is used

Bits	PLLREG	Field Mnemonic: Description
22	RO	TST_MODE_EN: For test use only
23	RO	TSTMODE_NCAP_LT: For test use only
24	RO	TSTMODE_IREF_LT: For test use only
25	RO	TSTMODE_DT_LT: For test use only
26	RO	TSTMODE_AOUT_LT: For test use only
27	RO	TSTMODE_VCOCMP_LT: For test use only
28	RO	TSTMODE_CTST_LT: For test use only
29	RO	TSTMODE_VCO_SEL: For test use only
30	RO	CPHASE: Sel for duty mux in out_driver
31	RO	E_MODE_ENABLE: Digital PLL and Digital Testout modes
32:62	RO	TUNE: Tune bits
63	RO	OUTA_DISABLE: Disable for output a

Register Name	***PLL Control Register***
Mnemonic	PLLMEM.PLL_CNTRL2
Address	0000000000000002 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	OUTB_DISABLE: Disable for output b
1:2	RO	VCODIV: VCO divider
3	RO	DIGTESTOUT: Digital test out of PLL (for test purpose)
4	RO	RESET: reset bit is not used in Analog PLL, only Filt and Tank
5:7	RO	SPARE: Not used

Register Name	***PLL Control Register NSL***
Mnemonic	PLLMEM.PLL_CNTRL_SETUP0
Address	0000000000000003 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	WO	SHADOW_BYPMODE: Bypass Mode Selector
3	WO	SHADOW_BYPASS: Enable PLL Bypass, only effective if no reset and no enables are set (that is, in case of a disable, HW141963) Values: OFF=>0b1 ON=>0b0
4:5	WO	SHADOW_CHARMODE: Testout Divide Selector
6:8	WO	SHADOW_CP_TUNE: Charge Pump Tune Bits
9:11	WO	SHADOW_DUTY_ADJ: Adjust Duty Cycle

Bits	PLLREG	Field Mnemonic: Description
12	WO	SHADOW_FBKMODE: Used by Digital Pll
13:14	WO	SHADOW_IREF_TUNE: IREF Process/Temperature Tune Bits
15:34	WO	SHADOW_JIT_CNTL: Jitter Macro Controller
35:45	WO	SHADOW_LOCK_TUNE: Lock Tune Bits
46:54	WO	SHADOW_MULT: Multiplication Factor
55:56	WO	SHADOW_OUTSEL: Select Between PLLOUTA and B for TESTOUT
57:58	WO	SHADOW_PHASEDET_TUNE: Phase Detector Tune Bits
59	WO	SHADOW_FBKSEL: Select between external and internal feedback clock
60:63	WO	SHADOW_RANGEA: Range Selector for PLLOUTA

Register Name	***PLL Control Register NSL***
Mnemonic	PLLMEM.PLL_CNTRL_SETUP1
Address	0000000000000004 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:3	WO	SHADOW_RANGEB: Range Selector for PLLOUTB
4	WO	SHADOW_REFDIV: Ref divider select
5:6	WO	SHADOW_A2D_TUNE_0_TO_1: Tune bits 0 to 1 for A to D converter
7:11	WO	SHADOW_A2D_TUNE_2_TO_6: Tune bits 2 to 6 for A to D converter
12:17	WO	SHADOW_ANALOGOUT_TUNE: Tune bits for Analog out ckt
18:19	WO	SHADOW_VREG_TUNE: Selector for Vreg
20	WO	SHADOW_CTST_TUNE: Cap leakage tune bit
21	WO	SHADOW_LOCK_SEL: Selects which lock detector is used
22	WO	SHADOW_TST_MODE_EN: For test use only
23	WO	SHADOW_TSTMODE_NCAP_LT: For test use only
24	WO	SHADOW_TSTMODE_IREF_LT: For test use only
25	WO	SHADOW_TSTMODE_DT_LT: For test use only
26	WO	SHADOW_TSTMODE_AOUT_LT: For test use only
27	WO	SHADOW_TSTMODE_VCOCMP_LT: For test use only
28	WO	SHADOW_TSTMODE_CTST_LT: For test use only
29	WO	SHADOW_TSTMODE_VCO_SEL: For test use only
30	WO	SHADOW_CPHASE: Sel for duty mux in out_driver
31	WO	SHADOW_E_MODE_ENABLE: Digital PLL and Digital Testout modes
32:62	WO	SHADOW_TUNE: Tune bits
63	WO	SHADOW_OUTA_DISABLE: Disable for output a

Register Name	***PLL Control Register NSL***
Mnemonic	PLLMEM.PLL_CNTRL_SETUP2
Address	0000000000000005 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	WO	SHADOW_OUTB_DISABLE: Disable for output b
1:2	WO	SHADOW_VCODIV: VCO divider
3	WO	SHADOW_DIGTESTOUT: Digital testout
4	WO	SHADOW_RESET: reset - bit not used in Analog PLL, only Tank and Filt
5:7	WO	SHADOW_SPARE: Not used - spare

Register Name	***PLL Control Register***
Mnemonic	DMI.DMIPLL.CWRAP.PLL_CNTRL0
Address	0000000000000010 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	
3	RW	BYPASS: Enable PLL Bypass, only effective if no reset and no enables are set (that is, in case of a disable, HW141963) Values: OFF=>0b1 ON=>0b0
4:8	RW	SPEDIV: Testout Divide Selector
9:11	RW	CPISEL:
12:20	RW	DIVSELB:
21:23	RW	PCLKSEL:
24:27	RO	BANDSEL:
28:38	RW	ANALOGTUNE:
39:42	RW	ATSTSEL:
43	RW	VCOSEL:
44:47	RW	BGOFFSET:
48:51	RW	CCALBANDSEL:
52:54	RW	UNUSED1:
55	RW	CCALFMAX:
56	RW	CCALFMIN:
57	RW	CCALLOAD:
58	RW	CCALCVHOLD:
59	RW	DCTEST_DC: control signal that does not get changed in mission mode or during lbist except for during specific tester-only periods
60	RW	CCALMETH:

Bits	PLLREG	Field Mnemonic: Description
61	RW	UNUSED4: controls vregbypass
62	RW	CMLEN:
63	RW	UNUSED5:

Register Name	*PLL Control Register*
Mnemonic	DMI.DMIPLL.CWRAP.PLL_CNTRL1
Address	0000000000000011 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	CALREQ:
1	RW	CALRECAL:
2:5	RW	RDIV: refclk divider
6:7	RW	UNUSED2:
8	RO	CCALCOMP:
9	RO	CCALERR:
10:11	RW	SEL:
12	RW	EN:
13:15	RW	VSEL:
16:62	RO	Reserved field. (Access type is unused)
63	RW	PLLOUTA_DISABLE:

Register Name	*PLL Control Register*
Mnemonic	DMI.DMIPLL.CWRAP.PLL_CNTRL2
Address	0000000000000012 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	UNUSED_OUTB_DISABLE: Unused: Disable for output b
1:3	RO	UNUSED: unused
4	RW	RESET: reset for Tank and Filt PLL
5:7	RO	SPARE: Not used - spare

Register Name	*PLL Control Register NSL*
Mnemonic	DMI.DMIPLL.CWRAP.PLL_CNTRL_SETUP0
Address	0000000000000013 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	
3	RW	SHADOW_BYPASS: Enable PLL Bypass, only effective if no reset and no enables are set (that is, in case of a disable, HW141963) Values: OFF=>0b1 ON=>0b0
4:8	RW	SHADOW_SPEDIV: Testout Divide Selector
9:11	RW	SHADOW_CPISEL:
12:20	RW	SHADOW_DIVSELB:
21:23	RW	SHADOW_PCLKSEL:
24:27	RO	SHADOW_BANDSEL:
28:38	RW	SHADOW_ANALOGTUNE:
39:42	RW	SHADOW_ATSTSEL:
43	RW	SHADOW_VCOSEL:
44:47	RW	SHADOW_BGOFFSET:
48:51	RW	SHADOW_CCALBANDSEL:
52:54	RW	SHADOW_UNUSED1:
55	RW	SHADOW_CCALFMAX:
56	RW	SHADOW_CCALFMIN:
57	RW	SHADOW_CCALLOAD:
58	RW	SHADOW_CCALCVHOLD:
59	RW	Reserved field. (Access type is SHADOW_unused)
60	RW	SHADOW_CCALMETH:
61	RW	SHADOW_UNUSED4: controls vregbypass
62	RW	SHADOW_CMLEN:
63	RW	SHADOW_UNUSED5:

Register Name	***PLL Control Register NSL***
Mnemonic	DMI.DMIPLL.CWRAP.PLL_CNTRL_SETUP1
Address	0000000000000014 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	SHADOW_CALREQ:
1	RW	SHADOW_CALRECAL:
2:5	RW	SHADOW_RDIV:
6:7	RW	SHADOW_UNUSED2:
8	RO	SHADOW_CCALCOMP:
9	RO	SHADOW_CCALERR:
10:62	RO	Reserved field. (Access type is SHADOW_unused)
63	RW	SHADOW_PLLOUTA_DISABLE:

Register Name	***PLL Control Register NSL***
Mnemonic	DMI.DMIPLL.CWRAP.PLL_CNTRL_SETUP2
Address	0000000000000015 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	SHADOW_UNUSED_OUTB_DISABLE: Unused: Disable for output b
1:3	RO	SHADOW_UNUSED: unused
4	RW	SHADOW_RESET: reset for Tank and Filt PLL
5:7	RO	SHADOW_SPARE: Not used - spare

Register Name	***Contains Command To The Shift Engine***
Mnemonic	VI.FSI.FSI_SHIFT.COMMAND_REGISTER
Address	0000000000000C01 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	CMD_REG: command register

Register Name	***Contains Number Of Bits To Be Shifted***
Mnemonic	VI.FSI.FSI_SHIFT.FRONY_END_LENGTH_REGISTER
Address	0000000000000C02 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:7	RWX	control_bits control
8:31	RWX	front_end_length front end length

Register Name	***Returns The Content Of The Buffer Placed Between FIFO And Scan Data***
Mnemonic	VI.FSI.FSI_SHIFT.READ_BUFFER
Address	0000000000000C03 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	READ_BUFFER_REG: Read receive buffer

Register Name	*Reset All Regs*
Mnemonic	VI.FSI.FSI_SHIFT.RESET
Address	0000000000000C06 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WOX	reset Reset

Register Name	*Reset Errors*
Mnemonic	VI.FSI.FSI_SHIFT.RESET_ERRORS
Address	0000000000000C07 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WOX	reset_errors Reset errors

Register Name	*Status Register*
Mnemonic	VI.FSI.FSI_SHIFT.STATUS
Address	0000000000000C07 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	status__register Bit0 : Front end count NOT zero (also readable via peek engine) Bit1 : Command address parity (LBUS address) (also readable via peek engine) Bit2 : Back end parity (data read from FIFO has incorrect parity) (also readable via peek engine) Bit3-4 : 3:FIFO overrun, 4: FIFO underrun; any active bit would indicate a hardware error Bit5 : Command overrun (also readable via peek engine) Bit6 : Header check failed: TP scan: receive_buffer(32:39) != 0xA5; PIB scan receive_buffer(0:31) != 0xA5A55A5A Bit7-9 : Reserved Bit10 : internal state machine busy Bit11 : No zeros detected during shift Bit12 : No ones detected during shift Bit13-16 : Reserved Bit17-19 : PCB/PIB error condition Bit20 : Parity error on incoming data Bit21 : PIB abort Bit22-23 : Reserved Bit24-31 : FIFO level

Register Name	*Extra Status*
Mnemonic	VI.FSI.FSI_SHIFT.EXTENDED_STATUS
Address	0000000000000C08 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:15	RO	constant=0b0000000000000100
16	ROX	residual_fe_cnt_is_zero Residual FE Count equal to zero
17:31	RO	constant=0b000000000000001

Register Name	***CFAM CHIP ID***
Mnemonic	VI.FSI.FSI_SHIFT.CHIP_ID
Address	0000000000000C09 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:19	ROX	cfam_chip_id CHIP ID comes from outside
20:31	RO	constant=0b000001001001

Register Name	***Complement Mask Register***
Mnemonic	VI.FSI.FSI_SHIFT.COMPLEMENT_MASK
Address	0000000000000C0C (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	COMPLEMENT_MASK_REG: Complement Mask for controlling generation of interrupts

Register Name	***True Mask Register***
Mnemonic	VI.FSI.FSI_SHIFT.TRUE_MASK
Address	0000000000000C0D (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	TRUE_MASK_REG: True Mask for controlling generation of interrupts

Register Name	***Shift Control Register***
Mnemonic	VI.FSI.FSI_SHIFT.SHIFT_CONTROL_REGISTER_2
Address	0000000000000C10 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	SHIFT_CONTROL_REGISTER: Controls the length of the set pulse

Register Name	*DMA Mode Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_MODE_REGISTER
Address	0000000000000C19 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	RW	DMA_MODE_REG_ENABLE: enables DMA mode for DMA-based CFAM init
1	RW	DMA_MODE_REG_FIFO_SIZE_EQ_1: set FIFO size to 1 (for debugging purposes)
2:31	RW	DMA_MODE_REG_UNUSED: Reserved

Register Name	*DMA Status Compare Mask Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_STAT_COMP_MASK_REGISTER
Address	0000000000000C1A (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_STAT_COMP_MASK_REG: defines the error bits of the status register (for debugging purposes)

Register Name	*DMA OP/BLOCKSIZE Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_OP_BLOCKSIZE_REGISTER
Address	0000000000000C1B (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:7	RW	DMA_OP_BLOCKSIZE_OPCODE: operation code of block command (for debugging purposes)
8:31	RW	DMA_OP_BLOCKSIZE_SIZE: size of block command (for debugging purposes)

Register Name	*DMA Remaining Size Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_REM_SIZE_REGISTER
Address	0000000000000C1C (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:7	RO	constant=0b00000000

Bits	FSI	Field Mnemonic: Description
8:31	RW	DMA_REM_SIZE_REMAINING_WORDS: number of 32bit words to be executed to complete block command

Register Name	*DMA PIB Send Data0 Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_PIB_SND_BUFFER0_REGISTER
Address	0000000000000C1D (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_PIB_SND_BUF0_REG_DATA0: holds the data to be sent to PIB (for debugging purposes)

Register Name	*DMA PIB Send Data1 Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_PIB_SND_BUFFER1_REGISTER
Address	0000000000000C1E (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_PIB_SND_BUF1_REG_DATA0: holds the data to be sent to PIB (for debugging purposes)

Register Name	*DMA PIB Receive Data0 Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_PIB_RCV_BUFFER0_REGISTER
Address	0000000000000C1F (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_PIB_RCV_BUF0_REG_DATA0: buffers the read data from PIB (for debugging purposes)

Register Name	*DMA PIB Receive Data1 Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_PIB_RCV_BUFFER1_REGISTER
Address	0000000000000C20 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_PIB_RCV_BUF1_REG_DATA1: buffers the read data from PIB (for debugging purposes)

Register Name	*DMA Error Pointer Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_ERROR_PTR_REGISTER
Address	0000000000000C21 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_ERROR_PTR_REG: points to the last loaded block command word (for debugging purposes)

Register Name	*DMA SCOM Command Register*
Mnemonic	VI.FSI.FSI_SHIFT.DMA_SCOM_CMD_REGISTER
Address	0000000000000C22 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	DMA_SCOM_CMD_REG: holds the SCOM command (for debugging purposes)

Register Name	*FSI Data Register 0*
Mnemonic	VI.FSI.DATA_REGISTER_0
Address	0000000000001000 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	DATA_REG_0: First 32 bits for PIB access

Register Name	*FSI Data Register 1*
Mnemonic	VI.FSI.DATA_REGISTER_1
Address	0000000000001001 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	DATA_REG_1: Second 32 bits for PIB access

Register Name	***Contains Command To The FSI2PIB Engine***
Mnemonic	VI.FSI.COMMAND_REGISTER
Address	0000000000001002 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	CMD_REG: command register

Register Name	***Resets Data,command,status Registers***
Mnemonic	VI.FSI.RESET
Address	0000000000001006 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	reset resets command,mode,watermark,interrupt mask,status,complement mask,true mask registers

Register Name	***Reset PIB Master IF***
Mnemonic	VI.FSI.SET_PIB_RESET
Address	0000000000001007 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	set_pib_reset Reset PIB master IF

Register Name	***Status Register***
Mnemonic	VI.FSI.STATUS
Address	0000000000001007 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	status__register Bit0 : Any error, ORing of bits 1,2,3,5 (also readable via the peek engine) Bit1 : System checkstop (also readable via the peek engine) Bit2 : Special attention (also readable via the peek engine) Bit3 : recoverable error (also readable via the peek engine) Bit4 : Chiplet interrupt (also readable via the peek engine) Bit5 : Reserved (also readable via the peek engine) Bit6 : Reserved (also readable via the peek engine) Bit7 : FSI2PIB idle (also readable via the peek engine) Bit8 : Reserved, may read 0 OR 1 Bit9 : Reserved Bit10 : Reserved Bit11 : PIB abort (=PIB reset during PIB access) Bit12-15: Reserved Bit16 : VDD nest observe Bit17-19: PCB/PIB error Bit20-23: Reserved Bit24 : PLL lock nest Bit25 : PLL lock mem Bit28 : Interrupt condition pending Bit29 : Interrupts enabled Bit30 : Reserved Bit31 : Any region stopped

Register Name	*CFAM Chip ID*
Mnemonic	VI.FSI.CHIPID
Address	000000000000100A (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:19	ROX	chip_id Chip ID
20:31	RO	constant=0b000001001001

Register Name	*INTERRUPT STATUS Register*
Mnemonic	VI.FSI.INTERRUPT
Address	000000000000100B (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	INTERRUPT_STATUS_REG: Contains status information, but gets frozen when interrupt occurs

Register Name	*Complement Mask Register*
Mnemonic	VI.FSI.COMPLEMENT_MASK
Address	000000000000100C (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	COMPLEMENT_MASK_REG: Complement Mask for controlling generation of interrupts

Register Name	*True Mask Register*
Mnemonic	VI.FSI.TRUE_MASK
Address	000000000000100D (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	TRUE_MASK_REG: True Mask for controlling generation of interrupts

Register Name	*FSI GP3 Register*
Mnemonic	VI.FSI.FSIGP3
Address	0000000000001012 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:19	RW	GP3_UNUSED_0_19: not used
20	RW	USE_PIB2PCB_MUX_DC: Directly connect FSI2PIB to pervasive chiplet
21	RW	OOB_MUX_DC: Select OOB mux
22	RW	PCB_RESET_DC: reset of Pervasive chiplet
23	RW	FENCE2_DC: FSI fence2
24	RW	FENCE3_DC: FSI fence3
25	RW	FENCE4_DC: FSI fence4
26	RW	FENCE5_DC: FSI fence5
27	RW	VDD2VIO_LVL_FENCE: VDD2VIO lvl fence.
28	RW	PLL_RESET_DC: Reset signal to all analog PLL
29	RW	PLL_OUT_EN_DC: Enable output signal of PLL
30	RW	GP3_UNUSED_30: not used
31	RW	GLOBAL_EP_RESET_DC: Global endpoint reset to all slaves

Register Name	*FSI GP4 Register*
Mnemonic	VI.FSI.FSIGP4
Address	0000000000001013 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	RW	TPFSI_PLLMEM_ALTREFCLK_ENABLE: PLL MEM altrefclk enable bit0.
1	RW	TPFSI_CLKSTOP_DPHY23_GRID_ENABLE: clockstop DPHY23 grid enable.
2	RW	TPFSI_MEMRST_B: MEM reset_b.
3	RW	TPFSI_FORCE_MCLK_OFF: Force mclk off.
4	RW	TP_CHIP_DPHY_PLLRESET_B:
5	RW	TP_CHIP_DPHY_RESET_ALL: Chip DPHY reset all.
6	RW	TP_CHIP_PADTEST_ENABLE: Chip padtest enable.
7	RW	TPFSI_TP_PLLMEM_ALTREFCLK_ENABLE: PLL MEM altrefclk enable bit1.
8:9	RW	TCN_DMI_TERM_DC: TCN DMI term
10:11	RW	TCM_DDR_TERM_DC: TCM DDR term
12:15	RW	GLBCK_RELAY_STRENGTH_DC: Global clocking sector buffer strength
16:20	RW	GP4_UNUSED_16_20: not used
21	RW	TPFSI_ARRAY_SET_VBL_TO_VDD_DC: Array set vbl to vdd.
22:23	RW	GP4_UNUSED_22_23: not used

Bits	FSI	Field Mnemonic: Description
24	RW	TPFSI_TP_PLL_TEST_ENABLE_DC: PLL test enable.
25:27	RW	GP4_UNUSED_25_27: not used
28	RW	TP_RI_DC_B: Receiver inhibit
29	RW	TP_DI1_DC_B: Driver inhibit
30	RW	GP4_UNUSED_30: not used
31	RW	GP4_UNUSED_31: not used

Register Name	*FSI GP5 Register*
Mnemonic	VI.FSI.FSIGP5
Address	0000000000001014 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:3	RW	PROBE0_SEL_DC: Probe0 select.
4:7	RW	PROBE1_SEL_DC: Probe1 select.
8	RW	PROBE_MESH_SEL_DC: Probe mesh select.
9	RW	PROBE_DRV_EN_DC: Probe drive enable.
10	RW	GP5_UNUSED_10: not used.
11	RW	GP5_UNUSED_11: not used.
12:15	RW	GP5_UNUSED_12_15: not used.
16:17	RW	FSI_PROBE_SEL_DC: FSI probe select.
18:22	RW	GP5_UNUSED_18_22: not used.
23	RW	PLL_DRV_EN_DC: PLL driver enable.
24	RW	DBG_PCB_ASYNC_EN_DC: Debug PCB async enable.
25	RW	DBG_PCB_DATA_PAR_DIS_DC: Debug PCB data parity disable.
26	RW	DBG_PCB_TYPE_PAR_DIS_DC: Debug PCB type parity disable.
27	RW	PCB_GSD_LATCHED_MODE_DC: PCB GSD latched mode.
28	RW	PIB_DISABLE_PARITY_DC: PIB master slave parity disable.
29:31	RW	GPIO_PIB_TIMEOUT: PIB timeout.

Register Name	*FSI GP6 Register*
Mnemonic	VI.FSI.FSIGP6
Address	0000000000001015 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	GP6_UNUSED_0_31: not used

Register Name	*FSI GP7 Register*
Mnemonic	VI.FSI.FSIGP7
Address	0000000000001016 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:3	RW	DPHYN_PROGDLY_SETTING_DC: DPHYN prog delay setting.
4:7	RW	DPHYS_PROGDLY_SETTING_DC: DPHYS prog delay setting.
8:11	RW	MBC_PROGDLY_SETTING_DC: MBC prog delay setting.
12:15	RW	MEM_PROGDLY_SETTING_DC: MEM prog delay setting.
16:19	RW	NEST_PROGDLY_SETTING_DC: NEST prog delay setting.
20:31	RW	GP7_UNUSED_20_31: not used.

Register Name	*GP Write Protection Register*
Mnemonic	VI.FSI.GPWRP
Address	0000000000001018 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:15	RWX	MAGIC_COOKIE: It needs to be programmed to 0x4453 for enabling write protection
16:31	RWX	EN_OR_DIS_WRITE_PROTECTION: If equal to xFFFF disabled write protection If it is unequal to xFFFF then this part along with magic cookie forms the if equal to x'0003' : register number of GP3 if equal to x'0004' : register number of GP4 if equal to x'0005' : register number of GP5 if equal to x'0006' : register number of GP6 if equal to x'0007' : register number of GP7

Register Name	*Osc Switch Sense 1 Register*
Mnemonic	VI.FSI.SNS1LTH
Address	0000000000001019 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RO	SNS1_UNUSED_0_31: not used

Register Name	*Osc Switch Sense 2 Register*
Mnemonic	VI.FSI.SNS2LTH
Address	000000000000101A (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RO	SNS2_UNUSED_0_31: not used

Register Name	*PERV GP3 Register*
Mnemonic	VI.FSI.PERV_GP3
Address	000000000000101B (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	RW	TP_CHIPLET_CHIPLET_EN_DC: Set if chiplet is good (NO partial good control)
1	RW	TP_CHIPLET_PCB_EP_RESET_DC: Global EP reset
2:4	RW	PERV_GP3_UNUSED_2_4: not used
5	RW	TP_PLLNST_BYPASS_EN_DC: PLL NEST bypass enable
6:10	RW	PERV_GP3_UNUSED_6_10: not used
11	RW	TP_CHIPLET_VTL_D_MODE_DC: LCB control for vital logic
12	RW	TP_CHIPLET_VTL_ACT_DIS_DC: LCB control for vital logic
13	RW	TP_CHIPLET_VTL_MPW2_DC_B: LCB control for vital logic
14	RW	TP_CHIPLET_VTL_MPW1_DC_B: LCB control for vital logic
15	RW	TP_CHIPLET_VTL_DELAY_LCLKR_DC: LCB control for vital logic
16	RW	TP_CHIPLET_VTL_CLKOFF_DC: LCB control for vital logic
17	RW	TP_CHIPLET_PLL_BYPASS_EN_DC:
18	RW	TP_CHIPLET_FENCE_EN_DC: Fencing for the chiplet
19:31	RW	PERV_GP3_UNUSED_19_31: not used

Register Name	*Scratch Pad Size*
Mnemonic	VI.FSI.SCPSIZE
Address	0000000000001400 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RO	scr0_rd_data Scratch pad size

Register Name	*FSI Scratch Pad*
Mnemonic	VI.FSI.FSISCRPD
Address	0000000000001401 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	FSI_SCRATCH_PAD: FSI scratch pad register

Register Name	*Contains Data To Be Written Onto The Fifo*
Mnemonic	VI.FSI.FSI_I2C.FIFO_REGISTER
Address	0000000000001800 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:7	RWX	fifo_bits_write0 fifo data byte 0
8:31	RO	constant=0b00000000000000000000000

Register Name	*Contains Command To The I2c Engine*
Mnemonic	VI.FSI.FSI_I2C.COMMAND_REGISTER
Address	0000000000001801 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RW	CMD_REG: command register

Register Name	*Contains Speed Information*
Mnemonic	VI.FSI.FSI_I2C.MODE_REGISTER
Address	0000000000001802 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:15	RW	BIT_RATE_DIVISOR: bit rate
16:21	RW	PORT_NUMBER: port number
22:27	RO	constant=0b000000
28	RW	FGAT_MODE: fgat mode
29	RW	DIAG_MODE: diag mode
30	RW	PACING_ALLOW_MODE: pacing allow mode
31	RW	WRAP_MODE: wrap_mode

Register Name	*Water Mark Register*
Mnemonic	VI.FSI.FSI_I2C.WATER_MARK_REGISTER
Address	0000000000001803 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:15	RO	constant=0b0000000000000000
16:31	RW	WATERMARK_REG: water mark register

Register Name	*Write To Interrupt Mask Register*
Mnemonic	VI.FSI.FSI_I2C.INTERRUPT_MASK_REGISTER
Address	0000000000001804 (FSI) 0000000000001805 (FSI1) 0000000000001806 (FSI2)
Attributes	
Description	

Bits	FSI	FSI1	FSI2	Field Mnemonic: Description
0:15	RO	RO	RO	constant=0b0000000000000000
16:31	RW	WO_OR	WO_AND	INT_MASK: interrupt mask register

Register Name	*Interrupt Conditions*
Mnemonic	VI.FSI.FSI_I2C.INTERRUPT_COND
Address	0000000000001805 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	int_conds interrupt conditions

Register Name	*Interrupts*
Mnemonic	VI.FSI.FSI_I2C.INTERRUPTS
Address	0000000000001806 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	ints interrupts

Register Name	***Resets Command,mode,watermark,interrupt Mask,status Registers***
Mnemonic	VI.FSI.FSI_I2C.IMM_RESET_I2C
Address	0000000000001807 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	imm_reset_i2c resets command,mode,watermark,interrupt mask,status registers

Register Name	***Status Of The Engine***
Mnemonic	VI.FSI.FSI_I2C.STATUS_REGISTER
Address	0000000000001807 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	ROX	invalid_cmd invalid command
1	ROX	lbus_parity_error local bus parity error
2	ROX	be_ov_error back end overrun error
3	ROX	be_acc_error back end access error
4	ROX	arbitration_lost_error arbitration lost error
5	ROX	nack_received_error nack received error
6	ROX	data_request data request
7	ROX	cmd_complete command complete
8	ROX	stop_error stop error
9:15	RW	
16	ROX	any_i2c_int any_i2c_int
17:19	RO	constant=0b000
20	ROX	scl_syn scl_syn
21	ROX	sda_syn sda_syn
22	ROX	i2c_busy i2c busy
23	ROX	self_busy self busy

Bits	FSI	Field Mnemonic: Description
24:31	ROX	fifo_entry_count fifo_entry count

Register Name	***Extra Status***
Mnemonic	VI.FSI.FSI_I2C.EXTENDED_STATUS
Address	0000000000001808 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:7	ROX	fifo_size total fifo size
8:10	RO	constant=0b000
11:15	ROX	msm_curr_state current state
16	ROX	scl_syn_ext scl_syn
17	ROX	sda_syn_ext sda_syn
18	ROX	s_scl s_sdl
19	ROX	s_sda s_sda
20	ROX	m_scl m_scl
21	ROX	m_sda m_sda
22	ROX	high_water high water mark
23	ROX	low_water low water mark
24	ROX	i2c_busy_ext i2c busy
25	ROX	self_busy_ext self busy
26:31	RO	constant=0b010101

Register Name	***Resets Fifo ,some Status Bits And State Machine***
Mnemonic	VI.FSI.FSI_I2C.IMM_RESET_ERR
Address	0000000000001808 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	imm_reset_errors resets fifo ,some status bits and state machine

Register Name	*Sets Output S_scl*
Mnemonic	VI.FSI.FSI_I2C.IMM_SET_S_SCL
Address	0000000000001809 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	imm_set_s_scl sets output s_scl

Register Name	*Residual Data Length*
Mnemonic	VI.FSI.FSI_I2C.RESIDUAL_FRONT_END_BACK_END_LENGTH
Address	0000000000001809 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:15	ROX	resid_fe_len residual front end length register
16:31	ROX	resid_be_len residual back end length register

Register Name	*Resets Output S_scl*
Mnemonic	VI.FSI.FSI_I2C.IMM_RESET_S_SCL
Address	000000000000180B (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	imm_reset_s_scl resets output s_scl

Register Name	*Sets Output S_sda*
Mnemonic	VI.FSI.FSI_I2C.IMM_SET_S_SDA
Address	000000000000180C (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	imm_set_s_sda sets output s_sda

Register Name	*Sets Output S_sda*
Mnemonic	VI.FSI.FSI_I2C.IMM_RESET_S_SDA
Address	000000000000180D (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	imm_reset_s_sda sets output s_sda

Register Name	*Input Register Which Reflects Status Of GPIO Inputs*
Mnemonic	VI.FSI.FSI_GPIO.GPIO_INPUT_REGISTER
Address	0000000000001C00 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:1	ROX	GPIO_INPUT_REGISTER_READ_DATA: Stores all GPIO Inputs
2:31	RO	constant=0b00000000000000000000000000000000

Register Name	*Output Register Which Reflects Status Of GPIO Outputs*
Mnemonic	VI.FSI.FSI_GPIO.GPIO_OUPUT_REGISTER
Address	0000000000001C01 (FSI) 0000000000001C02 (FSI1) 0000000000001C03 (FSI2)
Attributes	
Description	

Bits	FSI	FSI1	FSI2	Field Mnemonic: Description
0:1	RW	WO_OR	WO_AND	GPIO_OUTPUT_REGISTER_READ_WRITE_DATA: Stores all GPIO Outputs
2:31	RO	RO	RO	constant=0b00000000000000000000000000000000

Register Name	*Output Enable Register For Masking*
Mnemonic	VI.FSI.FSI_GPIO.GPIO_OUPUT_ENABLE_REGISTER
Address	0000000000001C04 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:1	RW	GPIO_OUTPUT_ENABLE_REGISTER_READ_WRITE_DATA: Stores all GPIO Output Mask info
2:31	RO	constant=0b00000000000000000000000000000000

Register Name	*Interrupt Register Which Reflects Status Of Interrupts From GPIO Inputs*
Mnemonic	VI.FSI.FSI_GPIO.GPIO_INTERRUPT_REGISTER
Address	0000000000001C07 (FSI) 0000000000001C0E (FSI2) 0000000000001C0F (FSI1)
Attributes	
Description	

Bits	FSI	FSI2	FSI1	Field Mnemonic: Description
0:1	RO	WO_AND	WO_OR	GPIO_INTERRUPT_REGISTER_READ_DATA: Stores all GPIO Interrupts info
2:31	RO	RO	RO	constant=0b00000000000000000000000000000000

Register Name	*Polarity Register Of GPIO*
Mnemonic	VI.FSI.FSI_GPIO.GPIO_POLARITY_REGISTER
Address	0000000000001C0C (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:1	RW	GPIO_POLARITY_REGISTER_READ_WRITE_DATA: Stores all GPIO Polarity info
2:31	RO	constant=0b00000000000000000000000000000000

Register Name	*Interrupt Enable Register For Masking*
Mnemonic	VI.FSI.FSI_GPIO.GPIO_INTERRUPT_ENABLE_REGISTER
Address	0000000000001C0D (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:1	RW	GPIO_INTERRUPT_ENABLE_REGISTER_READ_WRITE_DATA: Interrupt Enable register bits
2:31	RO	constant=0b00000000000000000000000000000000

Register Name	*FSI Data Register 0*
Mnemonic	VI.FSI.I2_DATA_REGISTER_0
Address	0000000000002000 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	I2_DATA_REG_0: First 32 bits for PIB access

Register Name	*FSI Data Register 1*
Mnemonic	VI.FSI.I2_DATA_REGISTER_1
Address	0000000000002001 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	I2_DATA_REG_1: Second 32 bits for PIB access

Register Name	*Contains Command To The FSI2PIB Engine*
Mnemonic	VI.FSI.I2_COMMAND_REGISTER
Address	0000000000002002 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	I2_CMD_REG: command register

Register Name	*Resets Data,command,status Registers*
Mnemonic	VI.FSI.I2_RESET
Address	0000000000002006 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	reset resets command,mode,watermark,interrupt mask,status,complement mask,true mask registers

Register Name	*Reset PIB Master IF*
Mnemonic	VI.FSI.I2_SET_PIB_RESET
Address	0000000000002007 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WO	set_pib_reset Reset PIB master IF

Register Name	*Status Register*
Mnemonic	VI.FSI.I2_STATUS
Address	0000000000002007 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	status__register Bit0 : Any error, OR of bits 1 to 5 (also readable via the peek engine) Bit1 : System checkstop (also readable via the peek engine) Bit2 : Special attention (also readable via the peek engine) Bit3 : recoverable error (also readable via the peek engine) Bit4 : Chiplet interrupt (also readable via the peek engine) Bit5 : Reserved (also readable via the peek engine) Bit6 : Reserved (also readable via the peek engine) Bit7 : FSI2PIB idle (also readable via the peek engine) Bit8 : Reserved, may read 0 OR 1, ORed unqualified scerror from PIB, use bit 17 to 19 instead Bit9 : Reserved Bit10 : Reserved Bit11 : PIB abort (=PIB reset during PIB access) Bit12-15: Reserved Bit16 : VDD nest observe Bit17-19: PCB/PIB error Bit20-23: Reserved Bit24 : PLL lock nest Bit25 : PLL lock mem Bit28 : Interrupt condition pending Bit29 : Interrupts enabled Bit30 : Reserved Bit31 : Any region stopped

Register Name	*CFAM Chip ID*
Mnemonic	VI.FSI.I2_CHIPID
Address	000000000000200A (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:19	ROX	chip_id Chip ID
20:31	RO	constant=0b000001001001

Register Name	*INTERRUPT STATUS Register*
Mnemonic	VI.FSI.I2_INTERRUPT
Address	000000000000200B (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	I2_INTERRUPT_STATUS_REG: Contains status information, but gets frozen when interrupt occurs

Register Name	*Complement Mask Register*
Mnemonic	VI.FSI.I2_COMPLEMENT_MASK
Address	000000000000200C (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	I2_COMPLEMENT_MASK_REG: Complement Mask for controlling generation of interrupts

Register Name	*True Mask Register*
Mnemonic	VI.FSI.I2_TRUE_MASK
Address	000000000000200D (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	I2_TRUE_MASK_REG: True Mask for controlling generation of interrupts

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART0_REGISTER
Address	0000000000010000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART1_REGISTER
Address	0000000000010001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART2_REGISTER
Address	0000000000010002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART3_REGISTER
Address	0000000000010003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART4_REGISTER
Address	0000000000010004 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART5_REGISTER
Address	0000000000010005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART6_REGISTER
Address	0000000000010006 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART7_REGISTER
Address	0000000000010007 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART8_REGISTER
Address	0000000000010008 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART9_REGISTER
Address	0000000000010009 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART10_REGISTER
Address	000000000001000A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART11_REGISTER
Address	000000000001000B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART12_REGISTER
Address	000000000001000C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART13_REGISTER
Address	000000000001000D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART14_REGISTER
Address	000000000001000E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART15_REGISTER
Address	000000000001000F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART16_REGISTER
Address	0000000000010010 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART17_REGISTER
Address	0000000000010011 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART18_REGISTER
Address	0000000000010012 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART19_REGISTER
Address	0000000000010013 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART20_REGISTER
Address	0000000000010014 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART21_REGISTER
Address	0000000000010015 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART22_REGISTER
Address	0000000000010016 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART23_REGISTER
Address	0000000000010017 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART24_REGISTER
Address	0000000000010018 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART25_REGISTER
Address	0000000000010019 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART26_REGISTER
Address	000000000001001A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART27_REGISTER
Address	000000000001001B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART28_REGISTER
Address	000000000001001C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART29_REGISTER
Address	000000000001001D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART30_REGISTER
Address	000000000001001E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART31_REGISTER
Address	000000000001001F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART32_REGISTER
Address	0000000000010020 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART33_REGISTER
Address	0000000000010021 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART34_REGISTER
Address	0000000000010022 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART35_REGISTER
Address	0000000000010023 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART36_REGISTER
Address	0000000000010024 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART37_REGISTER
Address	0000000000010025 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART38_REGISTER
Address	0000000000010026 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART39_REGISTER
Address	0000000000010027 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART40_REGISTER
Address	0000000000010028 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART41_REGISTER
Address	0000000000010029 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART42_REGISTER
Address	000000000001002A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART43_REGISTER
Address	000000000001002B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART44_REGISTER
Address	000000000001002C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART45_REGISTER
Address	000000000001002D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART46_REGISTER
Address	000000000001002E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART47_REGISTER
Address	000000000001002F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART48_REGISTER
Address	0000000000010030 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART49_REGISTER
Address	0000000000010031 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART50_REGISTER
Address	0000000000010032 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART51_REGISTER
Address	0000000000010033 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART52_REGISTER
Address	0000000000010034 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART53_REGISTER
Address	0000000000010035 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART54_REGISTER
Address	0000000000010036 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART55_REGISTER
Address	0000000000010037 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART56_REGISTER
Address	0000000000010038 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART57_REGISTER
Address	0000000000010039 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART58_REGISTER
Address	000000000001003A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART59_REGISTER
Address	000000000001003B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART60_REGISTER
Address	000000000001003C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART61_REGISTER
Address	000000000001003D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART62_REGISTER
Address	000000000001003E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#0.OTPROM.ECID_PART63_REGISTER
Address	000000000001003F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART0_REGISTER
Address	0000000000010040 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART1_REGISTER
Address	0000000000010041 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART2_REGISTER
Address	0000000000010042 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART3_REGISTER
Address	0000000000010043 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART4_REGISTER
Address	0000000000010044 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART5_REGISTER
Address	0000000000010045 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART6_REGISTER
Address	0000000000010046 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART7_REGISTER
Address	0000000000010047 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART8_REGISTER
Address	0000000000010048 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART9_REGISTER
Address	0000000000010049 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART10_REGISTER
Address	000000000001004A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART11_REGISTER
Address	000000000001004B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART12_REGISTER
Address	000000000001004C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART13_REGISTER
Address	000000000001004D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART14_REGISTER
Address	000000000001004E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART15_REGISTER
Address	000000000001004F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART16_REGISTER
Address	0000000000010050 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART17_REGISTER
Address	0000000000010051 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART18_REGISTER
Address	0000000000010052 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART19_REGISTER
Address	0000000000010053 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART20_REGISTER
Address	0000000000010054 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART21_REGISTER
Address	0000000000010055 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART22_REGISTER
Address	0000000000010056 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART23_REGISTER
Address	0000000000010057 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART24_REGISTER
Address	0000000000010058 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART25_REGISTER
Address	0000000000010059 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART26_REGISTER
Address	000000000001005A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART27_REGISTER
Address	000000000001005B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART28_REGISTER
Address	000000000001005C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART29_REGISTER
Address	000000000001005D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART30_REGISTER
Address	000000000001005E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART31_REGISTER
Address	000000000001005F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART32_REGISTER
Address	0000000000010060 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART33_REGISTER
Address	0000000000010061 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART34_REGISTER
Address	0000000000010062 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART35_REGISTER
Address	0000000000010063 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART36_REGISTER
Address	0000000000010064 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART37_REGISTER
Address	0000000000010065 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART38_REGISTER
Address	0000000000010066 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART39_REGISTER
Address	0000000000010067 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART40_REGISTER
Address	0000000000010068 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART41_REGISTER
Address	0000000000010069 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART42_REGISTER
Address	000000000001006A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART43_REGISTER
Address	000000000001006B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART44_REGISTER
Address	000000000001006C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART45_REGISTER
Address	000000000001006D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART46_REGISTER
Address	000000000001006E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART47_REGISTER
Address	000000000001006F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART48_REGISTER
Address	0000000000010070 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART49_REGISTER
Address	0000000000010071 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART50_REGISTER
Address	0000000000010072 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART51_REGISTER
Address	0000000000010073 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART52_REGISTER
Address	0000000000010074 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART53_REGISTER
Address	0000000000010075 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART54_REGISTER
Address	0000000000010076 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART55_REGISTER
Address	0000000000010077 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART56_REGISTER
Address	0000000000010078 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART57_REGISTER
Address	0000000000010079 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART58_REGISTER
Address	000000000001007A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART59_REGISTER
Address	000000000001007B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART60_REGISTER
Address	000000000001007C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART61_REGISTER
Address	000000000001007D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART62_REGISTER
Address	000000000001007E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#1.OTPROM.ECID_PART63_REGISTER
Address	000000000001007F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART0_REGISTER
Address	0000000000010080 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART1_REGISTER
Address	0000000000010081 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART2_REGISTER
Address	0000000000010082 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART3_REGISTER
Address	0000000000010083 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART4_REGISTER
Address	0000000000010084 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART5_REGISTER
Address	0000000000010085 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART6_REGISTER
Address	0000000000010086 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART7_REGISTER
Address	0000000000010087 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART8_REGISTER
Address	0000000000010088 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART9_REGISTER
Address	0000000000010089 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART10_REGISTER
Address	000000000001008A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART11_REGISTER
Address	000000000001008B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART12_REGISTER
Address	000000000001008C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART13_REGISTER
Address	000000000001008D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART14_REGISTER
Address	000000000001008E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART15_REGISTER
Address	000000000001008F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART16_REGISTER
Address	0000000000010090 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART17_REGISTER
Address	0000000000010091 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART18_REGISTER
Address	0000000000010092 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART19_REGISTER
Address	0000000000010093 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART20_REGISTER
Address	0000000000010094 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART21_REGISTER
Address	0000000000010095 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART22_REGISTER
Address	0000000000010096 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART23_REGISTER
Address	0000000000010097 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART24_REGISTER
Address	0000000000010098 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART25_REGISTER
Address	0000000000010099 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART26_REGISTER
Address	000000000001009A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART27_REGISTER
Address	000000000001009B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART28_REGISTER
Address	000000000001009C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART29_REGISTER
Address	000000000001009D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART30_REGISTER
Address	000000000001009E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART31_REGISTER
Address	000000000001009F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART32_REGISTER
Address	00000000000100A0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART33_REGISTER
Address	00000000000100A1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART34_REGISTER
Address	00000000000100A2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART35_REGISTER
Address	00000000000100A3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART36_REGISTER
Address	00000000000100A4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART37_REGISTER
Address	00000000000100A5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART38_REGISTER
Address	00000000000100A6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART39_REGISTER
Address	00000000000100A7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART40_REGISTER
Address	00000000000100A8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART41_REGISTER
Address	00000000000100A9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART42_REGISTER
Address	00000000000100AA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART43_REGISTER
Address	00000000000100AB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART44_REGISTER
Address	00000000000100AC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART45_REGISTER
Address	00000000000100AD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART46_REGISTER
Address	00000000000100AE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART47_REGISTER
Address	00000000000100AF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART48_REGISTER
Address	00000000000100B0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART49_REGISTER
Address	00000000000100B1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART50_REGISTER
Address	00000000000100B2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART51_REGISTER
Address	00000000000100B3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART52_REGISTER
Address	00000000000100B4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART53_REGISTER
Address	00000000000100B5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART54_REGISTER
Address	00000000000100B6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART55_REGISTER
Address	00000000000100B7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART56_REGISTER
Address	00000000000100B8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART57_REGISTER
Address	00000000000100B9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART58_REGISTER
Address	00000000000100BA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART59_REGISTER
Address	00000000000100BB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART60_REGISTER
Address	00000000000100BC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART61_REGISTER
Address	00000000000100BD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART62_REGISTER
Address	00000000000100BE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#2.OTPROM.ECID_PART63_REGISTER
Address	00000000000100BF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART0_REGISTER
Address	00000000000100C0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART1_REGISTER
Address	00000000000100C1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART2_REGISTER
Address	00000000000100C2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART3_REGISTER
Address	00000000000100C3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART4_REGISTER
Address	00000000000100C4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART5_REGISTER
Address	00000000000100C5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART6_REGISTER
Address	00000000000100C6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART7_REGISTER
Address	00000000000100C7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART8_REGISTER
Address	00000000000100C8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART9_REGISTER
Address	00000000000100C9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART10_REGISTER
Address	00000000000100CA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART11_REGISTER
Address	00000000000100CB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART12_REGISTER
Address	00000000000100CC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART13_REGISTER
Address	00000000000100CD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART14_REGISTER
Address	00000000000100CE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART15_REGISTER
Address	00000000000100CF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART16_REGISTER
Address	00000000000100D0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART17_REGISTER
Address	00000000000100D1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART18_REGISTER
Address	00000000000100D2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART19_REGISTER
Address	00000000000100D3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART20_REGISTER
Address	00000000000100D4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART21_REGISTER
Address	00000000000100D5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART22_REGISTER
Address	00000000000100D6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART23_REGISTER
Address	00000000000100D7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART24_REGISTER
Address	00000000000100D8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART25_REGISTER
Address	00000000000100D9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART26_REGISTER
Address	00000000000100DA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART27_REGISTER
Address	00000000000100DB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART28_REGISTER
Address	00000000000100DC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART29_REGISTER
Address	00000000000100DD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART30_REGISTER
Address	00000000000100DE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART31_REGISTER
Address	00000000000100DF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART32_REGISTER
Address	00000000000100E0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART33_REGISTER
Address	00000000000100E1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART34_REGISTER
Address	00000000000100E2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART35_REGISTER
Address	00000000000100E3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART36_REGISTER
Address	00000000000100E4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART37_REGISTER
Address	00000000000100E5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART38_REGISTER
Address	00000000000100E6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART39_REGISTER
Address	00000000000100E7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART40_REGISTER
Address	00000000000100E8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART41_REGISTER
Address	00000000000100E9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART42_REGISTER
Address	00000000000100EA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART43_REGISTER
Address	00000000000100EB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART44_REGISTER
Address	00000000000100EC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART45_REGISTER
Address	00000000000100ED (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART46_REGISTER
Address	00000000000100EE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART47_REGISTER
Address	00000000000100EF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART48_REGISTER
Address	00000000000100F0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART49_REGISTER
Address	00000000000100F1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART50_REGISTER
Address	00000000000100F2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART51_REGISTER
Address	00000000000100F3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART52_REGISTER
Address	00000000000100F4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART53_REGISTER
Address	00000000000100F5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART54_REGISTER
Address	00000000000100F6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART55_REGISTER
Address	00000000000100F7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART56_REGISTER
Address	00000000000100F8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART57_REGISTER
Address	00000000000100F9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART58_REGISTER
Address	00000000000100FA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART59_REGISTER
Address	00000000000100FB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART60_REGISTER
Address	00000000000100FC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART61_REGISTER
Address	00000000000100FD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART62_REGISTER
Address	00000000000100FE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#3.OTPROM.ECID_PART63_REGISTER
Address	00000000000100FF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART0_REGISTER
Address	0000000000010100 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART1_REGISTER
Address	0000000000010101 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART2_REGISTER
Address	0000000000010102 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART3_REGISTER
Address	0000000000010103 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART4_REGISTER
Address	0000000000010104 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART5_REGISTER
Address	0000000000010105 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART6_REGISTER
Address	0000000000010106 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART7_REGISTER
Address	0000000000010107 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART8_REGISTER
Address	0000000000010108 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART9_REGISTER
Address	0000000000010109 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART10_REGISTER
Address	000000000001010A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART11_REGISTER
Address	000000000001010B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART12_REGISTER
Address	000000000001010C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART13_REGISTER
Address	000000000001010D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART14_REGISTER
Address	000000000001010E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART15_REGISTER
Address	000000000001010F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART16_REGISTER
Address	0000000000010110 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART17_REGISTER
Address	0000000000010111 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART18_REGISTER
Address	0000000000010112 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART19_REGISTER
Address	0000000000010113 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART20_REGISTER
Address	0000000000010114 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART21_REGISTER
Address	0000000000010115 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART22_REGISTER
Address	0000000000010116 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART23_REGISTER
Address	0000000000010117 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART24_REGISTER
Address	0000000000010118 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART25_REGISTER
Address	0000000000010119 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART26_REGISTER
Address	000000000001011A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART27_REGISTER
Address	000000000001011B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART28_REGISTER
Address	000000000001011C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART29_REGISTER
Address	000000000001011D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART30_REGISTER
Address	000000000001011E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART31_REGISTER
Address	000000000001011F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART32_REGISTER
Address	0000000000010120 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART33_REGISTER
Address	0000000000010121 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART34_REGISTER
Address	0000000000010122 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART35_REGISTER
Address	0000000000010123 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART36_REGISTER
Address	0000000000010124 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART37_REGISTER
Address	0000000000010125 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART38_REGISTER
Address	0000000000010126 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART39_REGISTER
Address	0000000000010127 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART40_REGISTER
Address	0000000000010128 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART41_REGISTER
Address	0000000000010129 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART42_REGISTER
Address	000000000001012A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART43_REGISTER
Address	000000000001012B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART44_REGISTER
Address	000000000001012C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART45_REGISTER
Address	000000000001012D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART46_REGISTER
Address	000000000001012E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART47_REGISTER
Address	000000000001012F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART48_REGISTER
Address	0000000000010130 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART49_REGISTER
Address	0000000000010131 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART50_REGISTER
Address	0000000000010132 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART51_REGISTER
Address	0000000000010133 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART52_REGISTER
Address	0000000000010134 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART53_REGISTER
Address	0000000000010135 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART54_REGISTER
Address	0000000000010136 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART55_REGISTER
Address	0000000000010137 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART56_REGISTER
Address	0000000000010138 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART57_REGISTER
Address	0000000000010139 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART58_REGISTER
Address	000000000001013A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART59_REGISTER
Address	000000000001013B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART60_REGISTER
Address	000000000001013C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART61_REGISTER
Address	000000000001013D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART62_REGISTER
Address	000000000001013E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#4.OTPROM.ECID_PART63_REGISTER
Address	000000000001013F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART0_REGISTER
Address	0000000000010140 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART1_REGISTER
Address	0000000000010141 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART2_REGISTER
Address	0000000000010142 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART3_REGISTER
Address	0000000000010143 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART4_REGISTER
Address	0000000000010144 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART5_REGISTER
Address	0000000000010145 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART6_REGISTER
Address	0000000000010146 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART7_REGISTER
Address	0000000000010147 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART8_REGISTER
Address	0000000000010148 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART9_REGISTER
Address	0000000000010149 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART10_REGISTER
Address	000000000001014A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART11_REGISTER
Address	000000000001014B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART12_REGISTER
Address	000000000001014C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART13_REGISTER
Address	000000000001014D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART14_REGISTER
Address	000000000001014E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART15_REGISTER
Address	000000000001014F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART16_REGISTER
Address	0000000000010150 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART17_REGISTER
Address	0000000000010151 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART18_REGISTER
Address	0000000000010152 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART19_REGISTER
Address	0000000000010153 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART20_REGISTER
Address	0000000000010154 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART21_REGISTER
Address	0000000000010155 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART22_REGISTER
Address	0000000000010156 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART23_REGISTER
Address	0000000000010157 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART24_REGISTER
Address	0000000000010158 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART25_REGISTER
Address	0000000000010159 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART26_REGISTER
Address	000000000001015A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART27_REGISTER
Address	000000000001015B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART28_REGISTER
Address	000000000001015C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART29_REGISTER
Address	000000000001015D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART30_REGISTER
Address	000000000001015E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART31_REGISTER
Address	000000000001015F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART32_REGISTER
Address	0000000000010160 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART33_REGISTER
Address	0000000000010161 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART34_REGISTER
Address	0000000000010162 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART35_REGISTER
Address	0000000000010163 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART36_REGISTER
Address	0000000000010164 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART37_REGISTER
Address	0000000000010165 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART38_REGISTER
Address	0000000000010166 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART39_REGISTER
Address	0000000000010167 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART40_REGISTER
Address	0000000000010168 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART41_REGISTER
Address	0000000000010169 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART42_REGISTER
Address	000000000001016A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART43_REGISTER
Address	000000000001016B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART44_REGISTER
Address	000000000001016C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART45_REGISTER
Address	000000000001016D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART46_REGISTER
Address	000000000001016E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART47_REGISTER
Address	000000000001016F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART48_REGISTER
Address	0000000000010170 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART49_REGISTER
Address	0000000000010171 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART50_REGISTER
Address	0000000000010172 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART51_REGISTER
Address	0000000000010173 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART52_REGISTER
Address	0000000000010174 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART53_REGISTER
Address	0000000000010175 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART54_REGISTER
Address	0000000000010176 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART55_REGISTER
Address	0000000000010177 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART56_REGISTER
Address	0000000000010178 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART57_REGISTER
Address	0000000000010179 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART58_REGISTER
Address	000000000001017A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART59_REGISTER
Address	000000000001017B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART60_REGISTER
Address	000000000001017C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART61_REGISTER
Address	000000000001017D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART62_REGISTER
Address	000000000001017E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#5.OTPROM.ECID_PART63_REGISTER
Address	000000000001017F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART0_REGISTER
Address	0000000000010180 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART1_REGISTER
Address	0000000000010181 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART2_REGISTER
Address	0000000000010182 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART3_REGISTER
Address	0000000000010183 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART4_REGISTER
Address	0000000000010184 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART5_REGISTER
Address	0000000000010185 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART6_REGISTER
Address	0000000000010186 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART7_REGISTER
Address	0000000000010187 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART8_REGISTER
Address	0000000000010188 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART9_REGISTER
Address	0000000000010189 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART10_REGISTER
Address	000000000001018A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART11_REGISTER
Address	000000000001018B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART12_REGISTER
Address	000000000001018C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART13_REGISTER
Address	000000000001018D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART14_REGISTER
Address	000000000001018E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART15_REGISTER
Address	000000000001018F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART16_REGISTER
Address	0000000000010190 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART17_REGISTER
Address	0000000000010191 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART18_REGISTER
Address	0000000000010192 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART19_REGISTER
Address	0000000000010193 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART20_REGISTER
Address	0000000000010194 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART21_REGISTER
Address	0000000000010195 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART22_REGISTER
Address	0000000000010196 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART23_REGISTER
Address	0000000000010197 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART24_REGISTER
Address	0000000000010198 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART25_REGISTER
Address	0000000000010199 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART26_REGISTER
Address	000000000001019A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART27_REGISTER
Address	000000000001019B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART28_REGISTER
Address	000000000001019C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART29_REGISTER
Address	000000000001019D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART30_REGISTER
Address	000000000001019E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART31_REGISTER
Address	000000000001019F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART32_REGISTER
Address	00000000000101A0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART33_REGISTER
Address	00000000000101A1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART34_REGISTER
Address	00000000000101A2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART35_REGISTER
Address	00000000000101A3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART36_REGISTER
Address	00000000000101A4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART37_REGISTER
Address	00000000000101A5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART38_REGISTER
Address	00000000000101A6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART39_REGISTER
Address	00000000000101A7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART40_REGISTER
Address	00000000000101A8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART41_REGISTER
Address	00000000000101A9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART42_REGISTER
Address	00000000000101AA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART43_REGISTER
Address	00000000000101AB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART44_REGISTER
Address	00000000000101AC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART45_REGISTER
Address	00000000000101AD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART46_REGISTER
Address	00000000000101AE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART47_REGISTER
Address	00000000000101AF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART48_REGISTER
Address	00000000000101B0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART49_REGISTER
Address	00000000000101B1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART50_REGISTER
Address	00000000000101B2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART51_REGISTER
Address	00000000000101B3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART52_REGISTER
Address	00000000000101B4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART53_REGISTER
Address	00000000000101B5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART54_REGISTER
Address	00000000000101B6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART55_REGISTER
Address	00000000000101B7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART56_REGISTER
Address	00000000000101B8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART57_REGISTER
Address	00000000000101B9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART58_REGISTER
Address	00000000000101BA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART59_REGISTER
Address	00000000000101BB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART60_REGISTER
Address	00000000000101BC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART61_REGISTER
Address	00000000000101BD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART62_REGISTER
Address	00000000000101BE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#6.OTPROM.ECID_PART63_REGISTER
Address	00000000000101BF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART0_REGISTER
Address	00000000000101C0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART1_REGISTER
Address	00000000000101C1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART2_REGISTER
Address	00000000000101C2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART3_REGISTER
Address	00000000000101C3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART4_REGISTER
Address	00000000000101C4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART5_REGISTER
Address	00000000000101C5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART6_REGISTER
Address	00000000000101C6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART7_REGISTER
Address	00000000000101C7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART8_REGISTER
Address	00000000000101C8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART9_REGISTER
Address	00000000000101C9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART10_REGISTER
Address	00000000000101CA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART11_REGISTER
Address	00000000000101CB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART12_REGISTER
Address	00000000000101CC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART13_REGISTER
Address	00000000000101CD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART14_REGISTER
Address	00000000000101CE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART15_REGISTER
Address	00000000000101CF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART16_REGISTER
Address	00000000000101D0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART17_REGISTER
Address	00000000000101D1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART18_REGISTER
Address	00000000000101D2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART19_REGISTER
Address	00000000000101D3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART20_REGISTER
Address	00000000000101D4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART21_REGISTER
Address	00000000000101D5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART22_REGISTER
Address	00000000000101D6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART23_REGISTER
Address	00000000000101D7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART24_REGISTER
Address	00000000000101D8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART25_REGISTER
Address	00000000000101D9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART26_REGISTER
Address	00000000000101DA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART27_REGISTER
Address	00000000000101DB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART28_REGISTER
Address	00000000000101DC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART29_REGISTER
Address	00000000000101DD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART30_REGISTER
Address	00000000000101DE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART31_REGISTER
Address	00000000000101DF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART32_REGISTER
Address	00000000000101E0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART33_REGISTER
Address	00000000000101E1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART34_REGISTER
Address	00000000000101E2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART35_REGISTER
Address	00000000000101E3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART36_REGISTER
Address	00000000000101E4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART37_REGISTER
Address	00000000000101E5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART38_REGISTER
Address	00000000000101E6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART39_REGISTER
Address	00000000000101E7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART40_REGISTER
Address	00000000000101E8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART41_REGISTER
Address	00000000000101E9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART42_REGISTER
Address	00000000000101EA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART43_REGISTER
Address	00000000000101EB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART44_REGISTER
Address	00000000000101EC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART45_REGISTER
Address	00000000000101ED (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART46_REGISTER
Address	00000000000101EE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART47_REGISTER
Address	00000000000101EF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART48_REGISTER
Address	00000000000101F0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART49_REGISTER
Address	00000000000101F1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART50_REGISTER
Address	00000000000101F2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART51_REGISTER
Address	00000000000101F3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART52_REGISTER
Address	00000000000101F4 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART53_REGISTER
Address	00000000000101F5 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART54_REGISTER
Address	00000000000101F6 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART55_REGISTER
Address	00000000000101F7 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART56_REGISTER
Address	00000000000101F8 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART57_REGISTER
Address	00000000000101F9 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART58_REGISTER
Address	00000000000101FA (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART59_REGISTER
Address	00000000000101FB (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART60_REGISTER
Address	00000000000101FC (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART61_REGISTER
Address	00000000000101FD (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART62_REGISTER
Address	00000000000101FE (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#7.OTPROM.ECID_PART63_REGISTER
Address	00000000000101FF (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART0_REGISTER
Address	0000000000010200 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART1_REGISTER
Address	0000000000010201 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART2_REGISTER
Address	0000000000010202 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART3_REGISTER
Address	0000000000010203 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART4_REGISTER
Address	0000000000010204 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART5_REGISTER
Address	0000000000010205 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART6_REGISTER
Address	0000000000010206 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART7_REGISTER
Address	0000000000010207 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART8_REGISTER
Address	0000000000010208 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART9_REGISTER
Address	0000000000010209 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART10_REGISTER
Address	000000000001020A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART11_REGISTER
Address	000000000001020B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART12_REGISTER
Address	000000000001020C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART13_REGISTER
Address	000000000001020D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART14_REGISTER
Address	000000000001020E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART15_REGISTER
Address	000000000001020F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART16_REGISTER
Address	0000000000010210 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART17_REGISTER
Address	0000000000010211 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART18_REGISTER
Address	0000000000010212 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART19_REGISTER
Address	0000000000010213 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART20_REGISTER
Address	0000000000010214 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART21_REGISTER
Address	0000000000010215 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART22_REGISTER
Address	0000000000010216 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART23_REGISTER
Address	0000000000010217 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART24_REGISTER
Address	0000000000010218 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART25_REGISTER
Address	0000000000010219 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART26_REGISTER
Address	000000000001021A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART27_REGISTER
Address	000000000001021B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART28_REGISTER
Address	000000000001021C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART29_REGISTER
Address	000000000001021D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART30_REGISTER
Address	000000000001021E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART31_REGISTER
Address	000000000001021F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART32_REGISTER
Address	0000000000010220 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART33_REGISTER
Address	0000000000010221 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART34_REGISTER
Address	0000000000010222 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART35_REGISTER
Address	0000000000010223 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART36_REGISTER
Address	0000000000010224 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART37_REGISTER
Address	0000000000010225 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART38_REGISTER
Address	0000000000010226 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART39_REGISTER
Address	0000000000010227 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART40_REGISTER
Address	0000000000010228 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART41_REGISTER
Address	0000000000010229 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART42_REGISTER
Address	000000000001022A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART43_REGISTER
Address	000000000001022B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART44_REGISTER
Address	000000000001022C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART45_REGISTER
Address	000000000001022D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART46_REGISTER
Address	000000000001022E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART47_REGISTER
Address	000000000001022F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART48_REGISTER
Address	0000000000010230 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART49_REGISTER
Address	0000000000010231 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART50_REGISTER
Address	0000000000010232 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART51_REGISTER
Address	0000000000010233 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART52_REGISTER
Address	0000000000010234 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART53_REGISTER
Address	0000000000010235 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART54_REGISTER
Address	0000000000010236 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART55_REGISTER
Address	0000000000010237 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART56_REGISTER
Address	0000000000010238 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART57_REGISTER
Address	0000000000010239 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART58_REGISTER
Address	000000000001023A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART59_REGISTER
Address	000000000001023B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART60_REGISTER
Address	000000000001023C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART61_REGISTER
Address	000000000001023D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART62_REGISTER
Address	000000000001023E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#8.OTPROM.ECID_PART63_REGISTER
Address	000000000001023F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Part 0 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART0_REGISTER
Address	0000000000010240 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name	*Contains Part 1 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART1_REGISTER
Address	0000000000010241 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name	*Contains Part 2 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART2_REGISTER
Address	0000000000010242 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_2: 2 address location

Register Name	*Contains Part 3 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART3_REGISTER
Address	0000000000010243 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_3: 3 address location

Register Name	*Contains Part 4 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART4_REGISTER
Address	0000000000010244 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_4: 4 address location

Register Name	*Contains Part 5 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART5_REGISTER
Address	0000000000010245 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_5: 5 address location

Register Name	*Contains Part 6 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART6_REGISTER
Address	0000000000010246 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_6: 6 address location

Register Name	*Contains Part 7 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART7_REGISTER
Address	0000000000010247 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_7: 7 address location

Register Name	*Contains Part 8 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART8_REGISTER
Address	0000000000010248 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_8: 8 address location

Register Name	*Contains Part 9 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART9_REGISTER
Address	0000000000010249 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_9: 9 address location

Register Name	*Contains Part 10 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART10_REGISTER
Address	000000000001024A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_10: 10 address location

Register Name	*Contains Part 11 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART11_REGISTER
Address	000000000001024B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_11: 11 address location

Register Name	*Contains Part 12 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART12_REGISTER
Address	000000000001024C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name	*Contains Part 13 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART13_REGISTER
Address	000000000001024D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location

Register Name	*Contains Part 14 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART14_REGISTER
Address	000000000001024E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_14: 14 address location

Register Name	*Contains Part 15 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART15_REGISTER
Address	000000000001024F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_15: 15 address location

Register Name	*Contains Part 16 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART16_REGISTER
Address	0000000000010250 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_16: 16 address location

Register Name	*Contains Part 17 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART17_REGISTER
Address	0000000000010251 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_17: 17 address location

Register Name	*Contains Part 18 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART18_REGISTER
Address	0000000000010252 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_18: 18 address location

Register Name	*Contains Part 19 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART19_REGISTER
Address	0000000000010253 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_19: 19 address location

Register Name	*Contains Part 20 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART20_REGISTER
Address	0000000000010254 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_20: 20 address location

Register Name	*Contains Part 21 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART21_REGISTER
Address	0000000000010255 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_21: 21 address location

Register Name	*Contains Part 22 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART22_REGISTER
Address	0000000000010256 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name	*Contains Part 23 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART23_REGISTER
Address	0000000000010257 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name	*Contains Part 24 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART24_REGISTER
Address	0000000000010258 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_24: 24 address location

Register Name	*Contains Part 25 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART25_REGISTER
Address	0000000000010259 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_25: 25 address location

Register Name	*Contains Part 26 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART26_REGISTER
Address	000000000001025A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_26: 26 address location

Register Name	*Contains Part 27 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART27_REGISTER
Address	000000000001025B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_27: 27 address location

Register Name	*Contains Part 28 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART28_REGISTER
Address	000000000001025C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_28: 28 address location

Register Name	*Contains Part 29 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART29_REGISTER
Address	000000000001025D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_29: 29 address location

Register Name	*Contains Part 30 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART30_REGISTER
Address	000000000001025E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_30: 30 address location

Register Name	*Contains Part 31 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART31_REGISTER
Address	000000000001025F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_31: 31 address location

Register Name	*Contains Part 32 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART32_REGISTER
Address	0000000000010260 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_32: 32 address location

Register Name	*Contains Part 33 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART33_REGISTER
Address	0000000000010261 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_33: 33 address location

Register Name	*Contains Part 34 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART34_REGISTER
Address	0000000000010262 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_34: 34 address location

Register Name	*Contains Part 35 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART35_REGISTER
Address	0000000000010263 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_35: 35 address location

Register Name	*Contains Part 36 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART36_REGISTER
Address	0000000000010264 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_36: 36 address location

Register Name	*Contains Part 37 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART37_REGISTER
Address	0000000000010265 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_37: 37 address location

Register Name	*Contains Part 38 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART38_REGISTER
Address	0000000000010266 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_38: 38 address location

Register Name	*Contains Part 39 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART39_REGISTER
Address	0000000000010267 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_39: 39 address location

Register Name	*Contains Part 40 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART40_REGISTER
Address	0000000000010268 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_40: 40 address location

Register Name	*Contains Part 41 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART41_REGISTER
Address	0000000000010269 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_41: 41 address location

Register Name	*Contains Part 42 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART42_REGISTER
Address	000000000001026A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_42: 42 address location

Register Name	*Contains Part 43 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART43_REGISTER
Address	000000000001026B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_43: 43 address location

Register Name	*Contains Part 44 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART44_REGISTER
Address	000000000001026C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_44: 44 address location

Register Name	*Contains Part 45 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART45_REGISTER
Address	000000000001026D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_45: 45 address location

Register Name	*Contains Part 46 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART46_REGISTER
Address	000000000001026E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_46: 46 address location

Register Name	*Contains Part 47 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART47_REGISTER
Address	000000000001026F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_47: 47 address location

Register Name	*Contains Part 48 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART48_REGISTER
Address	0000000000010270 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_48: 48 address location

Register Name	*Contains Part 49 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART49_REGISTER
Address	0000000000010271 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_49: 49 address location

Register Name	*Contains Part 50 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART50_REGISTER
Address	0000000000010272 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_50: 50 address location

Register Name	*Contains Part 51 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART51_REGISTER
Address	0000000000010273 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_51: 51 address location

Register Name	*Contains Part 52 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART52_REGISTER
Address	0000000000010274 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_52: 52 address location

Register Name	*Contains Part 53 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART53_REGISTER
Address	0000000000010275 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_53: 53 address location

Register Name	*Contains Part 54 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART54_REGISTER
Address	0000000000010276 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_54: 54 address location

Register Name	*Contains Part 55 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART55_REGISTER
Address	0000000000010277 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_55: 55 address location

Register Name	*Contains Part 56 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART56_REGISTER
Address	0000000000010278 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_56: 56 address location

Register Name	*Contains Part 57 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART57_REGISTER
Address	0000000000010279 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_57: 57 address location

Register Name	*Contains Part 58 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART58_REGISTER
Address	000000000001027A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_58: 58 address location

Register Name	*Contains Part 59 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART59_REGISTER
Address	000000000001027B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_59: 59 address location

Register Name	*Contains Part 60 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART60_REGISTER
Address	000000000001027C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_60: 60 address location

Register Name	*Contains Part 61 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART61_REGISTER
Address	000000000001027D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_61: 61 address location

Register Name	*Contains Part 62 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART62_REGISTER
Address	000000000001027E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_62: 62 address location

Register Name	*Contains Part 63 Of The eFUSE*
Mnemonic	TPTOP.OTPR.OTPROM_GEN#9.OTPROM.ECID_PART63_REGISTER
Address	000000000001027F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_63: 63 address location

Register Name	*Contains Command To The Repair Loader*
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.RLDLOG.COMMAND_REGISTER
Address	0000000000050000 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:63	RWX	CMD_REG: command register Bit0-2 : Command Type (000 Skip 001 Scan Write) Bit3 : Last Command Indicator Bit4-15 : Start Address of Repair Data or Repair Command in OTP ROM Bit16-31 : Chain Length (max 64K) Bit32 : Shift with setpulse Bit33-63 : Chain Address

Register Name	*Contains Front End Command To The Repair Loader*
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.RLDLOG.FRONTEND_REGISTER
Address	0000000000050001 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:63	ROX	FRONTEND_REG: front end register Bit0-2 : Command Type (000 Skip 001 Scan Write) Bit3 : Last Command Indicator Bit4-15 : Start Address of Repair Data or Repair Command in OTP ROM Bit16-31 : Chain Length (max 64K) Bit32 : Shift with setpulse Bit33-63 : Chain Address

Register Name	*Contains Command Valid To The Repair Loader*
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.RLDLOG.CMDVAL_REGISTER
Address	0000000000050002 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:63	RWX	CMDVAL_REG: Command Valid Register

Register Name	***Contains Status Of The Repair Loader***
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.RLDLOG.STATUS_REGISTER
Address	0000000000050003 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:63	ROX	STATUS_REG: Status Register Bit0 : Busy Bit1 : Reserved Bit2 : Repair Done Bit3 : Command Flag Bit4 : FrontEnd Flag Bit5 : PIB parity Check Bit6 : FSM Error Bit7 : ECC Error Bit8-21 : Current FSM State Bit22-31 : Reserved Bit32-47 : Command Count Bit48-63 : Bit Count

Register Name	***Contains Status Of The Repair Loader ECC***
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.RLDLOG.ECCTRAP_REGISTER
Address	0000000000050004 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	ROX	ECCTRAP_REG: ECC Trap Register Bit0-3 : Number Correctable Error Bit4-7 : Number Uncorrectable Error Bit8 : Reserved Bit9-15 : First Error Syndrome Bit16-17 : Reserved Bit18 : ECC Data Correction Enable Bit19 : Address Checking Enable Bit20-21 : Reserved Bit22-31 : First Error Address

Register Name	***Contains Configuration Of The Repair Loader***
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.RLDLOG.CONFIG_REGISTER
Address	0000000000050005 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:2	RWX	CONFIG_REG: Repair Loader Configuration Register Bit0 : PIB Master Interface Parity Enable Bit1 : PIB Slave Interface Parity Enable Bit2 : Stop on error Bit3 : Reserved Bit4-7 : OTPROM Port Number Bit8-9 : Reserved Bit10-15 : OTPROM Chiplet Number Bit16-19 : Reserved Bit20-23 : Repair Loader Port Number Bit24-31 : Reserved
3	ROX	CONFIG_REG: Repair Loader Configuration Register Bit0 : PIB Master Interface Parity Enable Bit1 : PIB Slave Interface Parity Enable Bit2 : Stop on error Bit3 : Reserved Bit4-7 : OTPROM Port Number Bit8-9 : Reserved Bit10-15 : OTPROM Chiplet Number Bit16-19 : Reserved Bit20-23 : Repair Loader Port Number Bit24-31 : Reserved
4:7	RWX	CONFIG_REG: Repair Loader Configuration Register Bit0 : PIB Master Interface Parity Enable Bit1 : PIB Slave Interface Parity Enable Bit2 : Stop on error Bit3 : Reserved Bit4-7 : OTPROM Port Number Bit8-9 : Reserved Bit10-15 : OTPROM Chiplet Number Bit16-19 : Reserved Bit20-23 : Repair Loader Port Number Bit24-31 : Reserved
8:9	ROX	CONFIG_REG: Repair Loader Configuration Register Bit0 : PIB Master Interface Parity Enable Bit1 : PIB Slave Interface Parity Enable Bit2 : Stop on error Bit3 : Reserved Bit4-7 : OTPROM Port Number Bit8-9 : Reserved Bit10-15 : OTPROM Chiplet Number Bit16-19 : Reserved Bit20-23 : Repair Loader Port Number Bit24-31 : Reserved

Bits	FSI	Field Mnemonic: Description
10:15	RWX	CONFIG_REG: Repair Loader Configuration Register Bit0 : PIB Master Interface Parity Enable Bit1 : PIB Slave Interface Parity Enable Bit2 : Stop on error Bit3 : Reserved Bit4-7 : OTPROM Port Number Bit8-9 : Reserved Bit10-15 : OTPROM Chiplet Number Bit16-19 : Reserved Bit20-23 : Repair Loader Port Number Bit24-31 : Reserved
16:31	ROX	CONFIG_REG: Repair Loader Configuration Register Bit0 : PIB Master Interface Parity Enable Bit1 : PIB Slave Interface Parity Enable Bit2 : Stop on error Bit3 : Reserved Bit4-7 : OTPROM Port Number Bit8-9 : Reserved Bit10-15 : OTPROM Chiplet Number Bit16-19 : Reserved Bit20-23 : Repair Loader Port Number Bit24-31 : Reserved

Register Name	***CONTROl REGISTER_PMC_MODE_0***
Mnemonic	TPTOP.PIB.I2CM.CONTROL_REGISTER_0
Address	00000000000A0000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	PIB_CNTR_REG_BIT_WITHSTART_0: for command register of i2c engine
1	WOX	PIB_CNTR_REG_BIT_WITHADDR_0: for command register of i2c engine
2	WOX	PIB_CNTR_REG_BIT_READCONT_0: for command register of i2c engine
3	WOX	PIB_CNTR_REG_BIT_WITHSTOP_0: for command register of i2c engine
4:7	WOX	PIB_CNTR_REG_LENGTH_0: Maximum_write = 4 , Maximum_read = 8
8:14	WOX	PIB_CNTR_REG_ADDR_0: for command register of i2c engine
15	WOX	PIB_CNTR_REG_BIT_RNW_0: for command register of i2c engine
16:17	WOX	PIB_CNTR_REG_SPEED_0: 00=100K 01=400K 10=3400K 11=50K
18:22	WOX	PIB_CNTR_REG_PORT_NUMBER_0: for mode register of i2c engine
23:25	WOX	REG_ADDR_LEN_0: 00= No register address in FIFO 01= 1 Byte of FIFO's data is Register address 10= 2 Byte of FIFO's data are Register address 11= 3 Byte of FIFO's data are Register address
26	WOX	ENH_MODE_0: Enable enhanced mode in mode register of I2C engine
27:31	WOX	UNUSED_0: reserved not used
32:39	WOX	PIB_CNTR_REG_DATA_1_0: data for i2c FIFO
40:47	WOX	PIB_CNTR_REG_DATA_2_0: data for i2c FIFO
48:55	WOX	PIB_CNTR_REG_DATA_3_0: data for i2c FIFO
56:63	WOX	PIB_CNTR_REG_DATA_4_0: data for i2c FIFO

Register Name	***RESET REGISTER_PMC_MODE***
Mnemonic	TPTOP.PIB.I2CM.RESET_REGISTER_0
Address	00000000000A0001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	overall_reset_0 one bit register resets all registers and I2C ENGINE

Register Name	***STATUS REGISTER_PMC_MODE***
Mnemonic	TPTOP.PIB.I2CM.STATUS_REGISTER_0
Address	00000000000A0002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_0: address invalid
1	ROX	BUS_STATUS_WRITE_NVLD_0: write invalid
2	ROX	BUS_STATUS_READ_NVLD_0: read invalid
3	ROX	BUS_STATUS_ADDR_P_ERR_0: address parity error
4	ROX	BUS_STATUS_PAR_ERR_0: data parity error
5	ROX	BUS_STATUS_LB_PARITY_ERROR_0: local bus parity error
6:13	ROX	PIB_REG_DATA_ACT_0_0: 1st byte of data
14:21	ROX	PIB_REG_DATA_ACT_1_0: 2nd byte of data
22:29	ROX	PIB_REG_DATA_ACT_2_0: 3rd byte of data
30:37	ROX	PIB_REG_DATA_ACT_3_0: 4th byte of data
38:43	RO	constant=0b000000
44	ROX	BUS_STATUS_BUSY_0: local bus busy
45	ROX	BUS_STATUS_INVALID_COMMAND_0: invalid command
46	ROX	BUS_STATUS_PARITY_ERROR_0: parity error
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_0: back end overrun error
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_0: back end access error
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_0: arbitration lost error
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_0: nack received error
51	ROX	BUS_STATUS_DATA_REQUEST_0: data request
52	ROX	BUS_STATUS_COMMAND_COMPLETE_0: command complete
53	ROX	BUS_STATUS_STOP_ERROR_0: stop error
54	ROX	BUS_STATUS_I2C_PORT_BUSY_0: i2c port busy
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_0: i2c interface busy
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_0: fifo entry count

Register Name	***DATA REGISTER_PMC_MODE***
Mnemonic	TPTOP.PIB.I2CM.DATA_REGISTER_0
Address	00000000000A0003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RWX	PIB_REG_DATA_ACT_0_0: 1st byte of data
8:15	RWX	PIB_REG_DATA_ACT_1_0: 2nd byte of data
16:23	RWX	PIB_REG_DATA_ACT_2_0: 3rd byte of data

Bits	PIB	Field Mnemonic: Description
24:31	RWX	PIB_REG_DATA_ACT_3_0: 4th byte of data
32:39	RWX	PIB_REG_DATA_ACT_4_0: 5th byte of data
40:47	RWX	PIB_REG_DATA_ACT_5_0: 6th byte of data
48:55	RWX	PIB_REG_DATA_ACT_6_0: 7th byte of data
56:63	RWX	PIB_REG_DATA_ACT_7_0: 8th byte of data

Register Name	***FIFO1_REGISTER_READ_0***
Mnemonic	TPTOP.PIB.I2CM.FIFO1_REGISTER_READ_0
Address	00000000000A0004 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_0: As FIFO is not a normal register, cannot be completely verified in regchk . So this is a dummy register to maintain address in HTML fifo data byte 0 .Should be able to read/write 1 bytes
8:31	RO	constant=0b000000000000000000000000
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***COMMAND_REGISTER_0***
Mnemonic	TPTOP.PIB.I2CM.COMMAND_REGISTER_0
Address	00000000000A0005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	WITH_START_0: Decides start command to be issued or not during the beginning of the operation Decides start command to be issued or not during the beginning of the operation
1	RWX	WITH_ADDRESS_0: Decides Device address to be send or not during the beginning of the operation Decides Device address to be send or not during the beginning of the operation
2	RWX	READ_CONTINUE_0: Decides Next read operation is continuation of present operation or not Decides Next read operation is continuation of present operation or not
3	RWX	WITH_STOP_0: Decides stop command to be issued or not during the end of the operation Decides stop command to be issued or not during the end of the operation
4:7	RWX	NOT_USED_0: not used not used
8:14	RWX	DEVICE_ADDRESS_0: Device address of Slave on the I2C Bus Device address of Slave on the I2C Bus

Bits	PIB	Field Mnemonic: Description
15	RWX	READ_NOT_WRITE_0: I2C read or write I2C read or write
16:31	RWX	LENGTH_IN_BYTES_0: Length of Bytes to be accessed through the I2C Bus Length of Bytes to be accessed through the I2C Bus
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***MODE_REGISTER_0***
Mnemonic	TPTOP.PIB.I2CM.MODE_REGISTER_0
Address	00000000000A0006 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus Decides the speed on the I2C bus
8:9	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus
10:15	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus port number
16:21	RWX	PORT_NUMBER_0: port number
22:26	RO	constant=0b00000
27	RWX	CHKSW_I2C_BUSY_0: Debug switch to switch b/w port_busy register , i2c_busy muxing logic and without this muxed version means older version
28	RWX	FGAT_MODE_0: fgat mode fgat mode
29	RWX	DIAG_MODE_0: diag mode diag mode
30	RWX	PACING_ALLOW_MODE_0: pacing allow mode pacing allow mode
31	RWX	WRAP_MODE_0: wrap_mode wrap_mode

Bits	PIB	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***WATER_MARK_REGISTER_0***
Mnemonic	TPTOP.PIB.I2CM.WATER_MARK_REGISTER_0
Address	00000000000A0007 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:15	RO	constant=0b0000000000000000
16:31	RWX	WATERMARK_REG_0: water mark register water mark register
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***INTERRUPT_MASK_REGISTER_0***
Mnemonic	TPTOP.PIB.I2CM.INTERRUPT_MASK_REGISTER_0
Address	00000000000A0008 (PIB) 00000000000A0009 (PIB1) 00000000000A000A (PIB2)
Attributes	
Description	

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0:15	RO	RO	RO	constant=0b0000000000000000

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
16:31	WOX	WOX_OR	WOX_AND	INT_MASK_0: interrupt mask register interrupt mask register
32:63	RO	RO	RO	constant=0b00000000000000000000000000000000

Register Name	***INTERRUPT_MASK_REGISTER_read_0***
Mnemonic	TPTOP.PIB.I2CM.INTERRUPT_MASK_REGISTER_READ_0
Address	00000000000A0008 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:15	RO	constant=0b0000000000000000
16:31	ROX	INT_MASK_0: interrupt mask register interrupt mask register
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***INTERRUPT_CONDITION_0***
Mnemonic	TPTOP.PIB.I2CM.INTERRUPT_COND_0
Address	00000000000A0009 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:15	RO	constant=0b0000000000000000 interrupt conditions
16	ROX	INVALID_CMD_0: invalid command : new command given when old command is not yet completed interrupt conditions
17	ROX	LBUS_PARITY_ERROR_0: local bus parity error interrupt conditions
18	ROX	BE_OV_ERROR_0: back end overrun error : Writing/reading into full/empty fifo resply interrupt conditions
19	ROX	BE_ACC_ERROR_0: back end access error : Writing/Reading more data than requested interrupt conditions

Bits	PIB	Field Mnemonic: Description
20	ROX	ARBITRATION_LOST_ERROR_0: arbitration lost error: I2C bus is held by some other master when trying to access interrupt conditions
21	ROX	NACK_RECEIVED_ERROR_0: nack received error: Slave is not responding back with the ACK. interrupt conditions
22	ROX	DATA_REQUEST_0: data request: FIFO needs to be accessed some more times to full fill the expectation interrupt conditions
23	ROX	int_conds_cmd_complete_0 interrupt conditions
24	ROX	STOP_ERROR_0: stop error: Did not able to send the stop condition on the BUS interrupt conditions
25	ROX	int_conds_i2c_busy_0 interrupt conditions
26	ROX	int_conds_not_i2c_busy_0 interrupt conditions
27	RO	constant=0b0 interrupt conditions
28	ROX	int_conds_scl_eq_1_0 interrupt conditions
29	ROX	int_conds_scl_eq_0_0 interrupt conditions
30	ROX	int_conds_sda_eq_1_0 interrupt conditions
31	ROX	int_conds_sda_eq_0_0 interrupt conditions
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***INTERRUPTS_REGISTER_0***
Mnemonic	TPTOP.PIB.I2CM.INTERRUPTS_0
Address	00000000000A000A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:31	ROX	ints_0 interrupts

Bits	PIB	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***IMM_RESET_I2C_0***
Mnemonic	TPTOP.PIB.I2CM.IMM_RESET_I2C_0
Address	00000000000A000B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_reset_i2c_0 resets command,mode,watermark,interrupt mask,status registers

Register Name	***STATUS_REGISTER_ENGINE_0***
Mnemonic	TPTOP.PIB.I2CM.STATUS_REGISTER_ENGINE_0
Address	00000000000A000B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	INVALID_CMD_0: invalid command : new command given when old command is not yet completed invalid command : new command given when old command is not yet completed
1	ROX	LBUS_PARITY_ERROR_0: local bus parity error local bus parity error
2	ROX	BE_OV_ERROR_0: back end overrun error : Writing/reading into full/empty fifo resply back end overrun error
3	ROX	BE_ACC_ERROR_0: back end access error : Writing/Reading more data than requested back end access error
4	ROX	ARBITRATION_LOST_ERROR_0: arbitration lost error: I2C bus is held by some other master when trying to access arbitration lost error
5	ROX	NACK_RECEIVED_ERROR_0: nack received error: Slave is not responding back with the ACK. nack received error
6	ROX	DATA_REQUEST_0: data request: FIFO needs to be accessed some more times to full fill the expectation data request

Bits	PIB	Field Mnemonic: Description
7	ROX	cmd_complete_0 command complete : Indicates the completion of command
8	ROX	STOP_ERROR_0: stop error: Did not able to send the stop condition on the BUS stop error
9:15	ROX	max_num_of_ports_0 maximum number of ports defined for this Engine
16	ROX	any_i2c_int_0 any_i2c_int
17:18	RO	constant=0b00
19	ROX	i2c_port_history_busy_0 i2c_port_history_busy_0
20	ROX	scl_syn_0 scl_syn
21	ROX	sda_syn_0 sda_syn
22	ROX	i2c_busy_0 i2c busy: I2C bus is occupied
23	ROX	SELF_BUSY_0: self busy: I2C bus is occupied by itself self busy: I2C bus is occupied by itself
24:27	RO	constant=0b0000
28:31	ROX	FIFO_ENTRY_COUNT_0: fifo_entry count : Number of bytes present in the FIFO fifo_entry count : Number of bytes present in the FIFO
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***EXTENDED_STATUS_0***
Mnemonic	TPTOP.PIB.I2CM.EXTENDED_STATUS_0
Address	00000000000A000C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	ROX	fifo_size_0 total fifo size
8:10	RO	constant=0b000
11:15	ROX	MSM_CURR_STATE_0: current state current state

Bits	PIB	Field Mnemonic: Description
16	ROX	scl_syn_ext_0 scl_syn
17	ROX	sda_syn_ext_0 sda_syn
18	ROX	s_scl_0 s_scl : clock input for wrap mode
19	ROX	s_sda_0 s_sda : Data input for wrap mode
20	ROX	m_scl_0 m_scl : clock output for wrap mode
21	ROX	m_sda_0 m_sda : data output for wrap mode
22	ROX	high_water_0 high water mark : FIFO reached highest water level
23	ROX	low_water_0 low water mark : FIFO reached lowest water level
24	ROX	i2c_busy_ext_0 i2c busy : I2C bus is busy
25	ROX	SELF_BUSY_0: self busy: I2C bus is occupied by itself self busy : I2C bus is held busy by itself
26:31	RO	constant=0b010111
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***IMM_RESET_ERR_0***
Mnemonic	TPTOP.PIB.I2CM.IMM_RESET_ERR_0
Address	00000000000A000C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_reset_errors_0 resets fifo ,some status bits and state machine

Register Name	***IMM_SET_S_SCL_0***
Mnemonic	TPTOP.PIB.I2CM.IMM_SET_S_SCL_0
Address	00000000000A000D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_set_s_scl_0 sets output s_scl

Register Name	***RESIDUAL_FRONT_END_BACK_END_LENGTH_0***
Mnemonic	TPTOP.PIB.I2CM.RESIDUAL_FRONT_END_BACK_END_LENGTH_0
Address	00000000000A000D (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:15	ROX	RESID_FE_LEN_0: residual front end length register residual front end length register
16:31	ROX	resid_be_len_0 residual back end length register
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***I2C_BUSY_REGISTER_0***
Mnemonic	TPTOP.PIB.I2CM.I2C_BUSY_REGISTER_0
Address	00000000000A000E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:31	ROX	port_busy_0 corresponding port is busy if it is '1' no one should access . If '0' can be accessed

Bits	PIB	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***IMM_RESET_S_SCL_0***
Mnemonic	TPTOP.PIB.I2CM.IMM_RESET_S_SCL_0
Address	00000000000A000F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_reset_s_scl_0 resets output s_scl

Register Name	***IMM_SET_S_SDA_0***
Mnemonic	TPTOP.PIB.I2CM.IMM_SET_S_SDA_0
Address	00000000000A0010 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_set_s_sda_0 sets output s_sda

Register Name	***IMM_RESET_S_SDA_0***
Mnemonic	TPTOP.PIB.I2CM.IMM_RESET_S_SDA_0
Address	00000000000A0011 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_reset_s_sda_0 resets output s_sda

Register Name	***FIFO4_REGISTER_READ_0***
Mnemonic	TPTOP.PIB.I2CM.FIFO4_REGISTER_READ_0
Address	00000000000A0012 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	ROX	FIFO_BITS_READ0_0: As FIFO is not a normal register, cannot be completely verified in regchk . So this is a dummy register to maintain address in HTML fifo data byte 0 .Should be able to read/write 1 bytes
8:15	ROX	Reserved field. (Access type is fifo_bits_read2_0)
16:23	ROX	Reserved field. (Access type is fifo_bits_read3_0)
24:31	ROX	Reserved field. (Access type is fifo_bits_read4_0)
32:39	ROX	PEEK_DATA1_0: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state
40	ROX	LBUS_PARITY_ERR1_0: local bus parity error from the local bus to glue logic
41:63	RO	constant=0b00000000000000000000000

Register Name	***Number Of Slaves In Multicast Group 0***
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_0_SLAVES_REG
Address	00000000000F0000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_0: Number of slaves in multicast group 0

Register Name	***Number Of Slaves In Multicast Group 1***
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_1_SLAVES_REG
Address	00000000000F0001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_1: Number of slaves in multicast group 1

Register Name	*Number Of Slaves In Multicast Group 2*
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_2_SLAVES_REG
Address	00000000000F0002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_2: Number of slaves in multicast group 2

Register Name	*Number Of Slaves In Multicast Group 3*
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_3_SLAVES_REG
Address	00000000000F0003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_3: Number of slaves in multicast group 3

Register Name	*Number Of Slaves In Multicast Group 4*
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_4_SLAVES_REG
Address	00000000000F0004 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_4: Number of slaves in multicast group 4

Register Name	*Number Of Slaves In Multicast Group 5*
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_5_SLAVES_REG
Address	00000000000F0005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_5: Number of slaves in multicast group 5

Register Name	***Number Of Slaves In Multicast Group 6***
Mnemonic	TPTOP.PIB.PCBMS.MCAST_GRP_6_SLAVES_REG
Address	00000000000F0006 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_6: Number of slaves in multicast group 6

Register Name	***Selects Bit To Be Returned By Multicast Read***
Mnemonic	TPTOP.PIB.PCBMS.BIT_SEL_REG_2
Address	00000000000F0008 (PIB_FSP)
Attributes	
Description	

Bits	PIB_FSP	Field Mnemonic: Description
0:5	RW	BIT_SELECT_REGISTER_FSP2PIB: Selects bit to be returned by multicast read register is per PIB master although same address

Register Name	***Selects Bit To Be Returned By Multicast Read***
Mnemonic	TPTOP.PIB.PCBMS.BIT_SEL_REG_3
Address	00000000000F0008 (PIB_FSI)
Attributes	
Description	

Bits	PIB_FSI	Field Mnemonic: Description
0:5	RW	BIT_SELECT_REGISTER_FSISHIFT: Selects bit to be returned by multicast read register is per PIB master although same address

Register Name	***Chip-ID Readout***
Mnemonic	TPTOP.PIB.PCBMS.DEVICE_ID_REG
Address	00000000000F000F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:19	RO	cfam_chipid Cfam ChipID
20:31	RO	constant=0b000001001001
32:33	RO	module_id ModuleID
34:39	RO	
40:45	RO	constant=0b000000

Register Name	*Register Containing The Information On What Slave Responded During A Multicast Access*
Mnemonic	TPTOP.PIB.PCBMS.REC_ACK_REG
Address	00000000000F0010 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RWX_WCLRREG	RECEIVE_ACKNOWLEDGE_REGISTER: Register containing the information on what slave responded during a multicast access

Register Name	*Register Containing The Information On What Slave Responded With An Error During A Multicast Access*
Mnemonic	TPTOP.PIB.PCBMS.REC_ERR_REG0
Address	00000000000F0011 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	MASTER_RESPONSE_BIT: Bit indicating that PCBMS has responded
1:3	RWX_WAND	MASTER_ERROR_CODE: Master error code
4	ROX	SLAVE1_RESPONSE_BIT: Bit indicating that Slave1 has responded
5:7	RWX_WAND	SLAVE1_ERROR_CODE: Slave1 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
8	ROX	SLAVE2_RESPONSE_BIT: Bit indicating that Slave2 has responded
9:11	RWX_WAND	SLAVE2_ERROR_CODE: Slave2 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
12	ROX	SLAVE3_RESPONSE_BIT: Bit indicating that Slave3 has responded
13:15	RWX_WAND	SLAVE3_ERROR_CODE: Slave3 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
16	ROX	SLAVE4_RESPONSE_BIT: Bit indicating that Slave4 has responded
17:19	RWX_WAND	SLAVE4_ERROR_CODE: Slave4 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
20	ROX	SLAVE5_RESPONSE_BIT: Bit indicating that Slave5 has responded
21:23	RWX_WAND	SLAVE5_ERROR_CODE: Slave5 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
24	ROX	SLAVE6_RESPONSE_BIT: Bit indicating that Slave6 has responded
25:27	RWX_WAND	SLAVE6_ERROR_CODE: Slave6 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
28	ROX	SLAVE7_RESPONSE_BIT: Bit indicating that Slave7 has responded
29:31	RWX_WAND	SLAVE7_ERROR_CODE: Slave7 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
32	ROX	SLAVE8_RESPONSE_BIT: Bit indicating that Slave8 has responded
33:35	RWX_WAND	SLAVE8_ERROR_CODE: Slave8 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout

Bits	PIB	Field Mnemonic: Description
36	ROX	SLAVE9_RESPONSE_BIT: Bit indicating that Slave9 has responded
37:39	RWX_WAND	SLAVE9_ERROR_CODE: Slave9 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
40	ROX	SLAVE10_RESPONSE_BIT: Bit indicating that Slave10 has responded
41:43	RWX_WAND	SLAVE10_ERROR_CODE: Slave10 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
44	ROX	SLAVE11_RESPONSE_BIT: Bit indicating that Slave11 has responded
45:47	RWX_WAND	SLAVE11_ERROR_CODE: Slave11 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
48	ROX	SLAVE12_RESPONSE_BIT: Bit indicating that Slave12 has responded
49:51	RWX_WAND	SLAVE12_ERROR_CODE: Slave12 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
52	ROX	SLAVE13_RESPONSE_BIT: Bit indicating that Slave13 has responded
53:55	RWX_WAND	SLAVE13_ERROR_CODE: Slave13 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
56	ROX	SLAVE14_RESPONSE_BIT: Bit indicating that Slave14 has responded
57:59	RWX_WAND	SLAVE14_ERROR_CODE: Slave14 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
60	ROX	SLAVE15_RESPONSE_BIT: Bit indicating that Slave15 has responded
61:63	RWX_WAND	SLAVE15_ERROR_CODE: Slave15 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout

Register Name	***Register Containing The Information On What Slave Responded With An Error During A Multicast Access***
Mnemonic	TPTOP.PIB.PCBMS.REC_ERR_REG1
Address	00000000000F0012 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	SLAVE16_RESPONSE_BIT: Bit indicating that Slave16 has responded
1:3	RWX_WAND	SLAVE16_ERROR_CODE: Slave16 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
4	ROX	SLAVE17_RESPONSE_BIT: Bit indicating that Slave17 has responded
5:7	RWX_WAND	SLAVE17_ERROR_CODE: Slave17 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
8	ROX	SLAVE18_RESPONSE_BIT: Bit indicating that Slave18 has responded
9:11	RWX_WAND	SLAVE18_ERROR_CODE: Slave18 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
12	ROX	SLAVE19_RESPONSE_BIT: Bit indicating that Slave19 has responded
13:15	RWX_WAND	SLAVE19_ERROR_CODE: Slave19 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
16	ROX	SLAVE20_RESPONSE_BIT: Bit indicating that Slave20 has responded
17:19	RWX_WAND	SLAVE20_ERROR_CODE: Slave20 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
20	ROX	SLAVE21_RESPONSE_BIT: Bit indicating that Slave21 has responded

Bits	PIB	Field Mnemonic: Description
21:23	RWX_WAND	SLAVE21_ERROR_CODE: Slave21 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
24	ROX	SLAVE22_RESPONSE_BIT: Bit indicating that Slave22 has responded
25:27	RWX_WAND	SLAVE22_ERROR_CODE: Slave22 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
28	ROX	SLAVE23_RESPONSE_BIT: Bit indicating that Slave23 has responded
29:31	RWX_WAND	SLAVE23_ERROR_CODE: Slave23 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
32	ROX	SLAVE24_RESPONSE_BIT: Bit indicating that Slave24 has responded
33:35	RWX_WAND	SLAVE24_ERROR_CODE: Slave24 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
36	ROX	SLAVE25_RESPONSE_BIT: Bit indicating that Slave25 has responded
37:39	RWX_WAND	SLAVE25_ERROR_CODE: Slave25 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
40	ROX	SLAVE26_RESPONSE_BIT: Bit indicating that Slave26 has responded
41:43	RWX_WAND	SLAVE26_ERROR_CODE: Slave26 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
44	ROX	SLAVE27_RESPONSE_BIT: Bit indicating that Slave27 has responded
45:47	RWX_WAND	SLAVE27_ERROR_CODE: Slave27 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
48	ROX	SLAVE28_RESPONSE_BIT: Bit indicating that Slave28 has responded
49:51	RWX_WAND	SLAVE28_ERROR_CODE: Slave28 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
52	ROX	SLAVE29_RESPONSE_BIT: Bit indicating that Slave29 has responded
53:55	RWX_WAND	SLAVE29_ERROR_CODE: Slave29 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
56	ROX	SLAVE30_RESPONSE_BIT: Bit indicating that Slave30 has responded
57:59	RWX_WAND	SLAVE30_ERROR_CODE: Slave30 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout
60	ROX	SLAVE31_RESPONSE_BIT: Bit indicating that Slave31 has responded
61:63	RWX_WAND	SLAVE31_ERROR_CODE: Slave31 error code, for example, 000: OK, 010: chiplet offline, 100: invalid address, 110: parity error / unexpected/wrong packet, 111: timeout

Register Name	***Mode Select For Multicast Compare***
Mnemonic	TPTOP.PIB.PCBMS.MCAST_COMP_REG
Address	00000000000F0015 (PIB)
Attributes	
Description	00: =, 01: <, 10: !=, 11: >=

Bits	PIB	Field Mnemonic: Description
0:1	RW	MULTICAST_COMPARE_REGISTER: Mode select for multicast compare. 00: =, 01: <, 10: !=, 11: >=

Register Name	*Value To Compare Against During Multicast Compare Operation*
Mnemonic	TPTOP.PIB.PCBMS.MCAST_COMP_VAL_REG
Address	00000000000F0016 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	MULTICAST_COMPARE_VALUE_REGISTER: Value to compare against during multicast compare operation Is not replicated per master, only a single copy.

Register Name	*Mask Value To Be Used During Multicast Compare*
Mnemonic	TPTOP.PIB.PCBMS.MCAST_COMP_MASK_REG
Address	00000000000F0017 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	MULTICAST_COMPARE_MASK_REGISTER: Mask value to be used during multicast compare

Register Name	*Contains Slave Address Of First Reply Packet*
Mnemonic	TPTOP.PIB.PCBMS.FIRST_REPLY_REG
Address	00000000000F0018 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	ROX	FIRST_REPLY_REGISTER: Contains slave address of first reply packet

Register Name	*Contains Timeout Value For PCB Master*
Mnemonic	TPTOP.PIB.PCBMS.TIMEOUT_REG
Address	00000000000F0019 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RW	TIMEOUT_REGISTER: Contains timeout value for PCB master

Register Name	*Interrupt Register For Special Attention, Checkstop, Recoverable Error*
Mnemonic	TPTOP.PIB.PCBMS.INTERRUPT_TYPE_REG
Address	00000000000F001A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX_WAND	ATTENTION: Attention
1	RWX_WAND	RECOVERABLE_ERROR: Recoverable error
2	RWX_WAND	CHECKSTOP: Checkstop

Register Name	*Ignore Parity Register*
Mnemonic	TPTOP.PIB.PCBMS.IGNORE_PAR_REG
Address	00000000000F001C (PIB)
Attributes	
Description	If set to 1, accesses to the PCB master get forwarded to PCB, also all interrupts are forwarded to the interrupt controller. If set to 0, accesses with parity error to the PCB master do not get forwarded to the PCB, interrupt packets with parity error do not get forwarded to the interrupt controller.

Bits	PIB	Field Mnemonic: Description
0	RW	IGNORE_PARITY_REG: Set to 0 to block accesses with parity errors from PCB, also to ignore interrupt packets with parity error.
1	RW	DISABLE_ECC_CORRECTION: If set, the ECC error correction feature is off.
2	RWX_WCLRPART	ECC_S_BIT_ERROR: Set by HW on single-bit ECC error. Cleared on writing

Register Name	*Reset Register*
Mnemonic	TPTOP.PIB.PCBMS.RESET_REG
Address	00000000000F001D (PIB)
Attributes	
Description	Bit 0 resets all PCB elements outside of the standby domain, Bit 1 resets all endpoints.

Bits	PIB	Field Mnemonic: Description
0	RW	RESET_PCB: Reset all PCB elements outside of the standby domain
1	RW	RESET_ENDPOINTS: Unused: Reset all endpoints attached to the PCB. Bit now in FSI Domain.
2	RW	TIMEOUT_RESET_EN: Enable for auto-reset PCB on PCB-timeout

Register Name	*PCB Master Error Register, Contains First Error*
Mnemonic	TPTOP.PIB.PCBMS.FIRST_ERR_REG
Address	00000000000F001E (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX_WCLRREG	FIRST_TIMEOUT_ACTIVE: Active when master ran into timeout
1	RWX_WCLRREG	FIRST_PARITY_ERR: Parity error on internal FSMs
2	RWX_WCLRREG	FIRST_BEAT_NUM_ERR: Beat with wrong beat number received
3	RWX_WCLRREG	FIRST_BEAT_REC_ERR: Unexpected beat received
4	RWX_WCLRREG	FIRST_RECEIVED_ERROR: Error packet received
5	RWX_WCLRREG	FIRST_RX_PCB_DATA_P_ERR: Data parity on incoming packet
6	RWX_WCLRREG	FIRST_PIB_ADDR_P_ERR: Parity error on PIB address
7	RWX_WCLRREG	FIRST_PIB_DATA_P_ERR: Parity error on PIB data

Register Name	*Internal PCB Master Error Register*
Mnemonic	TPTOP.PIB.PCBMS.ERROR_REG
Address	00000000000F001F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX_WCLRREG	TIMEOUT_ACTIVE: Active when master ran into timeout
1	RWX_WCLRREG	PARITY_ERR: Parity error on internal FSMs
2	RWX_WCLRREG	BEAT_NUM_ERR: Beat with wrong beat number received
3	RWX_WCLRREG	BEAT_REC_ERR: Unexpected beat received
4	RWX_WCLRREG	RECEIVED_ERROR: Error packet received
5	RWX_WCLRREG	RX_PCB_DATA_P_ERR: Data parity on incoming packet
6	RWX_WCLRREG	PIB_ADDR_P_ERR: Parity error on PIB address
7	RWX_WCLRREG	PIB_DATA_P_ERR: Parity error on PIB data

Register Name	*PIB Extended Error Register 0*
Mnemonic	MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_0
Address	00000000000FFFA0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	*PIB Extended Error Register 1*
Mnemonic	MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_1
Address	00000000000FFFA1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	*PIB Extended Error Register 2*
Mnemonic	MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_2
Address	00000000000FFFA2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	*PIB Extended Error Register 3*
Mnemonic	MBU.MBS.IBB.PIBMST.PIB_EXTENDED_ERROR_REGISTER_3
Address	00000000000FFFA3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

Register Name	*PIB Extended Error Register 0*
Mnemonic	SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_0
Address	00000000000FFFB0 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	*PIB Extended Error Register 1*
Mnemonic	SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_1
Address	00000000000FFFB1 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	*PIB Extended Error Register 2*
Mnemonic	SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_2
Address	00000000000FFFB2 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	*PIB Extended Error Register 3*
Mnemonic	SCAC.SCAC.PIBMST.PIB_EXTENDED_ERROR_REGISTER_3
Address	00000000000FFFB3 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

Register Name	*PIB Extended Error Register 0*
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.PIBMST.PIB_EXTENDED_ERROR_REGISTER_0
Address	000000000014FF00 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	***PIB Extended Error Register 1***
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.PIBMST.PIB_EXTENDED_ERROR_REGISTER_1
Address	000000000014FF01 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	***PIB Extended Error Register 2***
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.PIBMST.PIB_EXTENDED_ERROR_REGISTER_2
Address	000000000014FF02 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	***PIB Extended Error Register 3***
Mnemonic	TPTOP.PIB.RLD.RLDCOMP.PIBMST.PIB_EXTENDED_ERROR_REGISTER_3
Address	000000000014FF03 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

Register Name	***PIB Extended Error Register 0***
Mnemonic	VI.FSI.FSI2PIB2.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_0
Address	00000000001EFF00 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Bits	PIB	Field Mnemonic: Description
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	***PIB Extended Error Register 1***
Mnemonic	VI.FSI.FSI2PIB2.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_1
Address	00000000001EFF01 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	***PIB Extended Error Register 2***
Mnemonic	VI.FSI.FSI2PIB2.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_2
Address	00000000001EFF02 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	***PIB Extended Error Register 3***
Mnemonic	VI.FSI.FSI2PIB2.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_3
Address	00000000001EFF03 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

Register Name	*PIB Extended Error Register 0*
Mnemonic	VI.FSI.FSI2PIB.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_0
Address	00000000001EFF20 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	*PIB Extended Error Register 1*
Mnemonic	VI.FSI.FSI2PIB.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_1
Address	00000000001EFF21 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	*PIB Extended Error Register 2*
Mnemonic	VI.FSI.FSI2PIB.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_2
Address	00000000001EFF22 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	*PIB Extended Error Register 3*
Mnemonic	VI.FSI.FSI2PIB.COMP.CORE.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_3
Address	00000000001EFF23 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

Register Name	*PIB Extended Error Register 0*
Mnemonic	VI.FSI.FSI_SHIFT.COMP.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_0
Address	00000000001EFF30 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	*PIB Extended Error Register 1*
Mnemonic	VI.FSI.FSI_SHIFT.COMP.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_1
Address	00000000001EFF31 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	*PIB Extended Error Register 2*
Mnemonic	VI.FSI.FSI_SHIFT.COMP.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_2
Address	00000000001EFF32 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	*PIB Extended Error Register 3*
Mnemonic	VI.FSI.FSI_SHIFT.COMP.PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_3
Address	00000000001EFF33 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

2. PCB Slave 1: TP Chiplet

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
TPTOP.NET.PCBSLPERV.ASSIST_INTERRUPT_REG	0x00000000010F0011	428
TPTOP.NET.PCBSLPERV.ATOMIC_LOCK_REG	0x00000000010F03FF	435
TPTOP.NET.PCBSLPERV.ATTN_INTERRUPT_REG	0x00000000010F001A	430
TPTOP.NET.PCBSLPERV.CLK_ADJ_REG	0x00000000010F0015	429
TPTOP.NET.PCBSLPERV.CLK_ADJ_SET	0x00000000010F0016	429
TPTOP.NET.PCBSLPERV.ERROR_REG	0x00000000010F001F	431
TPTOP.NET.PCBSLPERV.GP3_REG	0x00000000010F0012	428
TPTOP.NET.PCBSLPERV.HANG_PULSE_0_REG	0x00000000010F0020	433
TPTOP.NET.PCBSLPERV.HANG_PULSE_1_REG	0x00000000010F0021	433
TPTOP.NET.PCBSLPERV.HANG_PULSE_2_REG	0x00000000010F0022	433
TPTOP.NET.PCBSLPERV.HANG_PULSE_3_REG	0x00000000010F0023	433
TPTOP.NET.PCBSLPERV.HANG_PULSE_4_REG	0x00000000010F0024	434
TPTOP.NET.PCBSLPERV.HANG_PULSE_5_REG	0x00000000010F0025	434
TPTOP.NET.PCBSLPERV.HANG_PULSE_6_REG	0x00000000010F0026	434
TPTOP.NET.PCBSLPERV.HEARTBEAT_REG	0x00000000010F0018	430
TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_1	0x00000000010F0001	427
TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_2	0x00000000010F0002	427
TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_3	0x00000000010F0003	427
TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_4	0x00000000010F0004	428
TPTOP.NET.PCBSLPERV.PLL_LOCK_REG	0x00000000010F0019	430
TPTOP.NET.PCBSLPERV.PRE_COUNTER_REG	0x00000000010F0028	434
TPTOP.NET.PCBSLPERV.PRIMARY_ADDRESS_REG	0x00000000010F0000	427
TPTOP.NET.PCBSLPERV.PROTECT_MODE_REG	0x00000000010F03FE	435
TPTOP.NET.PCBSLPERV.RECOV_INTERRUPT_REG	0x00000000010F001B	431
TPTOP.NET.PCBSLPERV.SLAVE_CONFIG_REG	0x00000000010F001E	431
TPTOP.NET.PCBSLPERV.TIMEOUT_REG	0x00000000010F0010	428
TPTOP.NET.PCBSLPERV.VITAL_SCAN_OUT	0x00000000010F0017	430
TPTOP.NET.PCBSLPERV.XSTOP_INTERRUPT_REG	0x00000000010F001C	431
TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_0	0x00000000010FFF00	435
TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_1	0x00000000010FFF01	436
TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_2	0x00000000010FFF02	436
TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_3	0x00000000010FFF03	436
TPTOP.TPC.CC_ATOMIC_LOCK_REG	0x00000000010303FF	416
TPTOP.TPC.CC_PROTECT_MODE_REG	0x00000000010303FE	416
TPTOP.TPC.CLK_REGION	0x0000000001030006	413
TPTOP.TPC.CLOCK_STAT	0x0000000001030008	414
TPTOP.TPC.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000001040010	419
TPTOP.TPC.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000001040011	420
TPTOP.TPC.EPS.FIR.LOCAL_FIR_MASK	0x000000000104000D	419
TPTOP.TPC.EPS.FIR.MODE_REG	0x0000000001040008	418
TPTOP.TPC.EPS.FIR.SPATTN	0x0000000001040004	417
TPTOP.TPC.EPS.FIR.SPA_MASK	0x0000000001040007	418

Mnemonic	Address	Page
TPTOP.TPC.EPS.PSC.ADDR_TRAP_REG	0x0000000001010003	403
TPTOP.TPC.EPS.PSC.ATOMIC_LOCK_REG	0x00000000010103FF	404
TPTOP.TPC.EPS.PSC.DEBUG_STATUS_REG	0x0000000001010004	403
TPTOP.TPC.EPS.PSC.PSCOM_ERROR_MASK	0x0000000001010002	402
TPTOP.TPC.EPS.PSC.PSCOM_MODE_REG	0x0000000001010000	400
TPTOP.TPC.EPS.PSC.PSCOM_STATUS_ERROR_REG	0x0000000001010001	401
TPTOP.TPC.EPS.PSC.PSCOM_WRITE_PROTECT_REG	0x0000000001010005	404
TPTOP.TPC.EPS.THERM.CONTROL_REG	0x0000000001050012	423
TPTOP.TPC.EPS.THERM.DTS_RESULT0	0x0000000001050000	420
TPTOP.TPC.EPS.THERM.DTS_TRC_RESULT	0x0000000001050003	420
TPTOP.TPC.EPS.THERM.ENC_CPM_RESULT0	0x0000000001050008	420
TPTOP.TPC.EPS.THERM.ERR_STATUS_REG	0x0000000001050013	423
TPTOP.TPC.EPS.THERM.INJECT_REG	0x0000000001050011	423
TPTOP.TPC.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000001050016	425
TPTOP.TPC.EPS.THERM.SKITTER_DATA0	0x0000000001050019	426
TPTOP.TPC.EPS.THERM.SKITTER_DATA1	0x000000000105001A	426
TPTOP.TPC.EPS.THERM.SKITTER_DATA2	0x000000000105001B	426
TPTOP.TPC.EPS.THERM.SKITTER_FORCE_REG	0x0000000001050014	425
TPTOP.TPC.EPS.THERM.SKITTER_MODE_REG	0x0000000001050010	422
TPTOP.TPC.EPS.THERM.THERM_MODE_REG	0x000000000105000F	421
TPTOP.TPC.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000105001C	426
TPTOP.TPC.EPS.THERM.VOLT_MODE_REG	0x0000000001050015	425
TPTOP.TPC.EPS.THERM.VOLT_READ0	0x000000000105000B	421
TPTOP.TPC.ERROR_STATUS	0x0000000001030009	415
TPTOP.TPC.FIR_MASK	0x0000000001040002	417
TPTOP.TPC.GP0	0x0000000001000000	396
TPTOP.TPC.GP1	0x0000000001000001	398
TPTOP.TPC.GP2	0x0000000001000002	398
TPTOP.TPC.GP4	0x0000000001000003	399
TPTOP.TPC.GPIO_ATOMIC_LOCK_REG	0x00000000010003FF	400
TPTOP.TPC.GPIO_PROTECT_MODE_REG	0x00000000010003FE	400
TPTOP.TPC.ITR.COMP.INTERRUPT1_REG	0x0000000001020000	405
TPTOP.TPC.ITR.COMP.INTERRUPT2_REG	0x0000000001020003	405
TPTOP.TPC.ITR.COMP.INTERRUPT3_REG	0x0000000001020006	405
TPTOP.TPC.ITR.COMP.INTERRUPT4_REG	0x0000000001020009	406
TPTOP.TPC.ITR.COMP.INTERRUPT_CONF_REG	0x000000000102000F	406
TPTOP.TPC.ITR.COMP.INTERRUPT_HOLD_REG	0x0000000001020012	407
TPTOP.TPC.ITR.COMP.INTERRUPT_TYPE_MASK_REG	0x000000000102000C	406
TPTOP.TPC.ITR.FMU.FMU_FORCE_OP_REG	0x000000000102002B	410
TPTOP.TPC.ITR.FMU.FMU_MODE_REG	0x0000000001020028	408
TPTOP.TPC.ITR.FMU.FMU_OSC_CNTR1_REG	0x0000000001020029	409
TPTOP.TPC.ITR.FMU.FMU_OSC_CNTR2_REG	0x000000000102002A	409
TPTOP.TPC.ITR.FMU.FMU_PULSE_GEN_REG	0x0000000001020029	409
TPTOP.TPC.ITR.MISC.ERROR_STATUS_REG	0x0000000001020014	407
TPTOP.TPC.ITR.MISC.IPOLL_MASK_REG	0x0000000001020013	407
TPTOP.TPC.ITR.OSCERR.OSCERR_HOLD	0x0000000001020019	408
TPTOP.TPC.ITR.OSCERR.OSCERR_MASK	0x000000000102001A	408
TPTOP.TPC.ITR.OSCERR.OSCERR_MCODE	0x000000000102001B	408
TPTOP.TPC.LOCAL_FIR	0x000000000104000A	418
TPTOP.TPC.OPCG_REG0	0x0000000001030002	411
TPTOP.TPC.OPCG_REG1	0x0000000001030003	411

Mnemonic	Address	Page
TPTOP.TPC.OPCG_REG2	0x0000000001030004	412
TPTOP.TPC.OPCG_REG3	0x0000000001030005	412
TPTOP.TPC.PHASE_SHADOW	0x0000000001030001	411
TPTOP.TPC.RFIR	0x0000000001040001	417
TPTOP.TPC.SCANSELQ	0x0000000001030007	413
TPTOP.TPC.SYNC_CONFIG	0x0000000001030000	410
TPTOP.TPC.TRA.PERVTRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000001010440	404
TPTOP.TPC.TRA.PERVTRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000001010441	404
TPTOP.TPC.XFIR	0x0000000001040000	416

The memory buffer registers are listed in the following tables.

Register Name	***GP Register 0***
Mnemonic	TPTOP.TPC.GP0
Address	0000000001000000 (PCB) 0000000001000004 (PCB1) 0000000001000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: not used, Reset (0b0)
1	RWX	WOX_AND	WOX_OR	NOT_USED1: not used, Reset (0b1)
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC_OUT: Prevent plats from going into flush mode (init value 1), Reset (0b1)
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (init value 1, drop before dropping flushmode_inh), Reset (0b1)
4	RWX	WOX_AND	WOX_OR	TC_GPIO_AVP_MODE_DC_OUT: Enable AVP mode, Reset (0b0)
5	RWX	WOX_AND	WOX_OR	NOT_USED3: not used, Reset (0b0)
6	RWX	WOX_AND	WOX_OR	TC_GPIO_CC_SCAN_DIS_DC_B_OUT: Disable scan - set output of scan chain to zero, Reset (0b0)
7	RWX	WOX_AND	WOX_OR	NOT_USED2: not used, Reset (0b0)
8	RWX	WOX_AND	WOX_OR	TC_GPIO_LBIST_EN_DC_OUT: LBIST mode, Reset (0b0)
9	RWX	WOX_AND	WOX_OR	TC_UNIT_LBIST_AC_MODE_DC: LBIST AC mode, Reset (0b0)
10	RWX	WOX_AND	WOX_OR	TC_UNIT_LBIST_ARY_WRT_THRU_DC: Array write-through mode - set Array in bypass mode, Reset (0b0)
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST, Reset (0b0)
12	RWX	WOX_AND	WOX_OR	TC_GPIO_ABIST_START_TEST_DC_OUT: Set to start ABIST testing, Reset (0b0)
13	RWX	WOX_AND	WOX_OR	NOT_USED4: not used, Reset (0b0)
14	RWX	WOX_AND	WOX_OR	NOT_USED5: not used, Reset (0b0)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
15	RWX	WOX_AND	WOX_OR	TC_GPIO_SCAN_PROTECT_DC_OUT: Scan protection enable (init value 1), Reset (0b1)
16	RWX	WOX_AND	WOX_OR	NOT_USED6: not used, Reset (0b1)
17	RWX	WOX_AND	WOX_OR	NOT_USED7: not used, Reset (0b0)
18	RWX	WOX_AND	WOX_OR	NOT_USED8: not used, Reset (0b0)
19	RWX	WOX_AND	WOX_OR	NOT_USED9: not used, Reset (0b1)
20	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_START: Start trace to debug macros, Reset (0b0)
21	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_STOP: Stop trace to debug macros, Reset (0b0)
22	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_RESET: Reset trace to debug macros, Reset (0b0)
23	RWX	WOX_AND	WOX_OR	TP_PIB_TRACE_MODE_DATA: Enable Data trace mode of PIB, Reset (0b0)
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio, Reset (0b0)
26	RWX	WOX_AND	WOX_OR	NOT_USED10: not used, Reset (0b0)
27	RWX	WOX_AND	WOX_OR	NOT_USED11: not used, Reset (0b0)
28:31	RWX	WOX_AND	WOX_OR	NOT_USED12: not used, Reset (0b0)
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7), Reset (0b0)
40:42	RWX	WOX_AND	WOX_OR	NOT_USED13: not used, Reset (0b0)
43:45	RWX	WOX_AND	WOX_OR	NOT_USED14: not used, Reset (0b0)
46	RWX	WOX_AND	WOX_OR	TC_BSC_WRAPSEL_DC: BSC wrapsel, Reset (0b0)
47	RWX	WOX_AND	WOX_OR	TC_BSC_INTMODE_DC: BSC intmode, Reset (0b0)
48	RWX	WOX_AND	WOX_OR	TC_BSC_INV_DC: BSC inv, Reset (0b0)
49	RWX	WOX_AND	WOX_OR	TC_BSC_EXTMODE_DC: BSC extmode, Reset (0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED15: not used, Reset (0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED16: not used, Reset (0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED17: not used, Reset (0b0)
53	RWX	WOX_AND	WOX_OR	NOT_USED18: not used, Reset (0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED19: not used, Reset (0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED20: not used, Reset (0b0)
56	RWX	WOX_AND	WOX_OR	NOT_USED21: not used, Reset (0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED22: not used, Reset (0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED23: not used, Reset (0b0)
59	RWX	WOX_AND	WOX_OR	NOT_USED24: not used, Reset (0b0)
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: mask for pcb error (access or parity) in CC, Reset (0b0)
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: mask for pcb write while OPCG_IP / scan collision in CC, Reset (0b0)
62	RWX	WOX_AND	WOX_OR	NOT_USED25: not used, Reset (0b1)
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (init value 1), Reset (0b1)

Register Name	*GP Register 1*
Mnemonic	TPTOP.TPC.GP1
Address	0000000001000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	TRA_ABIST_DONE: SRAM ABIST_DONE for 1:1, Reset (0)
1	ROX	NOT_USED26: not used, Reset (0)
2	ROX	NOT_USED27: not used, Reset (0)
3	ROX	NOT_USED28: not used, Reset (0)
4	ROX	NOT_USED29: not used, Reset (0)
5	ROX	NOT_USED30: not used, Reset (0)
6	ROX	NOT_USED31: not used, Reset (0)
7	ROX	NOT_USED32: not used, Reset (0)
8	ROX	NOT_USED33: not used, Reset (0)
9	ROX	NOT_USED34: not used, Reset (0)
10	ROX	NOT_USED35: not used, Reset (0)
11	ROX	NOT_USED36: not used, Reset (0)
12	ROX	NOT_USED37: not used, Reset (0)
13	ROX	NOT_USED38: not used, Reset (0)
14	ROX	NOT_USED39: not used, Reset (0)
15	ROX	TC_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs, Reset (0)
16	ROX	NOT_USED40: not used, Reset (0)
17	ROX	NOT_USED41: not used, Reset (0)
18	ROX	NOT_USED42: not used, Reset (0)
19	ROX	NOT_USED43: not used, Reset (0)
20	ROX	NOT_USED44: not used, Reset (0)
21	ROX	NOT_USED45: not used, Reset (0)
22	ROX	NOT_USED46: not used, Reset (0)
23	ROX	NOT_USED47: not used, Reset (0)

Register Name	*GP Register 2*
Mnemonic	TPTOP.TPC.GP2
Address	0000000001000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking

Register Name	*GP Register 4*
Mnemonic	TPTOP.TPC.GP4
Address	0000000001000003 (PCB) 0000000001000006 (PCB1) 0000000001000007 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select Reset (0b000000)
6:7	RWX	WOX_AND	WOX_OR	NOT_USED48: not used, Reset (0b00)
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select, Reset (0b000000)
14:15	RWX	WOX_AND	WOX_OR	NOT_USED49: not used, Reset (0b00)
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select, Reset (0b000000)
22:23	RWX	WOX_AND	WOX_OR	NOT_USED50: not used, Reset (0b00)
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: tc_probe3_sel_dc(0:5) / tc_ex_amux_sel_dc(0:3), -, Reset (0b000000)
30	RWX	WOX_AND	WOX_OR	NOT_USED51: not used, Reset (0b0)
31	RWX	WOX_AND	WOX_OR	NOT_USED52: not used, Reset (0b0)
32	RWX	WOX_AND	WOX_OR	NOT_USED53: not used, Reset (0b0)
33	RWX	WOX_AND	WOX_OR	NOT_USED54: not used, Reset (0b0)
34	RWX	WOX_AND	WOX_OR	NOT_USED55: not used, Reset (0b1)
35	RWX	WOX_AND	WOX_OR	NOT_USED56: not used, Reset (0b0)
36	RWX	WOX_AND	WOX_OR	NOT_USED57: not used, Reset (0b0)
37	RWX	WOX_AND	WOX_OR	NOT_USED58: not used, Reset (0b0)
38	RWX	WOX_AND	WOX_OR	NOT_USED59: not used, Reset (0b0)
39	RWX	WOX_AND	WOX_OR	NOT_USED60: not used, Reset (0b0)
40	RWX	WOX_AND	WOX_OR	NOT_USED61: not used, Reset (0b1)
41	RWX	WOX_AND	WOX_OR	NOT_USED62: not used, Reset (0b0)
42	RWX	WOX_AND	WOX_OR	NOT_USED63: not used, Reset (0b0)
43	RWX	WOX_AND	WOX_OR	NOT_USED64: not used, Reset (0b0)
44	RWX	WOX_AND	WOX_OR	NOT_USED65: not used, Reset (0b0)
45	RWX	WOX_AND	WOX_OR	NOT_USED66: not used, Reset (0b0)
46	RWX	WOX_AND	WOX_OR	NOT_USED67: not used, Reset (0b1)
47	RWX	WOX_AND	WOX_OR	NOT_USED68: not used, Reset (0b0)
48	RWX	WOX_AND	WOX_OR	NOT_USED69: not used, Reset (0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED70: not used, Reset (0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED71: not used, Reset (0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED72: not used, Reset (0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED73: not used, Reset (0b1)
53	RWX	WOX_AND	WOX_OR	NOT_USED74: not used, Reset (0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED75: not used, Reset (0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED76: not used, Reset (0b0)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
56	RWX	WOX_AND	WOX_OR	NOT_USED77: not used, Reset (0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED78: not used, Reset (0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED79: not used, Reset (0b1)
59	RWX	WOX_AND	WOX_OR	NOT_USED80: not used, Reset (0b0)
60	RWX	WOX_AND	WOX_OR	NOT_USED81: not used, Reset (0b0)
61	RWX	WOX_AND	WOX_OR	NOT_USED82: not used, Reset (0b0)
62	RWX	WOX_AND	WOX_OR	NOT_USED83: not used, Reset (0b0)
63	RWX	WOX_AND	WOX_OR	NOT_USED84: not used, Reset (0b0)

Register Name	***CC Protect Mode Register***
Mnemonic	TPTOP.TPC.GPIO_PROTECT_MODE_REG
Address	00000000010003FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_READ_PROTECT_ENABLE: Enable read protection
1	RW	GPIO_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TPTOP.TPC.GPIO_ATOMIC_LOCK_REG
Address	00000000010003FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	GPIO_ATOMIC_ID: Atomic ID

Register Name	***PSCOMLE Mode Register***
Mnemonic	TPTOP.TPC.EPS.PSC.PSCOM_MODE_REG
Address	0000000001010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: abort_on_PCB_addr_parity_error
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: abort_on_PCB_wdata_parity_error
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: abort_on_DL_return_P0_error
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: abort_on_DL_return_wdata_parity_error

Bits	PCB	Field Mnemonic: Description
4	RW	WATCHDOG_ENABLE: watchdog_enable
5:6	RW	SCOM_HANG_LIMIT: 0b11: 256, 0b10:512, 0b01:768, 0b00:1023
7	RW	FORCE_ALL_RINGS: set to logic 1 if all rings should be enable independent of ring address
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: fsm_selfreset_on_statevec_parityerror_enable
9:11	RW	RESERVED_PSCOM_MODE_LT: reserved

Register Name	***PSCOMLE Error Register***
Mnemonic	TPTOP.TPC.EPS.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000001010001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated_PCB_wdata_parity_error
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated_PCB_address_parity_error
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated_DL_return_wdata_parity_error
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated_DL_return_P0_error
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated_UL_rdata_parity_error
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated_UL_P0_error
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated_parity_error_on_interface_machine
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated_parity_error_on_p2s_machine
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated_timeout_while_waiting_for_ULCCH
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated_timeout_while_waiting_for_DLDCH_return
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated_timeout_while_waiting_for_ULDCH
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated_pscom_parallel_write_nvld
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated_pscom_parallel_read_nvld
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated_pscom_parallel_addr_invalid
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated_PCB_command_parity_error
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated_General_timeout
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated_satellite_acknowledge_access_violation
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated_satellite_acknowledge_invalid_register
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped_PCB_wdata_parity_error
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped_PCB_address_parity_error
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped_DL_return_wdata_parity_error
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped_DL_return_P0_error
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped_UL_rdata_parity_error

Bits	PCB	Field Mnemonic: Description
23	RWX	TRAPPED_UL_P0_ERROR: Trapped_UL_P0_error
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped_parity_error_on_interface_machine
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped_parity_error_on_p2s_machine
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped_timeout_while_waiting_for_ULCCH
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped_timeout_while_waiting_for_DLDCH_return
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped_timeout_while_waiting_for_ULDCH
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped_pscom_parallel_write_nvld
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped_pscom_parallel_read_nvld
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped_pscom_parallel_addr_invalid
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped_PCB_command_parity_error
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped_General_timeout
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped_satellite_acknowledge_access_violation
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped_satellite_acknowledge_invalid_register

Register Name	***PSCOMLE Error Mask Register***
Mnemonic	TPTOP.TPC.EPS.PSC.PSCOM_ERROR_MASK
Address	0000000001010002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: mask_PCB_wdata_parity_error
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: mask_PCB_address_parity_error
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: mask_DL_return_wdata_parity_error
3	RW	MASK_DL_RETURN_P0_ERROR: mask_DL_return_P0_error
4	RW	MASK_UL_RDATA_PARITY_ERROR: mask_UL_rdata_parity_error
5	RW	MASK_UL_P0_ERROR: mask_UL_P0_error
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: mask_parity_error_on_interface_machine
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: mask_parity_error_on_p2s_machine
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: mask_timeout_while_waiting_for_ULCCH
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: mask_timeout_while_waiting_for_DLDCH_return
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: mask_timeout_while_waiting_for_ULDCH
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: mask_pscom_parallel_write_nvld
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: mask_pscom_parallel_read_nvld
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: mask_pscom_parallel_addr_invalid
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: mask_PCB_command_parity_error
15	RW	MASK_GENERAL_TIMEOUT: mask_general_timeout
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: mask_satellite_acknowledge_access_violation

Bits	PCB	Field Mnemonic: Description
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: mask_satellite_acknowledge_invalid_register

Register Name	***PSCOMLE Address Trap Register***
Mnemonic	TPTOP.TPC.EPS.PSC.ADDR_TRAP_REG
Address	0000000001010003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB_address_of_last_transaction_with_error
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB_read_notwrite_of_last_transaction_with_error
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: reserved_0
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2Parallel_state_machine_at_time_of_error
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit: set to 1 if no parity error detected of Sat. No and Ack-bits
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: set if write parity error detected by satellite
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: set if invalid read or write access detected by satellite
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: set if invalid register address detected by satellite

Register Name	***Debug Status Register***
Mnemonic	TPTOP.TPC.EPS.PSC.DEBUG_STATUS_REG
Address	0000000001010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: local trace run
1:2	RWX	TRACE_STATE_LAT: trace state latch
3	RWX	TRACE_FREEZE: trace freeze
4:5	RWX	COND3_STATE_LT: condition 3 state latch
6:7	RWX	COND5_STATE_LT: condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: condition event history for condtition0_lt
9	RWX	HISTORY_CONDITION1_LT: condition event history for condtition1_lt
10	RWX	HISTORY_COND2_3_EVENT: condition event history for cond2_3_event
11	RWX	HISTORY_COND2_TIMEOUT: condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: reserved, set to zero

Register Name	***PSCOMLE Modewrite Protect Enable Register***
Mnemonic	TPTOP.TPC.EPS.PSC.PSCOM_WRITE_PROTECT_REG
Address	0000000001010005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_SERIAL_RING_WRITE_PROTECT: enable_serial_ring_write_protect
1	RW	RESERVED_WRITE_PROTECT: enable_serial_ring_write_protect

Register Name	***Atomic Lock Register***
Mnemonic	TPTOP.TPC.EPS.PSC.ATOMIC_LOCK_REG
Address	00000000010103FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	***Trace Array High Data Register***
Mnemonic	TPTOP.TPC.TRA.PERVTRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000001010440 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	***Trace Array Low Data Register***
Mnemonic	TPTOP.TPC.TRA.PERVTRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000001010441 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid

Bits	SCOM	Field Mnemonic: Description
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	*Interrupt Presentation Register*
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT1_REG
Address	0000000001020000 (PCB) 0000000001020001 (PCB1) 0000000001020002 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT1: interrupt type 1 (gp) for up to 32 chiplets

Register Name	*Interrupt Presentation Register*
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT2_REG
Address	0000000001020003 (PCB) 0000000001020004 (PCB1) 0000000001020005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT2: interrupt type 2 (cc) for up to 32 chiplets

Register Name	*Interrupt Presentation Register*
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT3_REG
Address	0000000001020006 (PCB) 0000000001020007 (PCB1) 0000000001020008 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT3: interrupt type 3 (--) for up to 32 chiplets

Register Name	*Interrupt Presentation Register*
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT4_REG
Address	0000000001020009 (PCB) 000000000102000A (PCB1) 000000000102000B (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT4: interrupt type 4 (--) for up to 32 chiplets

Register Name	*Interrupt Type Mask Register*
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT_TYPE_MASK_REG
Address	000000000102000C (PCB) 000000000102000D (PCB1) 000000000102000E (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_GP: Mask all BIST Done interrupts (0 = active, 1 = masked)
1	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_CC: Mask all clock state change interrupts (0 = active, 1 = masked)
2	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_UNUSED2: Mask all clock state change interrupts (0 = active, 1 = masked)
3	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_UNUSED3: Mask all clock state change interrupts (0 = active, 1 = masked)

Register Name	*Interrupt Configuration Register*
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT_CONF_REG
Address	000000000102000F (PCB) 0000000001020010 (PCB1) 0000000001020011 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_GP: Configuration for BIST Done interrupts (0 = or, 1 = and)
1	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_CC: Configuration for clock state change interrupts (0 = or, 1 = and)
2	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED2: Configuration for clock state change interrupts (0 = or, 1 = and)
3	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED3: Configuration for clock state change interrupts (0 = or, 1 = and)

Register Name	***Last Interrupt Packet Received From PCB Master***
Mnemonic	TPTOP.TPC.ITR.COMP.INTERRUPT_HOLD_REG
Address	0000000001020012 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:25	ROX	INTERRUPT_HOLD: Last interrupt packet received from PCB Master

Register Name	***IPOLL Mask Register***
Mnemonic	TPTOP.TPC.ITR.MISC.IPOLL_MASK_REG
Address	0000000001020013 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	IPOLL_MASK_X: IPOLL mask for xstop
1	RW	IPOLL_MASK_R: IPOLL mask for recoverable
2	RW	IPOLL_MASK_A: IPOLL mask for special attention
3	RW	IPOLL_MASK_H: IPOLL mask for host attention
4	RW	ERROR_MASK_X: mask xstop from fsi_intr
5	RW	ERROR_MASK_R: mask recoverable from fsi_intr
6	RW	ERROR_MASK_A: mask attention from fsi_intr
7	RW	ERROR_MASK_H: mask host attention from fsi_intr

Register Name	***Status Of The Errors***
Mnemonic	TPTOP.TPC.ITR.MISC.ERROR_STATUS_REG
Address	0000000001020014 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	ipoll_err_masked status of ipoll errors
4:7	ROX	fsi_err_masked status of fsi errors

Register Name	*OSC Error Hold Latch*
Mnemonic	TPTOP.TPC.ITR.OSCERR.OSCERR_HOLD
Address	0000000001020019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RWX	OSCERR_CP: OSC Error hold values for cp
4:7	RWX	OSCERR_MEM: OSC Error hold values for mem
8:11	RO	Reserved.
12:15	RWX	OSCERR_CPLITE: OSC Error hold values for cplite

Register Name	*OSC Error Mask Latch*
Mnemonic	TPTOP.TPC.ITR.OSCERR.OSCERR_MASK
Address	000000000102001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	OSCERR_CP_MASK: OSC Error hold values for cp
4:7	RW	OSCERR_MEM_MASK: OSC Error hold values for mem
8:11	RO	Reserved
12:15	RW	OSCERR_CPLITE_MASK: OSC Error hold values for cplite

Register Name	*OSC Error Mcode Latch*
Mnemonic	TPTOP.TPC.ITR.OSCERR.OSCERR_MCODE
Address	000000000102001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	OSCERR_MCODE_IN: OSC Error mcode

Register Name	*Counter References*
Mnemonic	TPTOP.TPC.ITR.FMU.FMU_MODE_REG
Address	0000000001020028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	RW	TOD_CNTR_REF: To determine timeframe the oscillator pulses are counted. This value is compared to a 16 bit wide tod pulse counter.

Bits	PCB	Field Mnemonic: Description
16	RW	Reserved field (Access type is unused1)
17:19	RW	POWER_UP_CNTR_REF: To determine timeframe the fmu starts counting the oscillator pulses. This value is compared to a 3 bit wide tod pulse counter. Needs to be 0b010 in case time to wait must be >= 62.5 ns (16 MHZ)
20:23	RW	Reserved field (Access type is unused2)

Register Name	***Osc Counter1 - Stressed Osc Counter For NBTI***
Mnemonic	TPTOP.TPC.ITR.FMU.FMU_OSC_CNTR1_REG
Address	0000000001020029 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RO	constant=0b0
1	ROX	Reserved field (Access type is fmu_pulse_gen_reg_err)
2	ROX	Reserved field (Access type is fmu_modereg_p_err)
3	ROX	RESULT_AVAILABLE: FMU result available
4:27	ROX	OSC_PULSE1_CNTR: Osc Counter1 - Stressed Osc Counter for NBTI

Register Name	***Counter References For Int***
Mnemonic	TPTOP.TPC.ITR.FMU.FMU_PULSE_GEN_REG
Address	0000000001020029 (PCB)
Attributes	
Description	Pulse

Bits	PCB	Field Mnemonic: Description
0	WO	FMU_INT_PULSE_ENA: FMU internal Tod pulse generation enable
1	WO	Reserved field (Access type is unused3)
2:11	WO	FMU_INT_PULSE_CNTR_REF: Reference value to compare against 10 Bit counter for FMU internal Tod pulse generation

Register Name	***Osc Counter2 - Reference Osc Counter For NBTI***
Mnemonic	TPTOP.TPC.ITR.FMU.FMU_OSC_CNTR2_REG
Address	000000000102002A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RO	constant=0b0
1	ROX	Reserved field (Access type is fmu_pulse_gen_reg_err)
2	ROX	Reserved field (Access type is fmu_modereg_p_err)

Bits	PCB	Field Mnemonic: Description
3	ROX	RESULT_AVAILABLE: FMU result available
4:27	ROX	OSC_PULSE2_CNTR: Osc Counter2 - Stressed Osc Counter for NBTI

Register Name	*Force Operations*
Mnemonic	TPTOP.TPC.ITR.FMU.FMU_FORCE_OP_REG
Address	000000000102002B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	NC	Reserved field (Access type is force_measure)
1	NC	Reserved field (Access type is force_fmu_sm_reset)

Register Name	*Configuration Of CC Counters*
Mnemonic	TPTOP.TPC.SYNC_CONFIG
Address	0000000001030000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ISLE_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from chiplet
1	RW	PCB_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from pcb
2	RW	CLKSTP_SYNC_EN: stop clocks aligned to sync pulse
3	RW	EDRAM_XSTOP_MASK_B: mask for clockstop of eDRAM clock on any xstop
4	RW	PLL_XSTOP_MASK_B: mask for clockstop of pll clock on any xstop
5	RW	LOCAL_XSTOP_MASK_B: mask for clockstop of all island clocks on local xstop from chiplet
6	RW	DISABLE_PCB_ITR: disable interrupt generation within CC
7	RW	USE_SYNC_FOR_SCAN: if set, use opcg initial alignment for scan requests
8	RW	KEEP_EDRAM_ON_XSTOP: keep eDRAM enabled when a checkstop occurs
9	RW	TRIGGER_OPCG_ON_XSTOP: trigger opcg on xstop instead of performing clockstop
10	RW	SEL_EXT_OPCG_TRIGGER: select external OPCG trigger (set OPCG in slave mode)
11	RW	LISTEN_TO_SYNC_PULSE: enable phase counter synchronization by sync_pulse signal
12	RW	SYNC_CLK_START_ENABLE: enable clk start driven by tc_sync_clk_stop (falling edge)
13	RW	SYNC_CLK_STOP_ENABLE: enable clk stop driven by tc_sync_clk_stop (rising_edge)
14	RWX_WOR	CHIP_PROTECTION_ENABLE: memory buffer only - can only be set, but not cleared via PCB. When this bit is SET, no clock starts are possible. Only two scan0's will clear this bit
15	RW	SPARE15: spare
16	RW	SPARE16: spare
17	RW	SPARE17: spare
18	RW	SPARE18: spare
19	RW	SPARE19: spare

Bits	PCB	Field Mnemonic: Description
20	RW	SPARE20: spare

Register Name	*Counter Offset*
Mnemonic	TPTOP.TPC.PHASE_SHADOW
Address	0000000001030001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RWX	PHASE_COUNT_SHADOW_Q: offset for sync counter
6	RO	constant=0b0

Register Name	*OPCG Control Register 0*
Mnemonic	TPTOP.TPC.OPCG_REG0
Address	0000000001030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), runn-mode: loopcnt(4:6)
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count (l = 1-2^28 (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	*OPCG Control Register 1*
Mnemonic	TPTOP.TPC.OPCG_REG1
Address	0000000001030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1
4:43	RW	FUNC_CAPT_INSTR_F: BIST mode: functional capture Instr 0-7 f domain (sl, nsl, ary, sg, fce)
44:63	RW	FUNC_CAPT_INSTR_FBY2: BIST mode: functional capture Instr 0-3 f/2 domain (sl, nsl, ary, sg, fce)

Register Name	***OPCG Control Register 2***
Mnemonic	TPTOP.TPC.OPCG_REG2
Address	0000000001030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	SCAN_CLK_USE_EVEN: BIST mode: Generate scan clock in f odd cycle. runn-mode: run one additional clock in f domain
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill runn-mode: OPCG engine controls start_abist (overrides GP0 setting)
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	***Opcg Start Register***
Mnemonic	TPTOP.TPC.OPCG_REG3
Address	0000000001030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence)
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse)
2	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse)
3:4	RW	ALIGN_SOURCE_SELECT: 0: use inopa setting from opcg_reg0, 1: use rising edge of sync pulse, 2: use input from unit (for AVP)

Bits	PCB	Field Mnemonic: Description
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: set to 0 for prpg always on, else seed
20	RW	EXTEND_INOPW_ENOPW: extend I/ENOPW: add 256 cycles if i/enop>0, else 257+max i/enop
21	RW	EXTEND_SNOPW: add 256 cycles if snop>0, else 257+max snop
22	RW	FORCE_SG_HIGH_DURING_SNOP: force sg high during snop
23:31	RW	CHKSW: reserved for debug switches (keep 0 unless chksw required)
32:43	RW	PRPG_A_VAL: a value for PRPG aperture
44:55	RW	PRPG_B_VAL: b value for PRPG aperture
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end)
57:63	RW	SPARE3: spares

Register Name	***Start/stop Of Clocks***
Mnemonic	TPTOP.TPC.CLK_REGION
Address	0000000001030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	constant=0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)
5	RWX	CLOCK_REGION_UNIT0: for clock region net
6	RWX	CLOCK_REGION_UNIT1: for clock region pib
7	RWX	CLOCK_REGION_UNIT2: for clock region unit2 region is UNUSED
8	RWX	CLOCK_REGION_UNIT3: for clock region unit3 region is UNUSED
9	RWX	CLOCK_REGION_UNIT4: for clock region unit4 region is UNUSED
10	RWX	CLOCK_REGION_UNIT5: for clock region unit5 region is UNUSED
11	RWX	CLOCK_REGION_PLL: for clock region pll
12	RWX	CLOCK_REGION_OSCSW: for clock region oscsw region is UNUSED
13:19	RO	constant=0b0000000
20	RWX	SEL_THOLD_SL: select sl tholds
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name	***Scan Region And Type***
Mnemonic	TPTOP.TPC.SCANSELQ
Address	0000000001030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b000
3	RW_WCLRPART	SCANSEL_CLK_VITL: scan clock region vitl (Vital = Clock)
4	RWX	SCANSEL_CLK_PERV: scan clock region perv (Pervasive)
5	RWX	SCANSEL_CLK_UNIT0: scan clock region net
6	RWX	SCANSEL_CLK_UNIT1: scan clock region pib
7	RWX	SCANSEL_CLK_UNIT2: scan clock region unit2 region is UNUSED
8	RWX	SCANSEL_CLK_UNIT3: scan clock region unit3 region is UNUSED
9	RWX	SCANSEL_CLK_UNIT4: scan clock region unit4 region is UNUSED
10	RWX	SCANSEL_CLK_UNIT5: scan clock region unit5 region is UNUSED
11	RWX	SCANSEL_CLK_PLL: scan clock region pll
12	RWX	SCANSEL_CLK_OSCSW: scan clock region oscsw region is UNUSED
13:19	RO	constant=0b0000000
20	RW	SCANSEL_FUNC: scan chain func (functional)
21	RW	SCANSEL_CFG: scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: scan chain ccfg / gptr (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: scan chain regf (register files)
24	RW	SCANSEL_LBIST: scan chain lbst (LBIST)
25	RW	SCANSEL_ABIST: scan chain abst (ABIST)
26	RW	SCANSEL_REPR: scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: scan chain time (Array Timing)
28	RW	SCANSEL_BNDY: scan chain bndy (Boundary IOs)
29	RW	SCANSEL_FARR: scan chain farr (fast array unload)
30	RW	SCANSEL_CMSK: scan chain cmsk (lbist channel mask)

Register Name	***Clocks Running***
Mnemonic	TPTOP.TPC.CLOCK_STAT
Address	0000000001030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: status of perv func_sl_thold 0=run, 1=stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: status of perv func_nsl_thold 0=run, 1=stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: status of perv ary_nsl_thold 0=run, 1=stop
3	ROX	CLOCK_STATUS_UNIT0_FUNC_SL: status of net func_sl_thold 0=run, 1=stop
4	ROX	CLOCK_STATUS_UNIT0_FUNC_NSL: status of net func_nsl_thold 0=run, 1=stop
5	ROX	CLOCK_STATUS_UNIT0_ARY_NSL: status of net ary_nsl_thold 0=run, 1=stop
6	ROX	CLOCK_STATUS_UNIT1_FUNC_SL: status of pib func_sl_thold 0=run, 1=stop
7	ROX	CLOCK_STATUS_UNIT1_FUNC_NSL: status of pib func_nsl_thold 0=run, 1=stop
8	ROX	CLOCK_STATUS_UNIT1_ARY_NSL: status of pib ary_nsl_thold 0=run, 1=stop

Bits	PCB	Field Mnemonic: Description
9	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of unit2 func_sl_thold 0=run, 1=stop region is UNUSED
10	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of unit2 func_nsl_thold 0=run, 1=stop region is UNUSED
11	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of unit2 ary_nsl_thold 0=run, 1=stop region is UNUSED
12	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of unit3 func_sl_thold 0=run, 1=stop region is UNUSED
13	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of unit3 func_nsl_thold 0=run, 1=stop region is UNUSED
14	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of unit3 ary_nsl_thold 0=run, 1=stop region is UNUSED
15	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of unit4 func_sl_thold 0=run, 1=stop region is UNUSED
16	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of unit4 func_nsl_thold 0=run, 1=stop region is UNUSED
17	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of unit4 ary_nsl_thold 0=run, 1=stop region is UNUSED
18	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of unit5 func_sl_thold 0=run, 1=stop region is UNUSED
19	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of unit5 func_nsl_thold 0=run, 1=stop region is UNUSED
20	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of unit5 ary_nsl_thold 0=run, 1=stop region is UNUSED
21	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of pll func_sl_thold 0=run, 1=stop
22	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of pll func_nsl_thold 0=run, 1=stop
23	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of pll ary_nsl_thold 0=run, 1=stop
24	ROX	CLOCK_STATUS_OSCSW_FUNC_SL: status of oscsw func_sl_thold 0=run, 1=stop region is UNUSED
25	ROX	CLOCK_STATUS_OSCSW_FUNC_NSL: status of oscsw func_nsl_thold 0=run, 1=stop region is UNUSED
26	ROX	CLOCK_STATUS_OSCSW_ARY_NSL: status of oscsw ary_nsl_thold 0=run, 1=stop region is UNUSED
27:63	RO	constant=0b11111111111111111111111111111111111111

Register Name	***Error Status Of CC***
Mnemonic	TPTOP.TPC.ERROR_STATUS
Address	0000000001030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: scan collision
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error

Bits	PCB	Field Mnemonic: Description
13	RWX	PHASE_CNT_CORRUPTED: phase hold counter corruption detected
14:15	RWX	CC_PAR_ERR: parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: parity error in GP0 register
17	RWX	SECURITY_VIOLATION: security_violation - when Chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name	***CC Protect Mode Register***
Mnemonic	TPTOP.TPC.CC_PROTECT_MODE_REG
Address	00000000010303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TPTOP.TPC.CC_ATOMIC_LOCK_REG
Address	00000000010303FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	CC_ATOMIC_ID: Atomic ID

Register Name	***Global Checkstop FIR***
Mnemonic	TPTOP.TPC.XFIR
Address	0000000001040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: Unused
3	RWX	XFIR_IN3: xstop from pervasive unit
4:25	RWX	XFIR_IN4: unused
26	RWX	XFIR_IN26: xstop on debug trigger

Register Name	*Global Recoverable FIR*
Mnemonic	TPTOP.TPC.RFIR
Address	0000000001040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: unused
1	ROX	LFIR_RECOV_ERR: error from local LFIR
2:23	ROX	RFIR_IN: recoverable errors: same mapping as XFIR(4:25)

Register Name	*FIR Mask*
Mnemonic	TPTOP.TPC.FIR_MASK
Address	0000000001040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit
1	RW	FIR_MASK_IN1: mask for xfir PCB status bit
2	RW	FIR_MASK_IN2: mask for xfir IO status bit
3	RW	FIR_MASK_IN3: mask for LFIR status bit
4:26	RW	FIR_MASK_IN4: masks for XFIR and RFIR

Register Name	*Special Attention*
Mnemonic	TPTOP.TPC.EPS.FIR.SPATTN
Address	0000000001040004 (PCB) 0000000001040005 (PCB1) 0000000001040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: MEM Chiplet Only: Special Attention from MBA01
1	ROX	NCX	NCX	SPATTN_IN1: MEM Chiplet Only: Special Attention from MBA23
2:9	ROX	NCX	NCX	SPATTN_IN2: unused special attentions

Register Name	*Special Attention Mask*
Mnemonic	TPTOP.TPC.EPS.FIR.SPA_MASK
Address	0000000001040007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask

Register Name	*Mode Register*
Mnemonic	TPTOP.TPC.EPS.FIR.MODE_REG
Address	0000000001040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: unused

Register Name	*Local FIR*
Mnemonic	TPTOP.TPC.LOCAL_FIR
Address	000000000104000A (PCB) 000000000104000B (PCB1) 000000000104000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (critical Trip error)
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (fatal Trip error)
10	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Thermal (Voltage Trip error)
11	RWX	WOX_AND	WOX_OR	FIR_IN11: local errors from Trace Array (error)
12	RWX	WOX_AND	WOX_OR	FIR_IN12: local errors from Trace Array (error)
13:14	RWX	WOX_AND	WOX_OR	FIR_IN13: local errors from ITR
15	RWX	WOX_AND	WOX_OR	FIR_IN15: local errors from ITR (itr_tc_pcbsl_slave_fir_err)
16:18	RWX	WOX_AND	WOX_OR	FIR_IN16: local errors from PIB ()
19	RWX	WOX_AND	WOX_OR	FIR_IN19: local errors from nest PLLlock
20	RWX	WOX_AND	WOX_OR	FIR_IN20: local errors from mem PLLlock
21:39	RWX	WOX_AND	WOX_OR	FIR_IN21: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	***Local FIR Mask***
Mnemonic	TPTOP.TPC.EPS.FIR.LOCAL_FIR_MASK
Address	000000000104000D (PCB) 000000000104000E (PCB1) 000000000104000F (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

Register Name	***Local FIR Action0***
Mnemonic	TPTOP.TPC.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000001040010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name	*Local FIR Action1*
Mnemonic	TPTOP.TPC.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000001040011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name	*DTS Thermal Sensor Results*
Mnemonic	TPTOP.TPC.EPS.THERM.DTS_RESULT0
Address	0000000001050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	*DTS Trace Results*
Mnemonic	TPTOP.TPC.EPS.THERM.DTS_TRC_RESULT
Address	0000000001050003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant=0b000
48:63	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.

Register Name	*DTS0-1 Bit 0 - 15: Temperature Result DTS0, Bit 16 - 31: Temperature Result DTS1 (available only in NEST Chiplet),*
Mnemonic	TPTOP.TPC.EPS.THERM.ENC_CPM_RESULT0
Address	0000000001050008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.

Bits	PCB	Field Mnemonic: Description
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.
32:55	RO	constant=0b00000000000000000000000

Register Name	*Voltage Sensor Results*
Mnemonic	TPTOP.TPC.EPS.THERM.VOLT_READ0
Address	000000000105000B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	Reserved field (Access type is volt_data0)
16:31	ROX	Reserved field (Access type is volt_data1)
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	*CPM & DTS Enables And Controls*
Mnemonic	TPTOP.TPC.EPS.THERM.THERM_MODE_REG
Address	000000000105000F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: critical path result bubble correction active
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables 1xx: trip0 - warning x1x: trip1 - critical xx1: trip2 - fatal
5	RW	THERM_DTS_SAMPLE_ENA: 0: no dts sampling, 1: dts sampling is enabled and below counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is feed into an 18 Bit counter, with the therm_sample_pulse_cnt it is possible to select a highorder bit of the counter to enable a resolutions of sampling dtss between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a dts sample 0000: 16 ms 0001: 8 ms 0010: 4 ms 0011: 2 ms 0100: 1 ms 0101: 0.5 ms 0110: 250 us 0111: 125 us 1000: 62 .5us 1001: 31.3 us 1010: 15.6 us 1011: 7.8 us 1100: 3.9 us 1101: 2 us 1110: 1 us 1111: 0.5 us

Bits	PCB	Field Mnemonic: Description
10:11	RW	THERM_THRES_MODE_ENA: forces max or min mode in threshold unit: 00: is off 11: is illegal 10: max mode 01: min mode
12	RW	DTS_TRIGGER_MODE: unused
13	RW	DTS_TRIGGER_SEL: unused
14:15	RW	THERM_MODE_UNUSED: unused
16:19	RW	THERM_DTS_READ_SEL: selects which dts result will be provided with pcb read addr_v(4): 000: DTS 0 001: DTS 1 010: DTS 2 011: DTS 3 100: DTS 4 111: Worst Case Sensor
20:21	RW	THERM_DTS_ENABLE: dts enables: 1xxxx: DTS 0 available x1xx: DTS 1 available
22:34	RO	constant=0b0000000000000
35:36	RW	THERM_CPM_ENABLE: cpm enables

Register Name	***Skitter Control Register***
Mnemonic	TPTOP.TPC.EPS.THERM.SKITTER_MODE_REG
Address	0000000001050010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: forces skitter to hold current sample
1	RW	DISABLE_SKITTER_STICKINESS: if '0' accumulation mode, '1' samples new value each cycle and resets sticky value
2:3	RW	SKITTER_MODE_UNUSED1: unused
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0 bit1: _on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0 bit1: reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: selects guts to measure: 00: guts1 01: guts2 10: guts3 11: guts4
10:43	RO	constant=0b00000000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: forces skitter to hold current sample on dbg trigger, this has highest priority
45	ROX	SKITTER_DATA_V_LT: if '1' the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 pcb reads

Register Name	***Error Injection Control Register***
Mnemonic	TPTOP.TPC.EPS.THERM.INJECT_REG
Address	0000000001050011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection 01: warning trip level injection 10: critical trip level injection 11: fatal trip level injection
2:3	RW	THERM_INJECT_MODE: 00: no injection 01: injection on the next dts sample 10: solid injection for the next dts samples till bit setting changes 11: not used

Register Name	***Control / Force Reset Register***
Mnemonic	TPTOP.TPC.EPS.THERM.CONTROL_REG
Address	0000000001050012 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	WO_1P	Reserved field (Access type is reset_trip_history)
1	WO_1P	Reserved field (Access type is reset_sample_pulse_cnt)
2	WO_1P	Reserved field (Access type is f_reset_cpm_rd)
3	WO_1P	Reserved field (Access type is f_reset_cpm_wr)
4	WO_1P	Reserved field (Access type is reset_sample_dts)
5	WO_1P	Reserved field (Access type is force_sample_dts)
6	WO_1P	Reserved field (Access type is force_sample_dts_interruptible)
7	WO_1P	Reserved field (Access type is force_reset_thres_l1results)
8	WO_1P	Reserved field (Access type is force_reset_thres_l2results)
9	WO_1P	Reserved field (Access type is force_reset_thres_l3results)
10	WO_1P	Reserved field (Access type is force_measure_volt_interruptible)
11	WO_1P	Reserved field (Access type is force_reset_measure_volt)
12	WO_1P	Reserved field (Access type is force_shift_sensor)

Register Name	***Thermal Error Status Register***
Mnemonic	TPTOP.TPC.EPS.THERM.ERR_STATUS_REG
Address	0000000001050013 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is serial_shiftcnt_modereg_parity_err_hold)
1	ROX	Reserved field (Access type is therm_modereg_parity_err_hold)
2	ROX	Reserved field (Access type is skitter_modereg_parity_err_hold)
3	ROX	Reserved field (Access type is skitter_forcereg_parity_err_hold)
4	ROX	Reserved field (Access type is scan_init_version_reg_parity_err_hold)
5	ROX	Reserved field (Access type is volt_modereg_parity_err_hold)
6	ROX	Reserved field (Access type is skitter_clksrcreg_parity_err_hold)
7	ROX	Reserved field (Access type is count_state_err_hold)
8	ROX	Reserved field (Access type is run_state_err_hold)
9	ROX	Reserved field (Access type is thres_therm_state_err_hold)
10	ROX	Reserved field (Access type is thres_therm_overflow_err_hold)
11	ROX	Reserved field (Access type is shifter_parity_err_hold)
12	ROX	Reserved field (Access type is shifter_valid_err_hold)
13	ROX	Reserved field (Access type is timeout_err_hold)
14	ROX	Reserved field (Access type is f_skitter_err_hold)
15	ROX	Reserved field (Access type is pcb_err_hold_out)
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: serial shift count parity error mask
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: therm mode reg parity error mask
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: skitter mode register parity error mask
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: skitter force register parity error mask
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: scan init version register parity error mask
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: volt mode reg parity error mask
22	RO	constant=0b0
23	ROX	COUNT_STATE_ERR_MASK: count state machine error mask
24	ROX	RUN_STATE_ERR_MASK: run state machine error mask
25	ROX	THRES_STATE_ERR_MASK: thres state machine error mask
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask
30	ROX	F_SKITTER_READ_ERR_MASK: force skitter read one hot error mask
31	ROX	PCB_ERR_MASK: pervasive control bus error mask
32:39	RO	constant=0b00000000
40:43	ROX	Reserved field (Access type is count_state_lt)
44:46	ROX	Reserved field (Access type is run_state_lt)
47	ROX	Reserved field (Access type is shift_dts_lt)
48	ROX	Reserved field (Access type is shift_volt_lt)
49:50	ROX	Reserved field (Access type is read_state_lt)
51:54	ROX	Reserved field (Access type is write_state_lt)
55	ROX	Reserved field (Access type is sample_dts_lt)
56	ROX	Reserved field (Access type is measure_volt_lt)

Bits	PCB	Field Mnemonic: Description
57	ROX	Reserved field (Access type is read_cpm_lt)
58	ROX	Reserved field (Access type is write_cpm_lt)
59	ROX	Reserved field (Access type is unused)
60:63	RO	constant=0b0000

Register Name	***Skitter Force Read Register***
Mnemonic	TPTOP.TPC.EPS.THERM.SKITTER_FORCE_REG
Address	0000000001050014 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter

Register Name	***Voltage Sensor Enables And Controls***
Mnemonic	TPTOP.TPC.EPS.THERM.VOLT_MODE_REG
Address	0000000001050015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	VOLT_MEASURE_ENA: enables the measurement of voltage sensor
1	RW	VOLT_TRIP_ENA: enables the trip of voltage sensor
2:3	RW	VOLT_ENABLE: Voltage sensor enables 1xxxx:voltage sensor0 available

Register Name	***Skitter Clock Src Control Register***
Mnemonic	TPTOP.TPC.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000001050016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: selects clock to measure: 000: local mesh clock 001: external pin skitter_c1_1_in 010: local d1clk only if d_mode = 1 011: external pin skitter_c1_2_in 100: local lclk only if d_mode = 1 101: external pin skitter_c1_3_in 110: unused 111: external pin skitter_c1_4_in
3:35	RO	constant=0b00000000000000000000000000000000

Register Name	***Skitter Data Register Read Bit0:63***
Mnemonic	TPTOP.TPC.EPS.THERM.SKITTER_DATA0
Address	0000000001050019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Skitter Data Register Read Bit32:95***
Mnemonic	TPTOP.TPC.EPS.THERM.SKITTER_DATA1
Address	000000000105001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Skitter Data Register Read Bit64:127***
Mnemonic	TPTOP.TPC.EPS.THERM.SKITTER_DATA2
Address	000000000105001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Timestamp Counter Read***
Mnemonic	TPTOP.TPC.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000105001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.

Register Name	***Contains The Slave's Primary Address***
Mnemonic	TPTOP.NET.PCBSLPERV.PRIMARY_ADDRESS_REG
Address	00000000010F0000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	***Multicast Group 1***
Mnemonic	TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_1
Address	00000000010F0001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	***Multicast Group 2***
Mnemonic	TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_2
Address	00000000010F0002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name	***Multicast Group 3***
Mnemonic	TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_3
Address	00000000010F0003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	*Multicast Group 4*
Mnemonic	TPTOP.NET.PCBSLPERV.MULTICAST_GROUP_4
Address	00000000010F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	*Timeout Select Register*
Mnemonic	TPTOP.NET.PCBSLPERV.TIMEOUT_REG
Address	00000000010F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	*Assist Interrupt Register*
Mnemonic	TPTOP.NET.PCBSLPERV.ASSIST_INTERRUPT_REG
Address	00000000010F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

Register Name	*GP3 Register (NA In PERV CPLT)*
Mnemonic	TPTOP.NET.PCBSLPERV.GP3_REG
Address	00000000010F0012 (PCB) 00000000010F0013 (PCB1) 00000000010F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2:4	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
5	RWX	RWX_WAND	RWX_WOR	NCLK_NODIV: Force cache_nclk to equal nclk (for test only).
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FENCE2_EN: Fencing signal for chiplet.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
22	RWX	RWX_WAND	RWX_WOR	RESCLK_FLUSH: Flush for resonant clocking.
23	RWX	RWX_WAND	RWX_WOR	RESCLK_OVERRIDE_VALUE: Override value for resonant clocking.
24	RWX	RWX_WAND	RWX_WOR	DPHY_PLL: dphy pll
25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	FSYNC_ENABLE: Set the 'Frame Synchronous (Geared) Clocking Mode' .
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
30	RWX	RWX_WAND	RWX_WOR	CHIPET_RI: Chiplet RI
31	RWX	RWX_WAND	RWX_WOR	CHIPET_DI1: Chiplet DI1

Register Name	***Skew Adjust Data***
Mnemonic	TPTOP.NET.PCBSLPERV.CLK_ADJ_REG
Address	00000000010F0015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	***Clk Adjust Config***
Mnemonic	TPTOP.NET.PCBSLPERV.CLK_ADJ_SET
Address	00000000010F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	*Vital Scan Out*
Mnemonic	TPTOP.NET.PCBSLPERV.VITAL_SCAN_OUT
Address	00000000010F0017 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	*Chiplet Heartbeat Register*
Mnemonic	TPTOP.NET.PCBSLPERV.HEARTBEAT_REG
Address	00000000010F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

Register Name	*Lock Indications From PLLs*
Mnemonic	TPTOP.NET.PCBSLPERV.PLL_LOCK_REG
Address	00000000010F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	*Attn Interrupt*
Mnemonic	TPTOP.NET.PCBSLPERV.ATTN_INTERRUPT_REG
Address	00000000010F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	*Recov Interrupt*
Mnemonic	TPTOP.NET.PCBSLPERV.RECOV_INTERRUPT_REG
Address	00000000010F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	*Xstop Interrupt*
Mnemonic	TPTOP.NET.PCBSLPERV.XSTOP_INTERRUPT_REG
Address	00000000010F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

Register Name	*Slave Config Register*
Mnemonic	TPTOP.NET.PCBSLPERV.SLAVE_CONFIG_REG
Address	00000000010F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	*Error Capture Register*
Mnemonic	TPTOP.NET.PCBSLPERV.ERROR_REG
Address	00000000010F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name	***Hang Pulse Generation Register 0***
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_0_REG
Address	00000000010F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 1***
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_1_REG
Address	00000000010F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 2***
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_2_REG
Address	00000000010F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 3***
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_3_REG
Address	00000000010F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 4*
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_4_REG
Address	00000000010F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 5*
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_5_REG
Address	00000000010F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 6*
Mnemonic	TPTOP.NET.PCBSLPERV.HANG_PULSE_6_REG
Address	00000000010F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Divider For Hang Counter Clock*
Mnemonic	TPTOP.NET.PCBSLPERV.PRE_COUNTER_REG
Address	00000000010F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

Register Name	***Protect Mode Register***
Mnemonic	TPTOP.NET.PCBSLPERV.PROTECT_MODE_REG
Address	00000000010F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TPTOP.NET.PCBSLPERV.ATOMIC_LOCK_REG
Address	00000000010F03FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	***PIB Extended Error Register 0***
Mnemonic	TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_0
Address	00000000010FFF00 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:3	ROX	PCB_SLAVE0_ERROR_REG: PCB master error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
4:7	ROX	PCB_SLAVE1_ERROR_REG: PCB slave1 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
8:11	ROX	PCB_SLAVE2_ERROR_REG: PCB slave2 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
12:15	ROX	PCB_SLAVE3_ERROR_REG: PCB slave3 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
16:19	ROX	PCB_SLAVE4_ERROR_REG: PCB slave4 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
20:23	ROX	PCB_SLAVE5_ERROR_REG: PCB slave5 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
24:27	ROX	PCB_SLAVE6_ERROR_REG: PCB slave6 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
28:31	ROX	PCB_SLAVE7_ERROR_REG: PCB slave7 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
32:35	ROX	PCB_SLAVE8_ERROR_REG: PCB slave8 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
36:39	ROX	PCB_SLAVE9_ERROR_REG: PCB slave9 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
40:43	ROX	PCB_SLAVE10_ERROR_REG: PCB slave10 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Bits	PIB	Field Mnemonic: Description
44:47	ROX	PCB_SLAVE11_ERROR_REG: PCB slave11 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
48:51	ROX	PCB_SLAVE12_ERROR_REG: PCB slave12 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
52:55	ROX	PCB_SLAVE13_ERROR_REG: PCB slave13 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
56:59	ROX	PCB_SLAVE14_ERROR_REG: PCB slave14 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.
60:63	ROX	PCB_SLAVE15_ERROR_REG: PCB slave15 error. Bit(0)=Response Bit; Bit(1-3)=Error Code.

Register Name	***PIB Extended Error Register 1***
Mnemonic	TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_1
Address	00000000010FFF01 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP1_ERROR_REGS: PCB slave group 1 error registers

Register Name	***PIB Extended Error Register 2***
Mnemonic	TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_2
Address	00000000010FFF02 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP2_ERROR_REGS: PCB slave group 2 error registers

Register Name	***PIB Extended Error Register 3***
Mnemonic	TPTOP.PIB.JTAG2.JTAG2_MAC.JTAG2PIB.TP_PIB_MASTER_IF.PIB_EXTENDED_ERROR_REGISTER_3
Address	00000000010FFF03 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	PCB_SLAVE_GROUP3_ERROR_REGS: PCB slave group 3 error registers

3. PCB Slave 2: NEST Chiplet

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
DMI.BUSCTL.SCOM.FIR_ACTION0_REG	0x0000000002010406	463
DMI.BUSCTL.SCOM.FIR_ACTION1_REG	0x0000000002010407	464
DMI.BUSCTL.SCOM.FIR_MASK_REG	0x0000000002010403	462
DMI.BUSCTL.SCOM.FIR_REG	0x0000000002010400	460
DMI.BUSCTL.SCOM.FIR_WOF_REG	0x0000000002010408	464
DMI.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000002010420	464
FBIST.FBN.FBNAMC	0x00000000020108B2	522
FBIST.FBN.FBNBAC	0x00000000020108EA	537
FBIST.FBN.FBNCNTL	0x000000000201088A	476
FBIST.FBN.FBNCSPCR	0x0000000002010894	511
FBIST.FBN.FBNDCM0	0x00000000020108B8	525
FBIST.FBN.FBNDCM1	0x00000000020108B9	525
FBIST.FBN.FBNDCM10	0x00000000020108C2	527
FBIST.FBN.FBNDCM11	0x00000000020108C3	527
FBIST.FBN.FBNDCM12	0x00000000020108C4	528
FBIST.FBN.FBNDCM13	0x00000000020108C5	528
FBIST.FBN.FBNDCM14	0x00000000020108C6	528
FBIST.FBN.FBNDCM15	0x00000000020108C7	528
FBIST.FBN.FBNDCM2	0x00000000020108BA	525
FBIST.FBN.FBNDCM3	0x00000000020108BB	525
FBIST.FBN.FBNDCM4	0x00000000020108BC	526
FBIST.FBN.FBNDCM5	0x00000000020108BD	526
FBIST.FBN.FBNDCM6	0x00000000020108BE	526
FBIST.FBN.FBNDCM7	0x00000000020108BF	526
FBIST.FBN.FBNDCM8	0x00000000020108C0	527
FBIST.FBN.FBNDCM9	0x00000000020108C1	527
FBIST.FBN.FBNDCR	0x0000000002010897	512
FBIST.FBN.FBNDMEC0	0x00000000020108B3	523
FBIST.FBN.FBNDMEC1	0x00000000020108B4	523
FBIST.FBN.FBNDMEC2	0x00000000020108B5	523
FBIST.FBN.FBNDMEC3	0x00000000020108B6	524
FBIST.FBN.FBNEA	0x00000000020108E8	537
FBIST.FBN.FBNEAC	0x000000000201089D	514
FBIST.FBN.FBNED0	0x00000000020108C8	529
FBIST.FBN.FBNED1	0x00000000020108C9	529
FBIST.FBN.FBNED10	0x00000000020108D2	531
FBIST.FBN.FBNED11	0x00000000020108D3	531
FBIST.FBN.FBNED12	0x00000000020108D4	532
FBIST.FBN.FBNED13	0x00000000020108D5	532
FBIST.FBN.FBNED14	0x00000000020108D6	532
FBIST.FBN.FBNED15	0x00000000020108D7	532
FBIST.FBN.FBNED2	0x00000000020108CA	529
FBIST.FBN.FBNED3	0x00000000020108CB	529
FBIST.FBN.FBNED4	0x00000000020108CC	530
FBIST.FBN.FBNED5	0x00000000020108CD	530

Mnemonic	Address	Page
FBIST.FBN.FBNED6	0x00000000020108CE	530
FBIST.FBN.FBNED7	0x00000000020108CF	530
FBIST.FBN.FBNED8	0x00000000020108D0	531
FBIST.FBN.FBNED9	0x00000000020108D1	531
FBIST.FBN.FBNEIR	0x00000000020108E9	537
FBIST.FBN.FBNEMS	0x00000000020108B7	524
FBIST.FBN.FBNHPC	0x00000000020108A0	518
FBIST.FBN.FBNM0	0x00000000020108F0	539
FBIST.FBN.FBNM1	0x00000000020108F1	539
FBIST.FBN.FBNMR0	0x000000000201088B	477
FBIST.FBN.FBNMR1	0x000000000201088C	481
FBIST.FBN.FBNMR2	0x000000000201088D	485
FBIST.FBN.FBNMR3	0x000000000201088E	490
FBIST.FBN.FBNMR4	0x000000000201088F	494
FBIST.FBN.FBNMR5	0x0000000002010890	498
FBIST.FBN.FBNMR6	0x0000000002010891	502
FBIST.FBN.FBNMR7	0x0000000002010892	506
FBIST.FBN.FBNPAM0	0x000000000201089E	514
FBIST.FBN.FBNPAM1	0x000000000201089F	517
FBIST.FBN.FBNPARM0	0x0000000002010893	510
FBIST.FBN.FBNRAER	0x00000000020108EF	539
FBIST.FBN.FBNRAG	0x000000000201089B	513
FBIST.FBN.FBNRAMR	0x00000000020108EB	537
FBIST.FBN.FBNRASR	0x00000000020108EE	539
FBIST.FBN.FBNRCCR	0x0000000002010899	513
FBIST.FBN.FBNRCSR	0x0000000002010898	512
FBIST.FBN.FBNRD0	0x00000000020108D8	533
FBIST.FBN.FBNRD1	0x00000000020108D9	533
FBIST.FBN.FBNRD10	0x00000000020108E2	535
FBIST.FBN.FBNRD11	0x00000000020108E3	535
FBIST.FBN.FBNRD12	0x00000000020108E4	536
FBIST.FBN.FBNRD13	0x00000000020108E5	536
FBIST.FBN.FBNRD14	0x00000000020108E6	536
FBIST.FBN.FBNRD15	0x00000000020108E7	536
FBIST.FBN.FBNRD2	0x00000000020108DA	533
FBIST.FBN.FBNRD3	0x00000000020108DB	533
FBIST.FBN.FBNRD4	0x00000000020108DC	534
FBIST.FBN.FBNRD5	0x00000000020108DD	534
FBIST.FBN.FBNRD6	0x00000000020108DE	534
FBIST.FBN.FBNRD7	0x00000000020108DF	534
FBIST.FBN.FBNRD8	0x00000000020108E0	535
FBIST.FBN.FBNRD9	0x00000000020108E1	535
FBIST.FBN.FBNRDSR0	0x00000000020108EC	538
FBIST.FBN.FBNRDSR1	0x00000000020108ED	538
FBIST.FBN.FBNRMWC	0x000000000201089A	513
FBIST.FBN.FBNRTCTR	0x0000000002010895	512
FBIST.FBN.FBNSAC	0x000000000201089C	514
FBIST.FBN.FBNTT	0x0000000002010896	512
FBIST.FBN.FBNUD0	0x00000000020108A2	518
FBIST.FBN.FBNUD1	0x00000000020108A3	519
FBIST.FBN.FBNUD10	0x00000000020108AC	521

Mnemonic	Address	Page
FBIST.FBN.FBNUD11	0x00000000020108AD	521
FBIST.FBN.FBNUD12	0x00000000020108AE	521
FBIST.FBN.FBNUD13	0x00000000020108AF	522
FBIST.FBN.FBNUD14	0x00000000020108B0	522
FBIST.FBN.FBNUD15	0x00000000020108B1	522
FBIST.FBN.FBNUD2	0x00000000020108A4	519
FBIST.FBN.FBNUD3	0x00000000020108A5	519
FBIST.FBN.FBNUD4	0x00000000020108A6	519
FBIST.FBN.FBNUD5	0x00000000020108A7	520
FBIST.FBN.FBNUD6	0x00000000020108A8	520
FBIST.FBN.FBNUD7	0x00000000020108A9	520
FBIST.FBN.FBNUD8	0x00000000020108AA	520
FBIST.FBN.FBNUD9	0x00000000020108AB	521
FBIST.FBN.FBN_FIR_ACTION0_REG	0x0000000002010886	475
FBIST.FBN.FBN_FIR_ACTION1_REG	0x0000000002010887	476
FBIST.FBN.FBN_FIR_MASK_REG	0x0000000002010883	475
FBIST.FBN.FBN_FIR_REG	0x0000000002010880	474
MBU.MBI.MBI.MBIERPT0	0x000000000201080F	473
MBU.MBI.MBI.SCOMFIR.MBICFGQ	0x000000000201080A	469
MBU.MBI.MBI.SCOMFIR.MBICRCSYNQ	0x000000000201080C	471
MBU.MBI.MBI.SCOMFIR.MBIERRINJQ	0x000000000201080D	472
MBU.MBI.MBI.SCOMFIR.MBIFIRACT0	0x0000000002010806	468
MBU.MBI.MBI.SCOMFIR.MBIFIRACT1	0x0000000002010807	468
MBU.MBI.MBI.SCOMFIR.MBIFIRMASK	0x0000000002010803	467
MBU.MBI.MBI.SCOMFIR.MBIFIRQ	0x0000000002010800	465
MBU.MBI.MBI.SCOMFIR.MBIFIRWOF	0x0000000002010808	468
MBU.MBI.MBI.SCOMFIR.MBIFPGAINTRQ	0x000000000201080E	Error: Reference source not found
MBU.MBI.MBI.SCOMFIR.MBISTATQ	0x000000000201080B	471
MBU.MBS.ARB.RXLT.MBAXCR01Q	0x000000000201140B	545
MBU.MBS.ARB.RXLT.MBAXCR23Q	0x000000000201140C	546
MBU.MBS.ARB.RXLT.MBAXCRMSQ	0x000000000201140D	547
MBU.MBS.ARB.RXLT.MBSSIRACT0	0x0000000002011424	563
MBU.MBS.ARB.RXLT.MBSSIRACT1	0x0000000002011425	563
MBU.MBS.ARB.RXLT.MBSSIRMASK	0x0000000002011421	563
MBU.MBS.ARB.RXLT.MBSSIRQ	0x000000000201141E	562
MBU.MBS.ARB.RXLT.MBSXCRQ	0x000000000201140A	545
MBU.MBS.ECC01.MBECCFIR	0x0000000002011440	566
MBU.MBS.ECC01.MBECCFIR_ACTION0	0x0000000002011446	568
MBU.MBS.ECC01.MBECCFIR_ACTION1	0x0000000002011447	568
MBU.MBS.ECC01.MBECCFIR_MASK	0x0000000002011443	568
MBU.MBS.ECC01.MBECCFIR_WOF	0x0000000002011448	569
MBU.MBS.ECC01.MBMMRQ	0x000000000201145B	572
MBU.MBS.ECC01.MBMS0	0x000000000201144B	570
MBU.MBS.ECC01.MBMS1	0x000000000201144C	570
MBU.MBS.ECC01.MBMS2	0x000000000201144D	570
MBU.MBS.ECC01.MBMS3	0x000000000201144E	571
MBU.MBS.ECC01.MBMS4	0x000000000201144F	571
MBU.MBS.ECC01.MBMS5	0x0000000002011450	571

Mnemonic	Address	Page
MBU.MBS.ECC01.MBMS6	0x0000000002011451	571
MBU.MBS.ECC01.MBMS7	0x0000000002011452	572
MBU.MBS.ECC01.MBRCEICRQ	0x000000000201145D	573
MBU.MBS.ECC01.MBSBS0	0x000000000201145E	574
MBU.MBS.ECC01.MBSBS1	0x000000000201145F	576
MBU.MBS.ECC01.MBSBS2	0x0000000002011460	579
MBU.MBS.ECC01.MBSBS3	0x0000000002011461	582
MBU.MBS.ECC01.MBSBS4	0x0000000002011462	585
MBU.MBS.ECC01.MBSBS5	0x0000000002011463	588
MBU.MBS.ECC01.MBSBS6	0x0000000002011464	591
MBU.MBS.ECC01.MBSBS7	0x0000000002011465	594
MBU.MBS.ECC01.MBSECCERR0	0x0000000002011466	597
MBU.MBS.ECC01.MBSECCERR1	0x0000000002011467	598
MBU.MBS.ECC01.MBSECCQ	0x000000000201144A	569
MBU.MBS.ECC01.MBSMSRQ	0x000000000201145C	572
MBU.MBS.ECC23.MBECCFIR	0x0000000002011480	598
MBU.MBS.ECC23.MBECCFIR_ACTION0	0x0000000002011486	600
MBU.MBS.ECC23.MBECCFIR_ACTION1	0x0000000002011487	600
MBU.MBS.ECC23.MBECCFIR_MASK	0x0000000002011483	600
MBU.MBS.ECC23.MBECCFIR_WOF	0x0000000002011488	601
MBU.MBS.ECC23.MBMMRQ	0x000000000201149B	604
MBU.MBS.ECC23.MBMS0	0x000000000201148B	602
MBU.MBS.ECC23.MBMS1	0x000000000201148C	602
MBU.MBS.ECC23.MBMS2	0x000000000201148D	602
MBU.MBS.ECC23.MBMS3	0x000000000201148E	603
MBU.MBS.ECC23.MBMS4	0x000000000201148F	603
MBU.MBS.ECC23.MBMS5	0x0000000002011490	603
MBU.MBS.ECC23.MBMS6	0x0000000002011491	603
MBU.MBS.ECC23.MBMS7	0x0000000002011492	604
MBU.MBS.ECC23.MBRCEICRQ	0x000000000201149D	605
MBU.MBS.ECC23.MBSBS0	0x000000000201149E	606
MBU.MBS.ECC23.MBSBS1	0x000000000201149F	608
MBU.MBS.ECC23.MBSBS2	0x00000000020114A0	611
MBU.MBS.ECC23.MBSBS3	0x00000000020114A1	614
MBU.MBS.ECC23.MBSBS4	0x00000000020114A2	617
MBU.MBS.ECC23.MBSBS5	0x00000000020114A3	620
MBU.MBS.ECC23.MBSBS6	0x00000000020114A4	623
MBU.MBS.ECC23.MBSBS7	0x00000000020114A5	626
MBU.MBS.ECC23.MBSECCERR0	0x00000000020114A6	629
MBU.MBS.ECC23.MBSECCERR1	0x00000000020114A7	630
MBU.MBS.ECC23.MBSECCQ	0x000000000201148A	601
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MBU.MBS.MBCCFGQ	0x000000000201140F	552
MBU.MBS.MBCDCPMQ	0x0000000002011410	554
MBU.MBS.MBCELOGQ	0x0000000002011416	558
MBU.MBS.MBCPRGQ	0x0000000002011414	557
MBU.MBS.MBCPRGSQ	0x0000000002011415	558
MBU.MBS.MBSACUMQ	0x0000000002011412	555
MBU.MBS.MBSCERR1Q	0x0000000002011413	555
MBU.MBS.MBSCERR2Q	0x000000000201142C	565
MBU.MBS.MBSCFGQ	0x0000000002011411	554

Mnemonic	Address	Page
MBU.MBS.MBSEINJQ	0x000000000201140E	550
MBU.MBS.MBSEMERTHROQ	0x000000000201142D	Error: Reference source not found
MBU.MBS.MBSIBERR0Q	0x000000000201141B	561
MBU.MBS.MBSIBERR1Q	0x000000000201141C	562
MBU.MBS.MBSIBWRSTATQ	0x000000000201141D	562
MBU.MBS.MBSOCC01HQ	0x0000000002011429	564
MBU.MBS.MBSOCC23HQ	0x000000000201142A	564
MBU.MBS.MBSOCCITCQ	0x0000000002011428	564
MBU.MBS.MBSOCCSCANQ	0x000000000201142B	564
MBU.MBS.MBSPMU0CFGQ	0x0000000002011418	559
MBU.MBS.MBSPMU0CNTQ	0x0000000002011419	560
MBU.MBS.MBSPMUSELQ	0x000000000201141A	561
MBU.MBS.MBSSQ	0x0000000002011417	559
MBU.MBS.MBS_FIR_ACTION0_REG	0x0000000002011406	544
MBU.MBS.MBS_FIR_ACTION1_REG	0x0000000002011407	544
MBU.MBS.MBS_FIR_MASK_REG	0x0000000002011403	542
MBU.MBS.MBS_FIR_REG	0x0000000002011400	540
MBU.MBS.MBS_FIR_WOF	0x0000000002011408	544
MBU.MBS.MCBISTS01.SCOMFIR.MBMPERQ	0x0000000002011662	675
MBU.MBS.MCBISTS01.SCOMFIR.MBNCERQ	0x0000000002011660	674
MBU.MBS.MCBISTS01.SCOMFIR.MBRCERQ	0x0000000002011661	675
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MBU.MBS.MCBISTS01.SCOMFIR.MBSEC1Q	0x0000000002011654	669
MBU.MBS.MCBISTS01.SCOMFIR.MBSEVRQ	0x000000000201165F	674
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MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA6	0x00000000020116C7	705
MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA7	0x00000000020116C8	705
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA0	0x00000000020116C9	706
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA1	0x00000000020116CA	706
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA2	0x00000000020116CB	706
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA3	0x00000000020116CC	706
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA4	0x00000000020116CD	707
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA5	0x00000000020116CE	707
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA6	0x00000000020116CF	707
MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA7	0x00000000020116D0	707
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA0	0x00000000020117B1	768
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA1	0x00000000020117B2	768
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA2	0x00000000020117B3	768
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA3	0x00000000020117B4	768
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA4	0x00000000020117B5	769
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA5	0x00000000020117B6	769
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA6	0x00000000020117B7	769
MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA7	0x00000000020117B8	769
MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA0	0x00000000020117B9	770
MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA1	0x00000000020117BA	770
MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA2	0x00000000020117BB	770
MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA3	0x00000000020117BC	770

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MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA5	0x00000000020117BE	771
MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA6	0x00000000020117BF	771
MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA7	0x00000000020117C0	771
MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA0	0x00000000020117C1	772
MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA1	0x00000000020117C2	772
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MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA3	0x00000000020117C4	772
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MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA6	0x00000000020117C7	773
MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA7	0x00000000020117C8	773
MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA0	0x00000000020117C9	774
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MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA2	0x00000000020117CB	774
MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA3	0x00000000020117CC	774
MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA4	0x00000000020117CD	775
MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA5	0x00000000020117CE	775
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MBU.MBX.MAINT0.MAINT_BUFF0_DATA1	0x000000000201160B	642
MBU.MBX.MAINT0.MAINT_BUFF0_DATA2	0x000000000201160C	642
MBU.MBX.MAINT0.MAINT_BUFF0_DATA3	0x000000000201160D	642
MBU.MBX.MAINT0.MAINT_BUFF0_DATA4	0x000000000201160E	643
MBU.MBX.MAINT0.MAINT_BUFF0_DATA5	0x000000000201160F	643
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MBU.MBX.MAINT0.MAINT_BUFF0_DATA7	0x0000000002011611	644
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MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC1	0x0000000002011613	644
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MBU.MBX.MAINT0.MAINT_BUFF1_DATA4	0x000000000201161E	648
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MBU.MBX.MAINT0.MAINT_BUFF1_DATA6	0x0000000002011620	648
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MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC0	0x0000000002011622	649
MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC1	0x0000000002011623	649
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MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC4	0x0000000002011626	650
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MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC6	0x0000000002011628	651

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MBU.MBX.MAINT0.MAINT_BUFF2_DATA1	0x000000000201162B	652
MBU.MBX.MAINT0.MAINT_BUFF2_DATA2	0x000000000201162C	652
MBU.MBX.MAINT0.MAINT_BUFF2_DATA3	0x000000000201162D	652
MBU.MBX.MAINT0.MAINT_BUFF2_DATA4	0x000000000201162E	653
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MBU.MBX.MAINT0.MAINT_BUFF2_DATA7	0x0000000002011631	654
MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC0	0x0000000002011632	654
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MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC1	0x000000000201164B	662
MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC2	0x000000000201164C	663
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MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC5	0x000000000201164F	666
MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC6	0x0000000002011650	667
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MBU.MBX.MAINT1.MAINT_BUFF0_DATA1	0x000000000201170B	710
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MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC1	0x0000000002011713	712

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MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC4	0x0000000002011736	723
MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC5	0x0000000002011737	723
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MBU.MBX.MAINT1.MAINT_BUFF3_DATA2	0x000000000201173C	725
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MBU.MBX.MAINT1.MAINT_BUFF3_DATA4	0x000000000201173E	725
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MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC1	0x0000000002011743	727
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MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC3	0x0000000002011745	728
MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC4	0x0000000002011746	728

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MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC1	0x000000000201174B	730
MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC2	0x000000000201174C	731
MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC3	0x000000000201174D	732
MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC4	0x000000000201174E	733
MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC5	0x000000000201174F	734
MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC6	0x0000000002011750	734
MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC7	0x0000000002011751	735
SCAC.SCAC_ACTIONMASK	0x00000000020115D3	639
SCAC.SCAC_ADDRMAP	0x00000000020115CD	637
SCAC.SCAC_CONFIG	0x00000000020115CE	637
SCAC.SCAC_DATA0_3	0x00000000020115CA	633
SCAC.SCAC_DATA4_7	0x00000000020115CB	634
SCAC.SCAC_ENABLE	0x00000000020115CC	636
SCAC.SCAC_ERRRPT	0x00000000020115D4	639
SCAC.SCAC_FIRACTION0	0x00000000020115C6	632
SCAC.SCAC_FIRACTION1	0x00000000020115C7	632
SCAC.SCAC_FIRMASK	0x00000000020115C3	632
SCAC.SCAC_FIRWOF	0x00000000020115C8	632
SCAC.SCAC_I2CMCTRL	0x00000000020115D1	638
SCAC.SCAC_LFIR	0x00000000020115C0	630
SCAC.SCAC_PIBTARGET	0x00000000020115D2	639
TCN.CC_ATOMIC_LOCK_REG	0x00000000020303FF	783
TCN.CC_PROTECT_MODE_REG	0x00000000020303FE	783
TCN.CLK_REGION	0x0000000002030006	780
TCN.CLOCK_STAT	0x0000000002030008	781
TCN.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000002040010	786
TCN.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000002040011	787
TCN.EPS.FIR.LOCAL_FIR_MASK	0x000000000204000D	786
TCN.EPS.FIR.MODE_REG	0x0000000002040008	785
TCN.EPS.FIR.SPATTN	0x0000000002040004	784
TCN.EPS.FIR.SPA_MASK	0x0000000002040007	785
TCN.EPS.PSC.ADDR_TRAP_REG	0x0000000002010003	459
TCN.EPS.PSC.ATOMIC_LOCK_REG	0x00000000020103FF	460
TCN.EPS.PSC.DEBUG_STATUS_REG	0x0000000002010004	459
TCN.EPS.PSC.PSCOM_ERROR_MASK	0x0000000002010002	458
TCN.EPS.PSC.PSCOM_MODE_REG	0x0000000002010000	456
TCN.EPS.PSC.PSCOM_STATUS_ERROR_REG	0x0000000002010001	457
TCN.EPS.PSC.PSCOM_WRITE_PROTECT_REG	0x0000000002010005	460
TCN.EPS.THERM.CONTROL_REG	0x0000000002050012	790
TCN.EPS.THERM.DTS_RESULT0	0x0000000002050000	787
TCN.EPS.THERM.DTS_TRC_RESULT	0x0000000002050003	787
TCN.EPS.THERM.ENC_CPM_RESULT0	0x0000000002050008	788
TCN.EPS.THERM.ERR_STATUS_REG	0x0000000002050013	791
TCN.EPS.THERM.INJECT_REG	0x0000000002050011	790
TCN.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000002050016	793
TCN.EPS.THERM.SKITTER_DATA0	0x0000000002050019	793
TCN.EPS.THERM.SKITTER_DATA1	0x000000000205001A	793

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TCN.EPS.THERM.SKITTER_DATA2	0x000000000205001B	793
TCN.EPS.THERM.SKITTER_FORCE_REG	0x0000000002050014	792
TCN.EPS.THERM.SKITTER_MODE_REG	0x0000000002050010	789
TCN.EPS.THERM.THERM_MODE_REG	0x000000000205000F	788
TCN.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000205001C	794
TCN.EPS.THERM.VOLT_MODE_REG	0x0000000002050015	792
TCN.EPS.THERM.VOLT_READ0	0x000000000205000B	788
TCN.ERROR_STATUS	0x0000000002030009	782
TCN.FIR_MASK	0x0000000002040002	784
TCN.GP0	0x0000000002000000	452
TCN.GP1	0x0000000002000001	454
TCN.GP2	0x0000000002000002	454
TCN.GP4	0x0000000002000003	455
TCN.GPIO_ATOMIC_LOCK_REG	0x00000000020003FF	456
TCN.GPIO_PROTECT_MODE_REG	0x00000000020003FE	456
TCN.LOCAL_FIR	0x000000000204000A	786
TCN.OPCG_REG0	0x0000000002030002	778
TCN.OPCG_REG1	0x0000000002030003	778
TCN.OPCG_REG2	0x0000000002030004	779
TCN.OPCG_REG3	0x0000000002030005	779
TCN.PHASE_SHADOW	0x0000000002030001	778
TCN.RFIR	0x0000000002040001	784
TCN.SCANSELQ	0x0000000002030007	780
TCN.SYNC_CONFIG	0x0000000002030000	777
TCN.TRA.MBITRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010C40	540
TCN.TRA.MBITRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010C41	540
TCN.TRA.MBS1TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002011880	776
TCN.TRA.MBS1TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002011881	776
TCN.TRA.MBS2TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x00000000020118C0	776
TCN.TRA.MBS2TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x00000000020118C1	776
TCN.XFIR	0x0000000002040000	783
TPTOP.NET.PCBSLNEST.ASSIST_INTERRUPT_REG	0x00000000020F0011	795
TPTOP.NET.PCBSLNEST.ATOMIC_LOCK_REG	0x00000000020F03FF	802
TPTOP.NET.PCBSLNEST.ATTN_INTERRUPT_REG	0x00000000020F001A	798
TPTOP.NET.PCBSLNEST.CLK_ADJ_REG	0x00000000020F0015	796
TPTOP.NET.PCBSLNEST.CLK_ADJ_SET	0x00000000020F0016	797
TPTOP.NET.PCBSLNEST.ERROR_REG	0x00000000020F001F	799
TPTOP.NET.PCBSLNEST.GP3_REG	0x00000000020F0012	796
TPTOP.NET.PCBSLNEST.HANG_PULSE_0_REG	0x00000000020F0020	800
TPTOP.NET.PCBSLNEST.HANG_PULSE_1_REG	0x00000000020F0021	800
TPTOP.NET.PCBSLNEST.HANG_PULSE_2_REG	0x00000000020F0022	800
TPTOP.NET.PCBSLNEST.HANG_PULSE_3_REG	0x00000000020F0023	801
TPTOP.NET.PCBSLNEST.HANG_PULSE_4_REG	0x00000000020F0024	801
TPTOP.NET.PCBSLNEST.HANG_PULSE_5_REG	0x00000000020F0025	801
TPTOP.NET.PCBSLNEST.HANG_PULSE_6_REG	0x00000000020F0026	801
TPTOP.NET.PCBSLNEST.HEARTBEAT_REG	0x00000000020F0018	797
TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_1	0x00000000020F0001	794
TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_2	0x00000000020F0002	794
TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_3	0x00000000020F0003	795
TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_4	0x00000000020F0004	795
TPTOP.NET.PCBSLNEST.PLL_LOCK_REG	0x00000000020F0019	797

Mnemonic	Address	Page
TPTOP.NET.PCBSLNEST.PRE_COUNTER_REG	0x00000000020F0028	802
TPTOP.NET.PCBSLNEST.PRIMARY_ADDRESS_REG	0x00000000020F0000	794
TPTOP.NET.PCBSLNEST.PROTECT_MODE_REG	0x00000000020F03FE	802
TPTOP.NET.PCBSLNEST.RECOV_INTERRUPT_REG	0x00000000020F001B	798
TPTOP.NET.PCBSLNEST.SLAVE_CONFIG_REG	0x00000000020F001E	798
TPTOP.NET.PCBSLNEST.TIMEOUT_REG	0x00000000020F0010	795
TPTOP.NET.PCBSLNEST.VITAL_SCAN_OUT	0x00000000020F0017	797
TPTOP.NET.PCBSLNEST.XSTOP_INTERRUPT_REG	0x00000000020F001C	798

The memory buffer registers are listed in the following tables.

Register Name	***GP Register 0***
Mnemonic	TCN.GP0
Address	0000000002000000 (PCB) 0000000002000004 (PCB1) 0000000002000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	TC_UNIT_ABSTCLK_MUXSEL_DC: Select ABIST clock source for Arrays on Chiplet Boundary. When set to 1, clocks where used from Chiplet with ABIST, Reset (0b0)
1	RWX	WOX_AND	WOX_OR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the sync clock for async latches (init value 1), Reset (0b1)
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC_OUT: Prevent plats from going into flush mode (init value 1), Reset (0b1)
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (init value 1, drop before dropping flushmode_inh), Reset (0b1)
4	RWX	WOX_AND	WOX_OR	TC_GPIO_AVP_MODE_DC_OUT: Enable AVP mode, Reset (0b0)
5	RWX	WOX_AND	WOX_OR	NOT_USED9: not used, Reset (0b0)
6	RWX	WOX_AND	WOX_OR	TC_GPIO_CC_SCAN_DIS_DC_B_OUT: Disable scan - set output of scan chain to zero, Reset (0b0)
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable Skitter measuring during Bist, Reset (0b0)
8	RWX	WOX_AND	WOX_OR	TC_GPIO_LBIST_EN_DC_OUT: LBIST mode, Reset (0b0)
9	RWX	WOX_AND	WOX_OR	TC_UNIT_LBIST_AC_MODE_DC: LBIST AC mode, Reset (0b0)
10	RWX	WOX_AND	WOX_OR	TC_UNIT_LBIST_ARY_WRT_THRU_DC: Array write-through mode - set Array in bypass mode, Reset (0b0)
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST, Reset (0b0)
12	RWX	WOX_AND	WOX_OR	TC_GPIO_ABIST_START_TEST_DC_OUT: Set to start ABIST testing, Reset (0b0)
13	RWX	WOX_AND	WOX_OR	NOT_USED0: not used, Reset (0b0)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
14	RWX	WOX_AND	WOX_OR	TC_UNIT_ATPG_EN_DC: ATPG mode, Reset (0b0)
15	RWX	WOX_AND	WOX_OR	TC_GPIO_SCAN_PROTECT_DC_OUT: Scan protection enable (init value 1), Reset (0b1)
16	RWX	WOX_AND	WOX_OR	NOT_USED1: not used, Reset (0b1)
17	RWX	WOX_AND	WOX_OR	NOT_USED2: not used, Reset (0b0)
18	RWX	WOX_AND	WOX_OR	NOT_USED3: not used, Reset (0b0)
19	RWX	WOX_AND	WOX_OR	TC_FENCE_EDRAM: Fence eDRAM, Reset (0b1)
20	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_START: Start trace to debug macros, Reset (0b0)
21	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_STOP: Stop trace to debug macros, Reset (0b0)
22	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_RESET: Reset trace to debug macros, Reset (0b0)
23	RWX	WOX_AND	WOX_OR	NOT_USED5: not used, Reset (0b0)
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio, Reset (0b0)
26	RWX	WOX_AND	WOX_OR	NOT_USED6: not used, Reset (0b0)
27	RWX	WOX_AND	WOX_OR	NOT_USED7: not used, Reset (0b0)
28:31	RWX	WOX_AND	WOX_OR	NOT_USED8: not used, Reset (0b0)
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7), Reset (0b0)
40:42	RWX	WOX_AND	WOX_OR	NOT_USED10: not used, Reset (0b0)
43:45	RWX	WOX_AND	WOX_OR	NOT_USED11: not used, Reset (0b0)
46	RWX	WOX_AND	WOX_OR	TC_PLLNSTIO_PADTEST_T_K: Wrap Sel for BSC, Reset (0b0)
47	RWX	WOX_AND	WOX_OR	TC_PLLNSTIO_PADTEST_C_K: Int Mode for BSC, Reset (0b0)
48	RWX	WOX_AND	WOX_OR	TC_UNIT_FENCE_RAM_DOUT_DC: LBIST: Fence RAM outputs for VCS=0, Reset (0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED13: not used, Reset (0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED14: not used, Reset (0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED15: not used, Reset (0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED16: not used, Reset (0b0)
53	RWX	WOX_AND	WOX_OR	NOT_USED17: not used, Reset (0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED18: not used, Reset (0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED19: not used, Reset (0b0)
56	RWX	WOX_AND	WOX_OR	NOT_USED20: not used, Reset (0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED21: not used, Reset (0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED22: not used, Reset (0b0)
59	RWX	WOX_AND	WOX_OR	TC_MBI_FENCE_EN_DC: fence off IO signals in MBI, Reset (0b0)
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: mask for pcb error (access or parity) in CC, Reset (0b0)
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: mask for pcb write while OPCG_IP / scan collision in CC, Reset (0b0)
62	RWX	WOX_AND	WOX_OR	TC_CC_LCC_EDGE_DELAYED_DC: Offset the clocking in the f domain by one cycle, Reset (0b1)
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (init value 1), Reset (0b1)

Register Name	*GP Register 1*
Mnemonic	TCN.GP1
Address	0000000002000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	REFR_ABIST_DONE: refr_abist_done, Reset (0)
1	ROX	MBS_ABIST_DONE: mbs_abist_done for 2:1, Reset (0)
2	ROX	MBI_ABIST_DONE: mbi_abist_done, Reset (0)
3	ROX	TRA_ABIST_DONE: tra_abist_done, Reset (0)
4	ROX	REFR_ABIST_DIAG: refr_abist_diag, Reset (0)
5	ROX	MBS_ABIST_DIAG: mbs_abist_diag, Reset (0)
6	ROX	NOT_USED27: not used, Reset (0)
7	ROX	NOT_USED28: not used, Reset (0)
8	ROX	NOT_USED29: not used, Reset (0)
9	ROX	NOT_USED30: not used, Reset (0)
10	ROX	NOT_USED31: not used, Reset (0)
11	ROX	NOT_USED32: not used, Reset (0)
12	ROX	NOT_USED33: not used, Reset (0)
13	ROX	NOT_USED34: not used, Reset (0)
14	ROX	NOT_USED35: not used, Reset (0)
15	ROX	TC_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs, Reset (0)
16	ROX	NOT_USED36: not used, Reset (0)
17	ROX	NOT_USED37: not used, Reset (0)
18	ROX	NOT_USED38: not used, Reset (0)
19	ROX	NOT_USED39: not used, Reset (0)
20	ROX	NOT_USED40: not used, Reset (0)
21	ROX	NOT_USED41: not used, Reset (0)
22	ROX	NOT_USED42: not used, Reset (0)
23	ROX	NOT_USED43: not used, Reset (0)

Register Name	*GP Register 2*
Mnemonic	TCN.GP2
Address	0000000002000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking

Register Name	*GP Register 4*
Mnemonic	TCN.GP4
Address	0000000002000003 (PCB) 0000000002000006 (PCB1) 0000000002000007 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select, Reset (0b000000)
6:7	RWX	WOX_AND	WOX_OR	NOT_USED44: not used, Reset (0b00)
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select, Reset (0b000000)
14:15	RWX	WOX_AND	WOX_OR	NOT_USED45: not used, Reset (0b00)
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select, Reset (0b000000)
22:23	RWX	WOX_AND	WOX_OR	NOT_USED46: not used, Reset (0b00)
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: Probe 3 select, Reset (0b000000)
30	RWX	WOX_AND	WOX_OR	NOT_USED47: not used, Reset (0b0)
31	RWX	WOX_AND	WOX_OR	TC_GP4_OFLOW_FEH_SEL_DC: ABIST: when 1, fail bit is overflow, otherwise its a fail, Reset (0b0)
32	RWX	WOX_AND	WOX_OR	NOT_USED48: not used, Reset (0b0)
33	RWX	WOX_AND	WOX_OR	NOT_USED49: not used, Reset (0b0)
34	RWX	WOX_AND	WOX_OR	NOT_USED50: not used, Reset (0b1)
35	RWX	WOX_AND	WOX_OR	NOT_USED51: not used, Reset (0b0)
36	RWX	WOX_AND	WOX_OR	NOT_USED52: not used, Reset (0b0)
37	RWX	WOX_AND	WOX_OR	NOT_USED53: not used, Reset (0b0)
38	RWX	WOX_AND	WOX_OR	NOT_USED54: not used, Reset (0b0)
39	RWX	WOX_AND	WOX_OR	NOT_USED55: not used, Reset (0b0)
40	RWX	WOX_AND	WOX_OR	NOT_USED56: not used, Reset (0b1)
41	RWX	WOX_AND	WOX_OR	NOT_USED57: not used, Reset (0b0)
42	RWX	WOX_AND	WOX_OR	NOT_USED58: not used, Reset (0b0)
43	RWX	WOX_AND	WOX_OR	NOT_USED59: not used, Reset (0b0)
44	RWX	WOX_AND	WOX_OR	NOT_USED60: not used, Reset (0b0)
45	RWX	WOX_AND	WOX_OR	NOT_USED61: not used, Reset (0b0)
46	RWX	WOX_AND	WOX_OR	NOT_USED62: not used, Reset (0b1)
47	RWX	WOX_AND	WOX_OR	NOT_USED63: not used, Reset (0b0)
48	RWX	WOX_AND	WOX_OR	NOT_USED64: not used, Reset (0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED65: not used, Reset (0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED66: not used, Reset (0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED67: not used, Reset (0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED68: not used, Reset (0b1)
53	RWX	WOX_AND	WOX_OR	NOT_USED69: not used, Reset (0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED70: not used, Reset (0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED71: not used, Reset (0b0)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
56	RWX	WOX_AND	WOX_OR	NOT_USED72: not used, Reset (0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED73: not used, Reset (0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED74: not used, Reset (0b1)
59	RWX	WOX_AND	WOX_OR	NOT_USED75: not used, Reset (0b0)
60	RWX	WOX_AND	WOX_OR	NOT_USED76: not used, Reset (0b0)
61	RWX	WOX_AND	WOX_OR	NOT_USED77: not used, Reset (0b0)
62	RWX	WOX_AND	WOX_OR	NOT_USED78: not used, Reset (0b0)
63	RWX	WOX_AND	WOX_OR	NOT_USED79: not used, Reset (0b0)

Register Name	***CC Protect Mode Register***
Mnemonic	TCN.GPIO_PROTECT_MODE_REG
Address	00000000020003FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_READ_PROTECT_ENABLE: Enable read protection
1	RW	GPIO_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TCN.GPIO_ATOMIC_LOCK_REG
Address	00000000020003FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	GPIO_ATOMIC_ID: Atomic ID

Register Name	***PSCOMLE Mode Register***
Mnemonic	TCN.EPS.PSC.PSCOM_MODE_REG
Address	0000000002010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: abort_on_PCB_addr_parity_error
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: abort_on_PCB_wdata_parity_error
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: abort_on_DL_return_P0_error
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: abort_on_DL_return_wdata_parity_error

Bits	PCB	Field Mnemonic: Description
4	RW	WATCHDOG_ENABLE: watchdog_enable
5:6	RW	SCOM_HANG_LIMIT: 0b11: 256, 0b10:512, 0b01:768, 0b00:1023
7	RW	FORCE_ALL_RINGS: set to logic 1 if all rings should be enable independent of ring address
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: fsm_selfreset_on_statevec_parityerror_enable
9:11	RW	RESERVED_PSCOM_MODE_LT: reserved

Register Name	***PSCOMLE Error Register***
Mnemonic	TCN.EPS.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000002010001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated_PCB_wdata_parity_error
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated_PCB_address_parity_error
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated_DL_return_wdata_parity_error
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated_DL_return_P0_error
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated_UL_rdata_parity_error
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated_UL_P0_error
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated_parity_error_on_interface_machine
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated_parity_error_on_p2s_machine
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated_timeout_while_waiting_for_ULCCH
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated_timeout_while_waiting_for_DLDCH_return
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated_timeout_while_waiting_for_ULDCH
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated_pscom_parallel_write_nvld
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated_pscom_parallel_read_nvld
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated_pscom_parallel_addr_invalid
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated_PCB_command_parity_error
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated_General_timeout
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated_satellite_acknowledge_access_violation
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated_satellite_acknowledge_invalid_register
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped_PCB_wdata_parity_error
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped_PCB_address_parity_error
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped_DL_return_wdata_parity_error
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped_DL_return_P0_error
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped_UL_rdata_parity_error

Bits	PCB	Field Mnemonic: Description
23	RWX	TRAPPED_UL_P0_ERROR: Trapped_UL_P0_error
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped_parity_error_on_interface_machine
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped_parity_error_on_p2s_machine
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped_timeout_while_waiting_for_ULCCH
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped_timeout_while_waiting_for_DLDCH_return
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped_timeout_while_waiting_for_ULDCH
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped_pscom_parallel_write_nvld
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped_pscom_parallel_read_nvld
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped_pscom_parallel_addr_invalid
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped_PCB_command_parity_error
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped_General_timeout
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped_satellite_acknowledge_access_violation
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped_satellite_acknowledge_invalid_register

Register Name	***PSCOMLE Error Mask Register***
Mnemonic	TCN.EPS.PSC.PSCOM_ERROR_MASK
Address	0000000002010002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: mask_PCB_wdata_parity_error
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: mask_PCB_address_parity_error
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: mask_DL_return_wdata_parity_error
3	RW	MASK_DL_RETURN_P0_ERROR: mask_DL_return_P0_error
4	RW	MASK_UL_RDATA_PARITY_ERROR: mask_UL_rdata_parity_error
5	RW	MASK_UL_P0_ERROR: mask_UL_P0_error
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: mask_parity_error_on_interface_machine
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: mask_parity_error_on_p2s_machine
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: mask_timeout_while_waiting_for_ULCCH
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: mask_timeout_while_waiting_for_DLDCH_return
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: mask_timeout_while_waiting_for_ULDCH
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: mask_pscom_parallel_write_nvld
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: mask_pscom_parallel_read_nvld
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: mask_pscom_parallel_addr_invalid
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: mask_PCB_command_parity_error
15	RW	MASK_GENERAL_TIMEOUT: mask_general_timeout
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: mask_satellite_acknowledge_access_violation

Bits	PCB	Field Mnemonic: Description
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: mask_satellite_acknowledge_invalid_register

Register Name	***PSCOMLE Address Trap Register***
Mnemonic	TCN.EPS.PSC.ADDR_TRAP_REG
Address	0000000002010003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB_address_of_last_transaction_with_error
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB_read_notwrite_of_last_transaction_with_error
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: reserved_0
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2Parallel_state_machine_at_time_of_error
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit: set to 1 if no parity error detected of Sat. No and Ack-bits
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: set if write parity error detected by satellite
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: set if invalid read or write access detected by satellite
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: set if invalid register address detected by satellite

Register Name	***Debug Status Register***
Mnemonic	TCN.EPS.PSC.DEBUG_STATUS_REG
Address	0000000002010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: local trace run
1:2	RWX	TRACE_STATE_LAT: trace state latch
3	RWX	TRACE_FREEZE: trace freeze
4:5	RWX	COND3_STATE_LT: condition 3 state latch
6:7	RWX	COND5_STATE_LT: condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: condition event history for condtition0_lt
9	RWX	HISTORY_CONDITION1_LT: condition event history for condtition1_lt
10	RWX	HISTORY_COND2_3_EVENT: condition event history for cond2_3_event
11	RWX	HISTORY_COND2_TIMEOUT: condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: reserved, set to zero

Register Name	*PSCOMLE Modewrite Protect Enable Register*
Mnemonic	TCN.EPS.PSC.PSCOM_WRITE_PROTECT_REG
Address	0000000002010005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_SERIAL_RING_WRITE_PROTECT: enable_serial_ring_write_protect
1	RW	RESERVED_WRITE_PROTECT: enable_serial_ring_write_protect

Register Name	*Atomic Lock Register*
Mnemonic	TCN.EPS.PSC.ATOMIC_LOCK_REG
Address	00000000020103FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	*Pervasive FIR Register*
Mnemonic	DMI.BUSCTL.SCOM.FIR_REG
Address	0000000002010400 (SCOM) 0000000002010401 (SCOM1) 0000000002010402 (SCOM2)
Attributes	
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A RX state machine parity or mode register parity error has occurred.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A TX state machine parity or mode register parity error has occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: FIR Register - The per-bus GCR ring hang detector error has occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus0. The bus is no longer capable of transferring data.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus4.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR Register- A SCOM FSM or FIR register parity error has occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR Register- A SCOM FSM or FIR register parity error has occurred.
50:63	RO	N/A	N/A	constant=0b00000000000000

Register Name	***Pervasive FIR Mask Register***
Mnemonic	DMI.BUSCTL.SCOM.FIR_MASK_REG
Address	0000000002010403 (SCOM) 0000000002010404 (SCOM1) 0000000002010405 (SCOM2)
Attributes	
Description	Error mask register (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked (1,x) = Checkstop Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask RX state machine parity or mode register parity error.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask TX state machine parity or mode register parity error.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR_MASK: FIR Register Mask - Mask GCR ring hang detector error.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7_MASK: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus0.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15_MASK: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus1.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23_MASK: FIR Register - Reserved.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus2.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31_MASK: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus3.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39_MASK: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus4.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47_MASK: FIR Register - Res47ved.
48	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: Internal SCOM Error Mask
49	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: Internal SCOM Error Mask Clone
50:63	RO	N/A	N/A	constant=0b00000000000000

Register Name	***Fault Isolation Action0 Register***
Mnemonic	DMI.BUSCTL.SCOM.FIR_ACTION0_REG
Address	0000000002010406 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION0: Action 0 for FIR(0:49)
50:63	RO	constant=0b00000000000000

Register Name	*Fault Isolation Action1 Register*
Mnemonic	DMI.BUSCTL.SCOM.FIR_ACTION1_REG
Address	0000000002010407 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION1: Action 1 for FIR(0:49)
50:63	RO	constant=0b00000000000000

Register Name	*FIR WOF Register*
Mnemonic	DMI.BUSCTL.SCOM.FIR_WOF_REG
Address	0000000002010408 (SCOM)
Attributes	
Description	FIR WOF Register

Bits	SCOM	Field Mnemonic: Description
0:49	RWX_WCLRREG	Reserved field. (Access type is WOF)
50:63	RO	constant=0b00000000000000

Register Name	*Normal SCOM Mode Reg*
Mnemonic	DMI.BUSCTL.SCOM.SCOM_MODE_PB
Address	0000000002010420 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	GCR_TEST_MODE: GCR Test Mode. Put register logic into GCR Test Mode which allows all RW registers to be read and written by diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers as well as the outputs from the logic. The outputs are gated to their scanflush value.
1	RWX	ENABLE_GCR_OFL_BUFF: Enables 2nd GCR overflow buffer, one is used by default

Bits	SCOM	Field Mnemonic: Description
2:7	RWX	IORESET_HARD_BUS0: IO Hard Reset Per-Bus and GCR Reset. Enables a Hard Reset on bus 0 through 5 (this is application dependent and bus 1-5 may not be present). A GCR reset affects all buses since any of them may be corrupted. 0b000000 = Functional (default) 0b100000 = Reset Bus 0 0b010000 = Reset Bus 1 0b001000 = Reset Bus 2 0b000100 = Reset Bus 3 0b000010 = Reset Bus 4 0b000001 = Reset Bus 5 0b111111 = Reset all local buses and perform a GCR reset.jfg Values: FUNCTIONAL=>0b000000 RESET0=>0b100000 RESET1=>0b010000 RESET2=>0b001000 RESET3=>0b000100 RESET4=>0b000010 RESET5=>0b000001 RESETGCR=>0b111111
8:10	RWX	GCR_HANG_DET_SEL: GCR hang detect threshold Select
11	ROX	GCR_BUFFER_ENABLED_RO_SIGNAL: 1 when 2nd GCR buffer is enabled
12	RWX	GCR_HANG_ERROR_MASK: Mask for GCR Hang error when 2nd buffer is enabled
13	RWX	GCR_HANG_ERROR_INJ: Inject for GCR Hang Error
14:21	RWX	SCOM_MODE_PB_SPARES: SCOM Mode Reg Spares
22:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***MBI Fault Isolation Register (MBIFIR)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIFIRQ
Address	0000000002010800 (SCOM) 0000000002010801 (SCOM1) 0000000002010802 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBIFIRQ_REPLAY_TIMEOUT: If 0 EDI channel is operational. If 1 Too many EDI replays due to CRC error. There is no forward progress for 5ms.
1	RWX	WOX_AND	WOX_OR	MBIFIRQ_CHANNEL_FAIL: If 0 EDI channel is operational. If 1 EDI channel is not operational. The channel can not be repaired. NOTE: Look at the EDI FIR for details. NOTE: This bit must be reset in the EDI phy.
2	RWX	WOX_AND	WOX_OR	MBIFIRQ_CRC_ERROR: If 0 No CRC errors detected. If 1 A CRC error was detected by receiver.
3	RWX	WOX_AND	WOX_OR	MBIFIRQ_FRAME_NOACK: If 0 All transmitted frames have been acknowledged. If 1 A transmitted frame did not get a Positive Acknowledge.
4	RWX	WOX_AND	WOX_OR	MBIFIRQ_SEQID_OUT_OF_ORDER: If 0 All received frames ID are in sequential order during non-replay transfer. If 1 Received frames ID are not in sequential order during non-replay transfer.
5	RWX	WOX_AND	WOX_OR	MBIFIRQ_REPLAY_BUFFER_ECC_CE: If 0 No ECC Correctable Error detected. If 1 An ECC Correctable Error was detected in the replay buffer.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RWX	WOX_AND	WOX_OR	MBIFIRQ_REPLAY_BUFFER_ECC_UE: If 0 No ECC Uncorrectable Error detected. If 1 An ECC Uncorrectable Error was detected in the replay buffer.
7	RWX	WOX_AND	WOX_OR	MBIFIRQ_MBI_STATE_MACHINE_TIMEOUT: If 1 An internal MBI state machine did not get a response within a programmable time interval.
8	RWX	WOX_AND	WOX_OR	MBIFIRQ_MBI_INTERNAL_CONTROL_PARITY_ERROR: If 1 An internal MBI state machine parity error was detected.
9	RWX	WOX_AND	WOX_OR	MBIFIRQ_MBI_DATA_FLOW_PARITY_ERROR: If '1' , a parity error was detected on the upstream data flow.
10	RWX	WOX_AND	WOX_OR	MBIFIRQ_CRC_PERFORMANCE_DEGRADATION: If '1' the EDI bus performance has degraded by 1% of the channel bandwidth.
11	RWX	WOX_AND	WOX_OR	MBIFIRQ_HOST_MC_GLOBAL_CHECKSTOP: If '1' the host memory controller has signaled a processor checkstop event across the EDI channel.
12	RWX	WOX_AND	WOX_OR	MBIFIRQ_HOST_MC_TRACESTOP: If '1' the host memory controller has signaled to the memory buffer, across the EDI channel to stop running its trace arrays.
13	RWX	WOX_AND	WOX_OR	MBIFIRQ_CHANNEL_INTERLOCK_FAIL: If '1' a CRC, NoAck, or sequence out of order error occurred during channel interlock
14	RWX	WOX_AND	WOX_OR	MBIFIRQ_HOST_MC_LOCAL_CHECKSTOP: If '1' the host memory controller has signaled a local processor checkstop event across the EDI channel.
15	RWX	WOX_AND	WOX_OR	MBIFIRQ_FRTL_CONTER_OVERFLOW: If '1' the FRTL counter has overflowed or wrapped around
16	RWX	WOX_AND	WOX_OR	MBIFIRQ_SCOM_REGISTER_PARITY_ERROR: Parity_Error on SCOM registers other than MBICFG
17	RWX	WOX_AND	WOX_OR	MBIFIRQ_IO_FAULT: IO to MBI Fault Line
18	RWX	WOX_AND	WOX_OR	MBIFIRQ_MULTIPLE_REPLAY: A replay event was detected while the transmitter was in replay.
19	RWX	WOX_AND	WOX_OR	MBIFIRQ_MBICFG_PARITY_SCOM_ERROR: MBICFG Parity SCOM Error
20	RWX	WOX_AND	WOX_OR	MBIFIRQ_BUFFER_OVERRUN_ERROR: Buffer_Overrun_Error
21	RWX	WOX_AND	WOX_OR	MBIFIRQ_RESERVED_1: Reserved_1
22	RWX	WOX_AND	WOX_OR	MBIFIRQ_RESERVED_2: Reserved_2
23	RWX	WOX_AND	WOX_OR	MBIFIRQ_RESERVED_3: Reserved_3
24	RWX	WOX_AND	WOX_OR	MBIFIRQ_RESERVED_4: Reserved_4
25	RWX	WOX_AND	WOX_OR	MBIFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
26	RWX	WOX_AND	WOX_OR	MBIFIRQ_INTERNAL_SCOM_ERROR_CLONE_COPY: Internal SCOM Error Clone copy
27:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000

Register Name	***MBI Fault Isolation Mask Register (MBIFIRMASK)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIFIRMASK
Address	0000000002010803 (SCOM) 0000000002010804 (SCOM1) 0000000002010805 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBIFIRMASK_REPLAY_TIMEOUT: Masks FIR(0)
1	RW	WO_AND	WO_OR	MBIFIRMASK_CHANNEL_FAIL: Masks FIR(1)
2	RW	WO_AND	WO_OR	MBIFIRMASK_CRC_ERROR: Masks FIR(2)
3	RW	WO_AND	WO_OR	MBIFIRMASK_FRAME_NOACK: Masks FIR(3)
4	RW	WO_AND	WO_OR	MBIFIRMASK_SEQID_OUT_OF_ORDER: Masks FIR(4)
5	RW	WO_AND	WO_OR	MBIFIRMASK_REPLAY_BUFFER_ECC_CE: Masks FIR(5)
6	RW	WO_AND	WO_OR	MBIFIRMASK_REPLAY_BUFFER_ECC_UE: Masks FIR(6)
7	RW	WO_AND	WO_OR	MBIFIRMASK_MBI_CHINIT_STATE_MACHINE_TIMEOUT: Masks FIR(7)
8	RW	WO_AND	WO_OR	MBIFIRMASK_MBI_INTERNAL_CONTROL_PARITY_ERROR: Masks FIR(8)
9	RW	WO_AND	WO_OR	MBIFIRMASK_MBI_DATA_FLOW_PARITY_ERROR: Masks FIR(9)
10	RW	WO_AND	WO_OR	MBIFIRMASK_CRC_PERFORMANCE_DEGRADATION: Masks FIR(10)
11	RW	WO_AND	WO_OR	MBIFIRMASK_HOST_MC_CHECKSTOP: Masks FIR(11)
12	RW	WO_AND	WO_OR	MBIFIRMASK_HOST_MC_TRACESTOP: Masks FIR(12)
13	RW	WO_AND	WO_OR	MBIFIRMASK_CHANNEL_INTERLOCK_FAIL: Masks FIR(13)
14	RW	WO_AND	WO_OR	MBIFIRMASK_HOST_MC_LOCAL_CHECKSTOP: Masks FIR(14)
15	RW	WO_AND	WO_OR	MBIFIRMASK_FRTL_COUNTER_OVERFLOW: Masks FIR(15)
16	RW	WO_AND	WO_OR	MBIFIRMASK_SCOM_REGISTER_PARITY_ERROR: Masks FIR(16)
17	RW	WO_AND	WO_OR	MBIFIRMASK_IO_FAULT: Masks FIR(17)
18	RW	WO_AND	WO_OR	MBIFIRMASK_MULTIPLE_REPLAY: Masks FIR(18)
19	RW	WO_AND	WO_OR	MBIFIRMASK_MBICFG_PARITY_SCOM_ERROR: Masks FIR(19)
20	RW	WO_AND	WO_OR	MBIFIRMASK_BUFFER_OVERRUN_ERROR: Masks FIR(20)
21	RW	WO_AND	WO_OR	MBIFIRMASK_RESERVED_1: Masks FIR(21)
22	RW	WO_AND	WO_OR	MBIFIRMASK_RESERVED_2: Masks FIR(22)
23	RW	WO_AND	WO_OR	MBIFIRMASK_RESERVED_3: Masks FIR(23)
24	RW	WO_AND	WO_OR	MBIFIRMASK_RESERVED_4: Masks FIR(24)
25	RW	WO_AND	WO_OR	MBIFIRMASK_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(25)
26	RW	WO_AND	WO_OR	MBIFIRMASK_INTERNAL_SCOM_ERROR_CLONE_COPY: Masks FIR(26)
27:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000

Register Name	***MBI Fault Isolation Action0 Register (MBIFIRACT0)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIFIRACT0
Address	0000000002010806 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:26	RW	MBIFIRACT0_ACTION_0: Action 0 for FIR(0:26)
27:63	RO	constant=0b00000000000000000000000000000000000000000

Register Name	***MBI Fault Isolation Action1 Register (MBIFIRACT1)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIFIRACT1
Address	0000000002010807 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:26	RW	MBIFIRACT1_ACTION_1: Action 1 for FIR(0:26)
27:63	RO	constant=0b00000000000000000000000000000000000000000

Register Name	***MBI Fault Isolation WOF Register (MBIFIRWOF)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIFIRWOF
Address	0000000002010808 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRREG	MBIFIRWOF_REPLAY_TIMEOUT: Who's On First (WOF0) Register
1	RWX_WCLRREG	MBIFIRWOF_CHANNEL_FAIL: Who's On First (WOF1) Register
2	RWX_WCLRREG	MBIFIRWOF_CRC_ERROR: Who's On First (WOF2) Register
3	RWX_WCLRREG	MBIFIRWOF_FRAME_NOACK: Who's On First (WOF3) Register
4	RWX_WCLRREG	MBIFIRWOF_SEQID_OUT_OF_ORDER: Who's On First (WOF4) Register
5	RWX_WCLRREG	MBIFIRWOF_REPLAY_BUFFER_ECC_CE: Who's On First (WOF5) Register
6	RWX_WCLRREG	MBIFIRWOF_REPLAY_BUFFER_ECC_UE: Who's On First (WOF6) Register
7	RWX_WCLRREG	MBIFIRWOF_MBI_STATE_MACHINE_TIMEOUT: Who's On First (WOF7) Register
8	RWX_WCLRREG	MBIFIRWOF_MBI_INTERNAL_CONTROL_PARITY_ERROR: Who's On First (WOF8) Register

Bits	SCOM	Field Mnemonic: Description
9	RWX_WCLRREG	MBIFIRWOF_MBI_DATA_FLOW_PARITY_ERROR: Who's On First (WOF9) Register
10	RWX_WCLRREG	MBIFIRWOF_CRC_PERFORMANCE_DEGRADATION: Who's On First (WOF10) Register
11	RWX_WCLRREG	MBIFIRWOF_HOST_MC_GLOBAL_CHECKSTOP: Who's On First (WOF11) Register
12	RWX_WCLRREG	MBIFIRWOF_HOST_MC_TRACESTOP: Who's On First (WOF12) Register
13	RWX_WCLRREG	MBIFIRWOF_CHANNEL_INTERLOCK_FAIL: Who's On First (WOF13) Register
14	RWX_WCLRREG	MBIFIRWOF_HOST_MC_LOCAL_CHECKSTOP: Who's On First (WOF14) Register
15	RWX_WCLRREG	MBIFIRWOF_FRTL_CONTER_OVERFLOW: Who's On First (WOF15) Register
16	RWX_WCLRREG	MBIFIRWOF_SCOM_REGISTER_PARITY_ERROR: Who's On First (WOF16) Register
17	RWX_WCLRREG	MBIFIRWOF_IO_FAULT: Who's On First (WOF17) Register
18	RWX_WCLRREG	MBIFIRWOF_MULTIPLE_REPLAY: Who's On First (WOF18) Register
19	RWX_WCLRREG	MBIFIRWOF_MBICFG_PARITY_SCOM_ERROR: Who's On First (WOF19) Register
20	RWX_WCLRREG	MBIFIRWOF_BUFFER_OVERRUN_ERROR: Who's On First (WOF20) Register
21:24	RWX_WCLRREG	MBIFIRWOF_RESERVED_21_24: Reserved
25	RWX_WCLRREG	MBIFIRWOF_INTERNAL_SCOM_ERROR_CLONE: Who's On First (WOF25) Register
26	RWX_WCLRREG	MBIFIRWOF_INTERNAL_SCOM_ERROR_CLONE_COPY: Who's On First (WOF26) Register
27:63	RO	constant=0b00000000000000000000000000000000000000000

Register Name	***MBI Configuration Register (MBICFG)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBICFGQ
Address	000000000201080A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBICFGQ_FORCE_CHANNEL_FAIL: If '1' the MBI will enter the channel fail state
1	RW	MBICFGQ_REPLAY_CRC_DISABLE: If 0 EDI frames will be replayed, by the transmitter, when a frame crc error is detected. If 1 EDI frames will not be replayed, by the transmitter, when a frame crc error occurs.
2	RW	MBICFGQ_REPLAY_NOACK_DISABLE: If 0 EDI frames will be replayed, by the transmitter, when the frame does not get acknowledged when the FRTL timer expires. If 1 EDI frames will not be replayed, by the transmitter, when the frame does not get acknowledged when the FRTL timer expires.
3	RW	MBICFGQ_REPLAY_OUTOFORDER_DISABLE: If 0 EDI frames will be replayed, by the transmitter, when an out-of-order Sequence ID is detected. If 1 EDI frames will not be replayed, by the transmitter, when an out-of-order Sequence ID is detected.

Bits	SCOM	Field Mnemonic: Description
4	RWX	MBICFGQ_FORCE_LFSR_REPLAY: If 1 EDI frames are replayed from the replay buffer when an LFSR pulse is detected by the replay controller. Setting this bit will result in multiple frame replays.
5	RW	MBICFGQ_CRC_CHECK_DISABLE: If 0 EDI frames will be checked for CRC errors. If 1 EDI frames will not be checked for CRC errors.
6	RW	MBICFGQ_ECC_CHECK_DISABLE: If 0 EDI frames, from the replay buffer, will be checked for ECC errors. If 1 EDI frames, from the replay buffer, will not be checked for ECC errors.
7	RWX	MBICFGQ_FORCE_FRAME_LOCK: If 1 Force EDI frame start generation. Note: This feature is meant to be used in a standalone memory buffer debug verification environment. An attached chip will not function properly if this bit is set. Normally, this process should be initiated from the host processor.
8	RWX	MBICFGQ_FORCE_FRTL: If 1 Frame Round Trip Latency (FRTL) will be calculated. Note: This feature is meant to be used in a standalone memory buffer debug verification environment. An attached chip will not function properly if this bit is set. Normally, this process should be initiated from the host processor.
9	RW	MBICFGQ_AUTO_FRTL_DISABLE: If 0 Frame Round Trip Latency of EDI frames will automatically be generated by hardware. If 1 Disable the automatic calculation of EDI Frame Round Trip Latency by hardware. This bit should be set when the FRTL value is set manually in bits 10:16.
10:16	RW	MBICFGQ_MANUAL_FRTL_VALUE: This 7-bit value represents the Frame Round Trip Latency of the memory channel. It measures the delay from when a EDI frame is launched to when the corresponding acknowledge bit is received by the initiator. Value Delay 0000000 No Delay 0000001 1 - 2.4 GHz cycle - - - 1111110 126 - 2.4 GHz cycles 1111111 127 - 2.4 GHz cycles Note: This value is used only when bit 9 of mbicfgq is a 1. Note: Both the memory buffer and the host MC must be set up similarly in either auto or manual mode.
17	RW	MBICFGQ_MANUAL_FRTL_DONE: If 1 the manual Frame Round Trip Latency (FRTL) value has been set by software. Note: This bit must be set, when in manual FRTL mode, to complete channel initialization.
18	RW	MBICFGQ_ECC_CORRECT_DISABLE: If 0 EDI frames, from the replay buffer, will be corrected for ECC Correctable Errors. If 1 EDI frames, from the replay buffer, will not be corrected for ECC Correctable Errors.
19	RW	MBICFGQ_SPARE1: Reserved
20	RW	MBICFGQ_LANE_VOTING_BYPASS: If 0 Bad lane vote is automatically generated by hardware when a crc error is detected. If 1 Force a one shot bad lane vote. Allows firmware to bypass the hardware lane voting algorithm.
21:25	RW	MBICFGQ_BAD_LANE_VALUE: Value Bad Lane 00000 Lane 0 00001 Lane 1 00010 Lane 2 - - - 10011 Lane 19 10100 Lane 20 Note: memory buffer attached chips have 14 downstream lanes and 21 upstream lanes.
26	RW	MBICFGQ_BAD_LANE_VOTING_DISABLE: If 1 the automatic bad lane voting by the hardware algorithm is disabled.
27:32	RW	MBICFGQ_NO_FORWARD_PROGRESS_TIMEOUT_VALUE: Value Timeout 000000 No Timeout - - 001001 1 ms - - 101101 5 ms - 111111 7 ms Formula: Timeout = 0.109 * DEC(Value) The Timeout term above is in milliseconds. The smallest timeout value is 109 microseconds.
33:34	RW	MBICFGQ_PERFORMANCE_DEGRADATION_PERCENT_SELECT: Value Timeout 00 1% 01 2% 10 3% 11 4%
35:36	RW	MBICFGQ_CHANNEL_INITIALIZATION_STATE_MACHINE_TIMEOUT_VALUE: Value Timeout 00 No Timeout 01 3us 10 7us 11 14us
37	RW	MBICFGQ_MBI_RESET_KEEPER: Writing this bit to a 1 will pulse the reset of the hold latches in the MBI c_err_rpt macros
38	RW	MBICFGQ_FAULT_LINE_ERROR_ENABLE: If 1, the fault line error generation is enabled.
39:43	RW	MBICFGQ_SPARE3: Reserved
44:63	RO	constant=0b00000000000000000000

Register Name	*MBI Status Register (MBISTAT)*
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBISTATQ
Address	000000000201080B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBISTATQ_FRAME_LOCK_PASS: If 1 Frame Lock completed successfully. A CRC error does not prevent complete status, unless it leads to a timeout.
1	RWX	MBISTATQ_FRAME_LOCK_FAIL: If 1 Frame Lock Failed and did not complete. This is caused by timeouts in frame lock state machine.
2	RWX	MBISTATQ_FRTL_PASS: If 1 Frame Round Trip Latency completed successfully. A CRC error does not prevent complete status, unless it leads to a timeout.
3	RWX	MBISTATQ_FRTL_FAIL: If 1 Frame Round Trip Latency Failed and did not complete. This is caused by timeouts in FRTL state machine.
4	ROX	MBISTATQ_REPLAY_IN_PROGRESS: If 0 Normal EDI frame transfer. If 1 EDI frames are getting replayed due to errors.
5:11	ROX	MBISTATQ_OPERATING_FRTL_VALUE: This 7-bit value represents the current Frame Round Trip Latency.
12	ROX	MBISTATQ_DMI_EDI_FENCE: If 0 The EDI is operational. MBI starts listening to the channel, on the falling edge of the fence signal. If 1 The EDI is fenced from the MBI.
13	RWX	MBISTATQ_CHAN_INTERLOCK_PASS: If '1' Channel Interlock completed successfully
14	RWX	MBISTATQ_CHAN_INTERLOCK_FAIL: If '1' Channel Interlock failed and did not complete
15	RWX	MBISTATQ_SPARE0: Reserved.
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*MBI CRC Syndromes Register (MBICRCSYN)*
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBICRCSYNQ
Address	000000000201080C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBICRCSYNQ_VALID: If 1 the CRC syndrome is valid.
1	RWX	MBICRCSYNQ_FIRST: If 0, continuously capture the crc syndrome when a crc error occurs. If 1, only capture the crc syndrome for the first crc error.
2	RWX	MBICRCSYNQ_AUTO_RESET_DISABLE: If 0, reset the crc syndrome register when MBICRCSYNQ is read. If 1, do not clear the crc syndrome register when MBICRCSYNQ is read.
3:27	RWX	MBICRCSYNQ_DS_SYNDROME: 25-bit Downstream CRC syndrome logged when a crc error is detected.
28:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***MBI Error Inject Register (MBIERRINJ)***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIERRINJQ
Address	000000000201080D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBIERRINJQ_FRAME_CRC_ERROR_INJECT_MODE: Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
1	RW	MBIERRINJQ_FRAME_CRC_ERROR_INJECT: If 0 A frame CRC error will not be injected. If 1 A frame CRC error is injected .
2	RW	MBIERRINJQ_REPLAY_BUFFER_ERROR_INJECT_MODE: Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	MBIERRINJQ_REPLAY_BUFFER_ECC_CE_INJECT: If 0 A Correctable ECC error will not be injected in the replay buffer. If 1 A Correctable ECC error is injected into the replay buffer.
4	RW	MBIERRINJQ_REPLAY_BUFFER_ECC_UE_INJECT: If 0 An uncorrectable ECC error will not be injected in the replay buffer. If 1 An uncorrectable ECC error will be injected in the replay buffer.
5	RW	MBIERRINJQ_DATA_FLOW_PARITY_ERROR_INJECT_MODE: Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
6	RW	MBIERRINJQ_DATA_FLOW_PARITY_ERROR_INJECT: If 0 A data flow parity error will not be injected. If 1 A data flow parity error is injected .
7	RW	MBIERRINJQ_DEAD_FRAME_CRC_ERROR_INJECT: If 0 A dead frame CRC error will not be injected. If 1 A dead frame CRC error is injected .
8:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***Memory Buffer FPGA Interrupt Register***
Mnemonic	MBU.MBI.MBI.SCOMFIR.MBIFPGAINTRQ
Address	000000000201080E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBIFPGAINTRQ_FPGA_INTERRUPT_ENABLE: If 0 This memory buffer FPGA interrupt register must be polled by software. If 1 FPGA Interrupts are sent, in the upstream EDI frames, to the host MC .
1	RWX	MBIFPGAINTRQ_FPGA_INTERRUPT_TRIGGER: If 0 there is no memory buffer FPGA interrupt pending. If 1 memory buffer FPGA interrupt is pending.
2	RW	MBIFPGAINTRQ_FPGA_INTERRUPT_FENCE_DISABLE: If 0 FPGA interrupt line is blocked from sending interrupts. If 1 FPGA interrupt line can cause interrupts.
3:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*MBI Error Report Register 0 (MBIERPT0)*
Mnemonic	MBU.MBI.MBI.MBIERPT0
Address	000000000201080F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RO	constant=0b0
1	ROX	MBIERPT0_MBISTAT_PARITY_ERROR: MBISTAT Register Parity Error, FIR(16)
2	ROX	MBIERPT0_MBICRCSYN_PARITY_ERROR: MBICRCSYN Register Parity Error, FIR(16)
3	ROX	MBIERPT0_MBIERRINJ_PARITY_ERROR: MBIERRINJ Register Parity Error, FIR(16)
4	ROX	MBIERPT0_MBIFPGAINTR_PARITY_ERROR: MBIFPGAINTR Register Parity Error, FIR(16)
5:10	RO	constant=0b000000
11	ROX	MBIERPT0_CRCG_DATAFLOW_PARITY_ERROR: CRCG dataflow parity error, FIR(9)
12	RO	constant=0b0
13	ROX	MBIERPT0_ECCG_DATAFLOW_PARITY_ERROR: ECCG dataflow parity error, FIR(9)
14:16	RO	constant=0b000
17	ROX	MBIERPT0_US_CHINIT_READY_TIMEOUT_ERROR: US Chinit Ready Timeout Error, FIR(7)
18	ROX	MBIERPT0_DS_FRAME_START_TIMEOUT_ERROR: DS Frame Start Timeout Error, FIR(7)
19	ROX	MBIERPT0_DS_NULL_PACKET_TIMEOUT_ERROR: DS Null Packet Timeout Error, FIR(7)
20	ROX	MBIERPT0_DS_ACK_PACKET_TIMEOUT_ERROR: DS Ack packet Timeout Error, FIR(7)
21	RO	constant=0b0
22	ROX	MBIERPT0_FRTL_SM_PARITY_ERROR: FRTL SM Parity Error, FIR(8)
23	ROX	MBIERPT0_FL_SM_PARITY_ERROR: FL SM Parity Error, FIR(8)
24	ROX	MBIERPT0_GLOBAL_SM_PARITY_ERROR: Global SM Parity Error, FIR(8)
25	ROX	MBIERPT0_REPLAY0_SM_PARITY_ERROR: Replay0 SM Parity Error, FIR(8))
26	ROX	MBIERPT0_REPLAY1_SM_PARITY_ERROR: Replay1 SM Parity Error, FIR(8))
27	ROX	MBIERPT0_REPLAY2_SM_PARITY_ERROR: Replay2 SM Parity Error, FIR(8)
28	ROX	MBIERPT0_REPLAY3_SM_PARITY_ERROR: Replay3 SM Parity Error, FIR(8)
29	ROX	MBIERPT0_REPLAY4_SM_PARITY_ERROR: Replay4 SM Parity Error, FIR(8)
30	ROX	MBIERPT0_REPLAY5_SM_PARITY_ERROR: Replay5 SM Parity Error, FIR(8)
31	ROX	MBIERPT0_REPLAY6_SM_PARITY_ERROR: Replay6 SM Parity Error, FIR(8)
32	RW	MBIERPT0_REPLAY7_SM_PARITY_ERROR: Replay7 SM Parity Error, FIR(8)
33	ROX	MBIERPT0_REPLAY8_SM_PARITY_ERROR: Replay8 SM Parity Error, FIR(8)
34	ROX	MBIERPT0_REPLAY9_SM_PARITY_ERROR: Replay9 SM Parity Error, FIR(8)
35	ROX	MBIERPT0_REPLAY10_SM_PARITY_ERROR: Replay10 SM Parity Error, FIR(8)
36	ROX	MBIERPT0_REPLAY11_SM_PARITY_ERROR: Replay11 SM Parity Error, FIR(8)
37	ROX	MBIERPT0_REPLAY12_SM_PARITY_ERROR: Replay12 SM Parity Error, FIR(8)
38	ROX	MBIERPT0_REPLAY13_SM_PARITY_ERROR: Replay13 SM Parity Error, FIR(8)
39	ROX	MBIERPT0_REPLAY14_SM_PARITY_ERROR: Replay14 SM Parity Error, FIR(8)
40	ROX	MBIERPT0_REPLAY15_SM_PARITY_ERROR: Replay15 SM Parity Error, FIR(8)
41	ROX	MBIERPT0_REPLAY16_SM_PARITY_ERROR: Replay16 SM Parity Error, FIR(8)

Bits	SCOM	Field Mnemonic: Description
42	ROX	MBIERPT0_REPLAY17_SM_PARITY_ERROR: Replay17 SM Parity Error, FIR(8)
43	ROX	MBIERPT0_REPLAY18_SM_PARITY_ERROR: Replay18 SM Parity Error, FIR(8)
44	ROX	MBIERPT0_REPLAY19_SM_PARITY_ERROR: Replay19 SM Parity Error, FIR(8)
45	ROX	MBIERPT0_REPLAY20_SM_PARITY_ERROR: Replay20 SM Parity Error, FIR(8)
46	ROX	MBIERPT0_REPLAY21_SM_PARITY_ERROR: Replay21 SM Parity Error, FIR(8)
47	ROX	MBIERPT0_REPLAY22_SM_PARITY_ERROR: Replay22 SM Parity Error, FIR(8)
48	ROX	MBIERPT0_REPLAY23_SM_PARITY_ERROR: Replay23 SM Parity Error, FIR(8)
49	ROX	MBIERPT0_REPLAY24_SM_PARITY_ERROR: Replay24 SM Parity Error, FIR(8)
50	ROX	MBIERPT0_REPLAY25_SM_PARITY_ERROR: Replay25 SM Parity Error, FIR(8)
51	ROX	MBIERPT0_REPLAY26_SM_PARITY_ERROR: Replay26 SM Parity Error, FIR(8)
52	ROX	MBIERPT0_REPLAY27_SM_PARITY_ERROR: Replay27 SM Parity Error, FIR(8)
53	ROX	MBIERPT0_REPLAY28_SM_PARITY_ERROR: Replay28 SM Parity Error, FIR(8)
54	ROX	MBIERPT0_REPLAY29_SM_PARITY_ERROR: Replay29 SM Parity Error, FIR(8)
55	ROX	MBIERPT0_REPLAY30_SM_PARITY_ERROR: Replay30 SM Parity Error, FIR(8)
56	ROX	MBIERPT0_REPLAY31_SM_PARITY_ERROR: Replay31 SM Parity Error, FIR(8)
57:63	RO	constant=0b0000000

Register Name	***FBIST NEST FIR Register***
Mnemonic	FBIST.FBN.FBN_FIR_REG
Address	0000000002010880 (SCOM) 0000000002010881 (SCOM1) 0000000002010882 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_SCOM_UE: Config reg parity error
1	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_USCHK_1HOT: Upstream Checker state machine one hot error
2	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_USCHK_DATA_DROP: Upstream Checker dropped data
3	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_DGEN_1HOT: Downstream data generation state machine one hot error
4	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_CMD_1HOT: Command control state machine one hot error
5	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_CMD_EARLY_RESPONSE: Command state machine received upstream response too early
6	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_FBIST_FAIL: Fbist run fail
7	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_FBN_US_CRC_ERR: MBI to FBISTN upstream CRC error
8:14	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_RESERVED_8_14: Reserved_8_14
15	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_INTERNAL_SCOM_ERROR: Internal Scom Error
16	RWX	WOX_AND	WOX_OR	FBN_FIR_REG_INTERNAL_SCOM_ERROR_CLONE: Internal Som Error Clone

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*FBIST NEST FIR Mask Register*
Mnemonic	FBIST.FBN.FBN_FIR_MASK_REG
Address	0000000002010883 (SCOM) 0000000002010884 (SCOM1) 0000000002010885 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_SCOM_UE: Masks FIR(0)
1	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_USCHK_1HOT: Masks FIR(1)
2	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_USCHK_DATA_DROP: Masks FIR(2)
3	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_DGEN_1HOT: Masks FIR(3)
4	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_CMD_1HOT: Masks FIR(4)
5	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_CMD_EARLY_RESPONSE: Masks FIR(5)
6	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_FBIST_FAIL: Masks FIR(6)
7	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_FBN_US_CRC_ERR: Masks FIR(7)
8:14	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_RESERVED_8_14: Reserved_8_14
15	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_INTERNAL_SCOM_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	FBN_FIR_MASK_REG_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(16)
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*FBIST NEST FIR Action 0 Register*
Mnemonic	FBIST.FBN.FBN_FIR_ACTION0_REG
Address	0000000002010886 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	FBN_FIR_ACTION0_REG_FBN_SCOM_UE: Action 0 FIR(0)
1	RW	FBN_FIR_ACTION0_REG_FBN_USCHK_1HOT: Action 0 FIR(1)
2	RW	FBN_FIR_ACTION0_REG_FBN_USCHK_DATA_DROP: Action 0 FIR(2)
3	RW	FBN_FIR_ACTION0_REG_FBN_DGEN_1HOT: Action 0 FIR(3)
4	RW	FBN_FIR_ACTION0_REG_FBN_CMD_1HOT: Action 0 FIR(4)
5	RW	FBN_FIR_ACTION0_REG_FBN_CMD_EARLY_RESPONSE: Action 0 FIR(5)
6	RW	FBN_FIR_ACTION0_REG_FBN_FBIST_FAIL: Action 0 FIR(6)
7	RW	FBN_FIR_ACTION0_REG_FBN_US_CRC_ERR: Action 0 FIR(7)
8:14	RW	FBN_FIR_ACTION0_REG_RESERVED_8_14: Reserved_8_14
15	RW	FBN_FIR_ACTION0_REG_INTERNAL_SCOM_ERROR: Action 0 FIR(15)

Bits	SCOM	Field Mnemonic: Description
16	RW	FBN_FIR_ACTION0_REG_INTERNAL_SCOM_ERROR_CLONE: Action 0 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*FBIST NEST FIR Action 1 Register*
Mnemonic	FBIST.FBN.FBN_FIR_ACTION1_REG
Address	0000000002010887 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	FBN_FIR_ACTION1_REG_FBN_SCOM_UE: Action 1 FIR(0)
1	RW	FBN_FIR_ACTION1_REG_FBN_USCHK_1HOT: Action 1 FIR(1)
2	RW	FBN_FIR_ACTION1_REG_FBN_USCHK_DATA_DROP: Action 1 FIR(2)
3	RW	FBN_FIR_ACTION1_REG_FBN_DGEN_1HOT: Action 1 FIR(3)
4	RW	FBN_FIR_ACTION1_REG_FBN_CMD_1HOT: Action 1 FIR(4)
5	RW	FBN_FIR_ACTION1_REG_FBN_CMD_EARLY_RESPONSE: Action 1 FIR(5)
6	RW	FBN_FIR_ACTION1_REG_FBN_FBIST_FAIL: Action 1 FIR(6)
7	RW	FBN_FIR_ACTION1_REG_FBN_US_CRC_ERR: Action 1 FIR(7)
8:14	RW	FBN_FIR_ACTION1_REG_RESERVED_8_14: Reserved_8_14
15	RW	FBN_FIR_ACTION1_REG_INTERNAL_SCOM_ERROR: Action 1 FIR(15)
16	RW	FBN_FIR_ACTION1_REG_INTERNAL_SCOM_ERROR_CLONE: Action 1 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*FBIST Nest Control Register*
Mnemonic	FBIST.FBN.FBNCNTL
Address	000000000201088A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	FBNCNTL_FBIST_START: Self Resetting Bit FBIST_MODE must also be set to 1 at the same time This will reset all cmd state machines, address and data. Start fbist from the beginning. Values: RESET=>0b0 START_FBIST_RUN=>0b1
1	RWX	FBNCNTL_FBIST_STOP: Self resetting bit Will stop the FBIST run after the next command completes. FBIST will continue to send idle commands while FBIST_MODE remains 1. This allows the current test to be paused and restarted with FBIST_CONT. Or the user defined commands can be reprogrammed and FBIST can start over with FBIST_START being set to 1. Values: RESET=>0b0 STOP_FBIST_RUN=>0b1
2:4	RWX	FBNCNTL_RESERVED_2_4: reserved
5	RWX	FBNCNTL_FBIST_MODE: Must be set to one when FBIST_START is set to 1. Will remain on until set to 0 by the user. This controls the FBIST mode bit and fbist to mbi fence signal.

Bits	SCOM	Field Mnemonic: Description
6	RWX	FBNCNTL_FBIST_CONT: When set to one, allows an FBIST test which has been stopped to continue from where it left off. Values: DEFAULT=>0b0 CONTINUE_FBIST_RUN=>0b1
7	RWX	FBNCNTL_FBIST_STEP: When set to one. FBIST will issue the next command and then pause Values: DEFAULT=>0b0 NOT_YET_FUNCTIONAL=>0b1
8:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000 Values: DEFAULT=>0b0 NOT_YET_FUNCTIONAL=>0b1

Register Name	***FBIST Nest Memory Registers 0***
Mnemonic	FBIST.FBN.FBNMR0
Address	0000000002010888 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR0_CFG_FBN_CMD0: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR0_CFG_FBN_CMD0_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR0_CFG_FBN_CMD0_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
8:11	RW	FBNMR0_CFG_FBN_CMD0_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBNMR0_CFG_FBN_CMD0_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR0_CFG_FBN_CMD0_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR0_CFG_FBN_CMD0_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR0_CFG_FBN_CMD0_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR0_CFG_FBN_CMD1: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR0_CFG_FBN_CMD1_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR0_CFG_FBN_CMD1_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
24:27	RW	FBNMR0_CFG_FBN_CMD1_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR0_CFG_FBN_CMD1_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBNMR0_CFG_FBN_CMD1_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR0_CFG_FBN_CMD1_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR0_CFG_FBN_CMD1_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR0_CFG_FBN_CMD2: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR0_CFG_FBN_CMD2_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR0_CFG_FBN_CMD2_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
40:43	RW	FBNMR0_CFG_FBN_CMD2_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR0_CFG_FBN_CMD2_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR0_CFG_FBN_CMD2_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBNMR0_CFG_FBN_CMD2_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR0_CFG_FBN_CMD2_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR0_CFG_FBN_CMD3: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR0_CFG_FBN_CMD3_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR0_CFG_FBN_CMD3_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
56:59	RW	FBNMR0_CFG_FBN_CMD3_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR0_CFG_FBN_CMD3_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR0_CFG_FBN_CMD3_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBNMR0_CFG_FBN_CMD3_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR0_CFG_FBN_CMD3_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Memory Registers 1***
Mnemonic	FBIST.FBN.FBNMR1
Address	000000000201088C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR1_CFG_FBN_CMD4: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
4:5	RW	FBNMR1_CFG_FBN_CMD4_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR1_CFG_FBN_CMD4_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR1_CFG_FBN_CMD4_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBNMR1_CFG_FBN_CMD4_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR1_CFG_FBN_CMD4_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR1_CFG_FBN_CMD4_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR1_CFG_FBN_CMD4_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR1_CFG_FBN_CMD5: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
20:21	RW	FBNMR1_CFG_FBN_CMD5_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR1_CFG_FBN_CMD5_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR1_CFG_FBN_CMD5_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR1_CFG_FBN_CMD5_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBNMR1_CFG_FBN_CMD5_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR1_CFG_FBN_CMD5_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR1_CFG_FBN_CMD5_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR1_CFG_FBN_CMD6: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
36:37	RW	FBNMR1_CFG_FBN_CMD6_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR1_CFG_FBN_CMD6_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR1_CFG_FBN_CMD6_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR1_CFG_FBN_CMD6_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR1_CFG_FBN_CMD6_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBNMR1_CFG_FBN_CMD6_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR1_CFG_FBN_CMD6_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR1_CFG_FBN_CMD7: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:53	RW	FBNMR1_CFG_FBN_CMD7_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR1_CFG_FBN_CMD7_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR1_CFG_FBN_CMD7_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR1_CFG_FBN_CMD7_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR1_CFG_FBN_CMD7_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBNMR1_CFG_FBN_CMD7_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR1_CFG_FBN_CMD7_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Memory Registers 2***
Mnemonic	FBIST.FBN.FBNMR2
Address	000000000201088D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR2_CFG_FBN_CMD8: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR2_CFG_FBN_CMD8_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR2_CFG_FBN_CMD8_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR2_CFG_FBN_CMD8_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBNMR2_CFG_FBN_CMD8_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR2_CFG_FBN_CMD8_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR2_CFG_FBN_CMD8_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR2_CFG_FBN_CMD8_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
16:19	RW	FBNMR2_CFG_FBN_CMD9: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR2_CFG_FBN_CMD9_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR2_CFG_FBN_CMD9_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR2_CFG_FBN_CMD9_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR2_CFG_FBN_CMD9_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBNMR2_CFG_FBN_CMD9_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR2_CFG_FBN_CMD9_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR2_CFG_FBN_CMD9_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
32:35	RW	FBNMR2_CFG_FBN_CMD10: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR2_CFG_FBN_CMD10_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR2_CFG_FBN_CMD10_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR2_CFG_FBN_CMD10_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR2_CFG_FBN_CMD10_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR2_CFG_FBN_CMD10_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBNMR2_CFG_FBN_CMD10_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR2_CFG_FBN_CMD10_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
48:51	RW	FBNMR2_CFG_FBN_CMD11: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR2_CFG_FBN_CMD11_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR2_CFG_FBN_CMD11_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR2_CFG_FBN_CMD11_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR2_CFG_FBN_CMD11_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR2_CFG_FBN_CMD11_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBNMR2_CFG_FBN_CMD11_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR2_CFG_FBN_CMD11_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	*FBIST Nest Memory Registers 3*
Mnemonic	FBIST.FBN.FBNMR3
Address	000000000201088E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR3_CFG_FBN_CMD12: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR3_CFG_FBN_CMD12_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR3_CFG_FBN_CMD12_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR3_CFG_FBN_CMD12_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBNMR3_CFG_FBN_CMD12_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR3_CFG_FBN_CMD12_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
14	RW	FBNMR3_CFG_FBN_CMD12_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR3_CFG_FBN_CMD12_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR3_CFG_FBN_CMD13: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR3_CFG_FBN_CMD13_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR3_CFG_FBN_CMD13_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR3_CFG_FBN_CMD13_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR3_CFG_FBN_CMD13_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBNMR3_CFG_FBN_CMD13_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
30	RW	FBNMR3_CFG_FBN_CMD13_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR3_CFG_FBN_CMD13_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR3_CFG_FBN_CMD14: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR3_CFG_FBN_CMD14_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR3_CFG_FBN_CMD14_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR3_CFG_FBN_CMD14_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR3_CFG_FBN_CMD14_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR3_CFG_FBN_CMD14_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBNMR3_CFG_FBN_CMD14_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR3_CFG_FBN_CMD14_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR3_CFG_FBN_CMD15: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR3_CFG_FBN_CMD15_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR3_CFG_FBN_CMD15_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR3_CFG_FBN_CMD15_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR3_CFG_FBN_CMD15_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR3_CFG_FBN_CMD15_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBNMR3_CFG_FBN_CMD15_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR3_CFG_FBN_CMD15_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Memory Registers 4***
Mnemonic	FBIST.FBN.FBNMR4
Address	000000000201088F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR4_CFG_FBN_CMD16: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR4_CFG_FBN_CMD16_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR4_CFG_FBN_CMD16_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR4_CFG_FBN_CMD16_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111

Bits	SCOM	Field Mnemonic: Description
12	RW	FBNMR4_CFG_FBN_CMD16_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR4_CFG_FBN_CMD16_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR4_CFG_FBN_CMD16_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR4_CFG_FBN_CMD16_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR4_CFG_FBN_CMD17: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR4_CFG_FBN_CMD17_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR4_CFG_FBN_CMD17_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR4_CFG_FBN_CMD17_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR4_CFG_FBN_CMD17_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1

Bits	SCOM	Field Mnemonic: Description
29	RW	FBNMR4_CFG_FBN_CMD17_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR4_CFG_FBN_CMD17_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR4_CFG_FBN_CMD17_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR4_CFG_FBN_CMD18: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR4_CFG_FBN_CMD18_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR4_CFG_FBN_CMD18_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR4_CFG_FBN_CMD18_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR4_CFG_FBN_CMD18_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR4_CFG_FBN_CMD18_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBNMR4_CFG_FBN_CMD18_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR4_CFG_FBN_CMD18_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR4_CFG_FBN_CMD19: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR4_CFG_FBN_CMD19_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR4_CFG_FBN_CMD19_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR4_CFG_FBN_CMD19_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR4_CFG_FBN_CMD19_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR4_CFG_FBN_CMD19_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBNMR4_CFG_FBN_CMD19_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR4_CFG_FBN_CMD19_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Memory Registers 5***
Mnemonic	FBIST.FBN.FBNMR5
Address	0000000002010890 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR5_CFG_FBN_CMD20: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR5_CFG_FBN_CMD20_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR5_CFG_FBN_CMD20_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR5_CFG_FBN_CMD20_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111

Bits	SCOM	Field Mnemonic: Description
12	RW	FBNMR5_CFG_FBN_CMD20_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR5_CFG_FBN_CMD20_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR5_CFG_FBN_CMD20_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR5_CFG_FBN_CMD20_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR5_CFG_FBN_CMD21: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR5_CFG_FBN_CMD21_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR5_CFG_FBN_CMD21_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR5_CFG_FBN_CMD21_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR5_CFG_FBN_CMD21_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1

Bits	SCOM	Field Mnemonic: Description
29	RW	FBNMR5_CFG_FBN_CMD21_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR5_CFG_FBN_CMD21_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR5_CFG_FBN_CMD21_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR5_CFG_FBN_CMD22: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR5_CFG_FBN_CMD22_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR5_CFG_FBN_CMD22_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR5_CFG_FBN_CMD22_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR5_CFG_FBN_CMD22_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR5_CFG_FBN_CMD22_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBNMR5_CFG_FBN_CMD22_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR5_CFG_FBN_CMD22_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR5_CFG_FBN_CMD23: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR5_CFG_FBN_CMD23_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR5_CFG_FBN_CMD23_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR5_CFG_FBN_CMD23_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR5_CFG_FBN_CMD23_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR5_CFG_FBN_CMD23_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBNMR5_CFG_FBN_CMD23_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR5_CFG_FBN_CMD23_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Memory Registers 6***
Mnemonic	FBIST.FBN.FBNMR6
Address	0000000002010891 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR6_CFG_FBN_CMD24: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR6_CFG_FBN_CMD24_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR6_CFG_FBN_CMD24_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR6_CFG_FBN_CMD24_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111

Bits	SCOM	Field Mnemonic: Description
12	RW	FBNMR6_CFG_FBN_CMD24_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR6_CFG_FBN_CMD24_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR6_CFG_FBN_CMD24_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR6_CFG_FBN_CMD24_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR6_CFG_FBN_CMD25: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR6_CFG_FBN_CMD25_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR6_CFG_FBN_CMD25_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR6_CFG_FBN_CMD25_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR6_CFG_FBN_CMD25_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1

Bits	SCOM	Field Mnemonic: Description
29	RW	FBNMR6_CFG_FBN_CMD25_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR6_CFG_FBN_CMD25_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR6_CFG_FBN_CMD25_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR6_CFG_FBN_CMD26: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR6_CFG_FBN_CMD26_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR6_CFG_FBN_CMD26_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR6_CFG_FBN_CMD26_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR6_CFG_FBN_CMD26_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR6_CFG_FBN_CMD26_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBNMR6_CFG_FBN_CMD26_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR6_CFG_FBN_CMD26_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR6_CFG_FBN_CMD27: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR6_CFG_FBN_CMD27_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR6_CFG_FBN_CMD27_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR6_CFG_FBN_CMD27_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR6_CFG_FBN_CMD27_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR6_CFG_FBN_CMD27_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBNMR6_CFG_FBN_CMD27_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR6_CFG_FBN_CMD27_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Memory Registers 7***
Mnemonic	FBIST.FBN.FBNMR7
Address	0000000002010892 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNMR7_CFG_FBN_CMD28: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBNMR7_CFG_FBN_CMD28_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBNMR7_CFG_FBN_CMD28_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBNMR7_CFG_FBN_CMD28_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111

Bits	SCOM	Field Mnemonic: Description
12	RW	FBNMR7_CFG_FBN_CMD28_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBNMR7_CFG_FBN_CMD28_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBNMR7_CFG_FBN_CMD28_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBNMR7_CFG_FBN_CMD28_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBNMR7_CFG_FBN_CMD29: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBNMR7_CFG_FBN_CMD29_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBNMR7_CFG_FBN_CMD29_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBNMR7_CFG_FBN_CMD29_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBNMR7_CFG_FBN_CMD29_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1

Bits	SCOM	Field Mnemonic: Description
29	RW	FBNMR7_CFG_FBN_CMD29_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBNMR7_CFG_FBN_CMD29_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBNMR7_CFG_FBN_CMD29_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBNMR7_CFG_FBN_CMD30: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBNMR7_CFG_FBN_CMD30_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBNMR7_CFG_FBN_CMD30_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBNMR7_CFG_FBN_CMD30_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBNMR7_CFG_FBN_CMD30_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBNMR7_CFG_FBN_CMD30_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBNMR7_CFG_FBN_CMD30_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBNMR7_CFG_FBN_CMD30_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBNMR7_CFG_FBN_CMD31: Command Type All other combinations default to read with good cresp. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBNMR7_CFG_FBN_CMD31_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBNMR7_CFG_FBN_CMD31_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBNMR7_CFG_FBN_CMD31_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBNMR7_CFG_FBN_CMD31_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBNMR7_CFG_FBN_CMD31_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBNMR7_CFG_FBN_CMD31_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBNMR7_CFG_FBN_CMD31_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Nest Parameter Register 0***
Mnemonic	FBIST.FBN.FBNPARM0
Address	0000000002010893 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	FBNPARM0_CFG_FBN_MODE: Sets the FBIST mode. Values: DDR_MODE=>0b0 CACHE_MODE=>0b1
1	RW	FBNPARM0_CFG_FBN_SYS_TYPE: Values: PSERIES=>0b0 ZSERIES=>0b1
2	RW	FBNPARM0_CFG_FBN_MBA_CHK: Configures which MBA will be checked Values: CHECK_MBA01=>0b0 CHECK_MBA23=>0b1
3	RW	FBNPARM0_CFG_FBN_CMD_SEQ: Command sequence selection Values: IN_ORDER=>0b0 AT_RANDOM=>0b1
4	RW	FBNPARM0_CFG_FBN_CONT_RUN: Run the test continuous without stopping or stop after test Values: STOP_AFTER_TEST=>0b0 RUN_CONTINUOUS=>0b1
5	RW	FBNPARM0_CFG_FBN_STOP_ON_ERR: Count all errors or stop after the first Values: TALLY_ERRORS=>0b0 STOP_ON_FIRST=>0b1
6	RW	FBNPARM0_CFG_FBN_STOP_ON_ADDR: Stop after each command has looped through the addr range once or continue to loop through. Values: CONT_LOOP=>0b0 ONE_LOOP=>0b1
7	RW	FBNPARM0_CFG_FBN_TST_LEN_TYPE: Count 2.4ghz4 clocks cycles or count each command issued not including idle commands Values: TIME=>0b0 CMDS=>0b1
8	RW	FBNPARM0_CFG_FBN_ADDR_CHK: Turn on or off address checking

Bits	SCOM	Field Mnemonic: Description
9	RW	FBNPARM0_CFG_FBN_CMD_SPC: Random or fixed command spacing Values: USER_DEFINED=>0b0 RANDOM=>0b1
10	RW	FBNPARM0_CFG_FBN_DP_TAG_LOC: The dptag includes an invert bit, the data pattern and wr tag bits. The 12 dp pattern bits will be placed in the 12b starting at bit 32 of the DWs selected. Be sure that the RMW command avoids writing to these bit positions. RMW is allowed to overwrite these bit positions ONLY for an entire cache line merge. Values: TAG_IN_DW048C=>0b0 TAG_IN_DW159D=>0b1
11	RW	FBNPARM0_CFG_FBN_MEM_TYPE: Choose ddr3 or ddr4 mem type Values: DDR3=>0b0 DDR4=>0b1
12	RW	FBNPARM0_CFG_FBN_DS_CRC: Turn on or off Downstream CRC generation
13	RW	FBNPARM0_CFG_FBN_US_CRC: Turn on or off upstream crc checking
14:15	RW	FBNPARM0_CFG_FBN_DS_CMD_LOC: Choose a fixed or random location for the downstream command blocks Values: BLOCK_0=>0b00 BLOCK_1=>0b01 BLOCK_2=>0b10 RANDOM=>0b11
16	RW	FBNPARM0_CFG_FBN_RST_KEEPER: FBN Reset keeper Values: DOES_NOTHING=>0b0 RESET_KEEPER=>0b1
17	RW	FBNPARM0_CFG_FBN_CACHELINE_CHK: Choose a specific command tag to read a full cache line into the expected data register, or use the next full upstream cache line Values: USER_SPECIFIED=>0b0 NEXT=>0b1
18	RW	FBNPARM0_CFG_FBN_2N_ADDR: Turn on or off 2N addr mode
19	RW	FBNPARM0_CFG_FBN_MBSXCRQ5: Should be set to same value as register bit mbsxcrq(5)
20:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***FBIST Nest Command Spacing Register***
Mnemonic	FBIST.FBN.FBNCSPCR
Address	0000000002010894 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FBNCSPCR_CFG_FBN_CMD_SPC: Provides the user defined command spacing from 0 to 255 2.44 clock cycles. This is used as a mask in random mode to limit the random spacing. Each bit when set to one allows the use of that same bit to be a one during random spacing. Hence setting this field to FF allows random cmd spacing from 00-FF and setting this field to 00 allows random passing from 00 - 00.
8:15	RWX	FBNCSPCR_CFG_FBN_CMD_SPC_SEED: Provides the random seed for random command spacing mode. Must be 0x01 or higher
16:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***FBIST Nest Runtime Counter Register***
Mnemonic	FBIST.FBN.FBNRTCTR
Address	0000000002010895 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	FBNRTCTR_FBN_RUN_CNT: This is the runtime counter facility. Will be able to count time or number of executed commands.
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest Test Time Register***
Mnemonic	FBIST.FBN.FBNTT
Address	0000000002010896 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	RW	FBNTT_CFG_FBN_TEST_TIME: This is the user defined test time. This should represent either the maximum run time, or the maximum number of commands to run.
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest Data Config Register***
Mnemonic	FBIST.FBN.FBNDCR
Address	0000000002010897 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	FBNDCR_CFG_FBN_DATA_INV: Data inversion configuration is used in conjunction with the data pattern inversion bits in the fbnmr0:7 registers. Each bit from 0 through 16 determines which dw of data will be inverted. In example, if b0 is 1 then dw0 will be inverted should the data pattern inversion bit for the commands (in fbnmr0:7) is also set. This allows the used to create data traffic on certain buses that will flip every cycle, etc.
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***FBIST Nest Random Command Seed Register***
Mnemonic	FBIST.FBN.FBNRCSR
Address	0000000002010898 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	FBNRCSR_CFG_FBN_CMD_GEN_SEED: This seed is used to generate a command at random
8:15	RWX	FBNRCSR_CFG_FBN_CMD_SEL_SEED: This seed is used to select a command at random
16:23	RWX	FBNRCSR_CFG_FBN_DATA_PAT_SEED: This seed is used to select a random data pattern
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***FBIST Nest Random Command Config Register***
Mnemonic	FBIST.FBN.FBNRCCR
Address	0000000002010899 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	FBNRCCR_CFG_FBN_RCCR_RESERVED0: Bits 0:7 reserved
8:15	RWX	FBNRCCR_CFG_FBN_CMD_LOC_SEED: Bits 8:15 the cmd loc seed
16:23	RW	FBNRCCR_CFG_FBN_CMD_CHK_SEED: Bits 16:23 The user specified command checking tag, used to select a tag to read out the full cache line. Used with fbmparm0(17)
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***FBIST Nest RMW Cmd Register***
Mnemonic	FBIST.FBN.FBNRMWC
Address	000000000201089A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNRMWC_CFG_FBN_RMW_FUNC: Default is for RMW partial write. No ALU support at this time
4	RW	FBNRMWC_RESERVED_4: Reserved
5:11	RW	FBNRMWC_CFG_FBN_RMW_TSZ: Default set for 1 Byte Partial write
12	RW	FBNRMWC_RESERVED_12: Reserved
13:19	RW	FBNRMWC_CFG_FBN_RMW_ADDR: Sets the byte address in the cache line for the partial write (be sure not to use the location of the wrtag and data pattern tag) Special considerations should be taken when running a test with random data as the first byte of each DW is used to reconstruct the data for checking.
20:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***FBIST Nest Random Address Gen Register***
Mnemonic	FBIST.FBN.FBNRAG
Address	000000000201089B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:32	RW	FBNRAG_CFG_FBN_ADDR_RND_LFSRM: Bits 0:32 of the random address RSFSR mask
33:38	RW	FBNRAG_CFG_FBN_ADDR_RND_FW: Bits 0:5 of the random address fixed width generation
39:47	RW	FBNRAG_CFG_FBN_ADDR_RND_RES: Reserved Block of bits
48:63	RO	constant=0b0000000000000000

Register Name	***FBIST Nest Start Address Configuration Register***
Mnemonic	FBIST.FBN.FBNSAC
Address	000000000201089C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	RW	FBNSAC_CFG_FBN_ADDR_START: Starting Address when addressing is forward Ending Address when addressing is reverse
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest End Address Configuration Register***
Mnemonic	FBIST.FBN.FBNEAC
Address	000000000201089D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	RW	FBNEAC_CFG_FBN_ADDR_END: Ending Address when addressing is forward Starting Address when addressing is reverse
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest P Address Map Register 0***
Mnemonic	FBIST.FBN.FBNPAM0
Address	000000000201089E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNPAM0_CFG_FBN_AMAP_MRANK0: Master Rank Bit 0 (MSB) Values: ADDR_BIT_30=>0b0000 ADDR_BIT_28=>0b0001 ADDR_BIT_27=>0b0010 ADDR_BIT_7=>0b0011 ADDR_BIT_6=>0b0100 ADDR_BIT_5=>0b0101 ADDR_BIT_4=>0b0110 ADDR_BIT_3=>0b0111 ADDR_BIT_2=>0b1000 ADDR_BIT_1=>0b1001 UNUSED=>0b1111
4:7	RW	FBNPAM0_CFG_FBN_AMAP_MRANK1: Master Rank Bit 1 Values: ADDR_BIT_28=>0b0000 ADDR_BIT_27=>0b0001 ADDR_BIT_6=>0b0010 ADDR_BIT_5=>0b0011 ADDR_BIT_4=>0b0100 ADDR_BIT_3=>0b0101 ADDR_BIT_2=>0b0110 UNUSED=>0b1111
8:11	RW	FBNPAM0_CFG_FBN_AMAP_MRANK2: Master Rank Rank Bit 2 Values: ADDR_BIT_30=>0b0000 ADDR_BIT_28=>0b0001 ADDR_BIT_27=>0b0010 ADDR_BIT_7=>0b0011 ADDR_BIT_6=>0b0100 ADDR_BIT_5=>0b0101 ADDR_BIT_4=>0b0110 ADDR_BIT_3=>0b0111 ADDR_BIT_2=>0b1000 UNUSED=>0b1111
12:15	RW	FBNPAM0_CFG_FBN_AMAP_SRANK0: Slave Rank Bit 0 (MSB) Values: UNUSED=>0b1111
16:19	RW	FBNPAM0_CFG_FBN_AMAP_SRANK1: Slave Rank Bit 1 Values: ADDR_BIT_28=>0b0000 ADDR_BIT_27=>0b0001 UNUSED=>0b1111
20:23	RW	FBNPAM0_CFG_FBN_AMAP_SRANK2: Slave Rank Rank Bit 2 Values: ADDR_BIT_30=>0b0000 UNUSED=>0b1111
24:27	RW	FBNPAM0_CFG_FBN_AMAP_BANK0: DRAM Bank Address Bit 0 (MSB) Values: ADDR_BIT_32=>0b0000 ADDR_BIT_30=>0b0001 ADDR_BIT_29=>0b0010 UNUSED=>0b1111
28:31	RW	FBNPAM0_CFG_FBN_AMAP_BANK1: DRAM Bank Address Bit 1 (MSB) Values: ADDR_BIT_31=>0b0000 ADDR_BIT_29=>0b0001 ADDR_BIT_28=>0b0010 UNUSED=>0b1111

Bits	SCOM	Field Mnemonic: Description
32:35	RW	FBNPAM0_CFG_FBN_AMAP_BANK2: DRAM Bank Address Bit 2 Values: ADDR_BIT_30=>0b0000 ADDR_BIT_29=>0b0001 UNUSED=>0b1111
36:39	RW	FBNPAM0_CFG_FBN_AMAP_BG0: DRAM Bank Group Address Bit 0 Values: ADDR_BIT_32=>0b0000 UNUSED=>0b1111
40:43	RW	FBNPAM0_CFG_FBN_AMAP_BG1: DRAM Bank Group Address Bit 1 Values: ADDR_BIT_31=>0b0000 UNUSED=>0b1111
44:47	RW	FBNPAM0_CFG_FBN_AMAP_ROW14: DRAM Row Address Bit 14 Values: ADDR_BIT_8=>0b0000 ADDR_BIT_7=>0b0001 ADDR_BIT_6=>0b0010 ADDR_BIT_5=>0b0011 UNUSED=>0b1111
48:51	RW	FBNPAM0_CFG_FBN_AMAP_ROW15: DRAM Row Address Bit 15 Values: ADDR_BIT_7=>0b0000 ADDR_BIT_6=>0b0001 ADDR_BIT_5=>0b0010 ADDR_BIT_4=>0b0011 ADDR_BIT_3=>0b0100 UNUSED=>0b1111
52:55	RW	FBNPAM0_CFG_FBN_AMAP_ROW16: DRAM Row Address Bit 16 Values: ADDR_BIT_5=>0b0000 ADDR_BIT_4=>0b0001 ADDR_BIT_3=>0b0010 UNUSED=>0b1111
56:59	RW	FBNPAM0_CFG_FBN_AMAP_MBA: DRAM MBA select Address Bit Values: ADDR_BIT_7=>0b0000 ADDR_BIT_6=>0b0001 ADDR_BIT_5=>0b0010 ADDR_BIT_4=>0b0011 ADDR_BIT_3=>0b0100 ADDR_BIT_2=>0b0101 ADDR_BIT_1=>0b0110 ADDR_BIT_0=>0b0111 UNUSED=>0b1111
60:63	RO	constant=0b0000 Values: ADDR_BIT_7=>0b0000 ADDR_BIT_6=>0b0001 ADDR_BIT_5=>0b0010 ADDR_BIT_4=>0b0011 ADDR_BIT_3=>0b0100 ADDR_BIT_2=>0b0101 ADDR_BIT_1=>0b0110 ADDR_BIT_0=>0b0111 UNUSED=>0b1111

Register Name	***FBIST Nest P Address Map Register 1***
Mnemonic	FBIST.FBN.FBNPAM1
Address	000000000201089F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBNPAM1_CFG_FBN_AMAP_COL3: DRAM Col Address Bit 3 (MSB) Values: ADDR_BIT_29=>0b0000 ADDR_BIT_28=>0b0001 ADDR_BIT_27=>0b0010 ADDR_BIT_26=>0b0011 UNUSED=>0b1111
4:7	RW	FBNPAM1_CFG_FBN_AMAP_COL4: DRAM Col Address Bit 4 (MSB) Values: ADDR_BIT_28=>0b0000 ADDR_BIT_27=>0b0001 ADDR_BIT_26=>0b0010 ADDR_BIT_25=>0b0011 UNUSED=>0b1111
8:11	RW	FBNPAM1_CFG_FBN_AMAP_COL5: DRAM Col Address Bit 5 (MSB)) Values: ADDR_BIT_27=>0b0000 ADDR_BIT_26=>0b0001 ADDR_BIT_25=>0b0010 ADDR_BIT_24=>0b0011 UNUSED=>0b1111
12:15	RW	FBNPAM1_CFG_FBN_AMAP_COL6: DRAM Col Address Bit 6 (MSB) Values: ADDR_BIT_26=>0b0000 ADDR_BIT_25=>0b0001 ADDR_BIT_24=>0b0010 ADDR_BIT_23=>0b0011 UNUSED=>0b1111
16:19	RW	FBNPAM1_CFG_FBN_AMAP_COL7: DRAM Col Address Bit 7 (MSB) Values: ADDR_BIT_25=>0b0000 ADDR_BIT_24=>0b0001 ADDR_BIT_23=>0b0010 ADDR_BIT_8=>0b0011 UNUSED=>0b1111
20:23	RW	FBNPAM1_CFG_FBN_AMAP_COL8: DRAM Col Address Bit 8 (MSB) Values: ADDR_BIT_24=>0b0000 ADDR_BIT_23=>0b0001 ADDR_BIT_8=>0b0010 ADDR_BIT_7=>0b0011 UNUSED=>0b1111
24:27	RW	FBNPAM1_CFG_FBN_AMAP_COL9: DRAM Col Address Bit 9 (MSB) Values: ADDR_BIT_23=>0b0000 ADDR_BIT_8=>0b0001 ADDR_BIT_7=>0b0010 ADDR_BIT_6=>0b0011 UNUSED=>0b1111
28:31	RW	FBNPAM1_CFG_FBN_AMAP_COL10: DRAM Col Address Bit 10 (MSB) Values: UNUSED=>0b1111

Bits	SCOM	Field Mnemonic: Description
32:35	RW	FBNPAM1_CFG_FBN_AMAP_COL11: DRAM Col Address Bit 11 (MSB) Values: ADDR_BIT_7=>0b0000 ADDR_BIT_6=>0b0001 ADDR_BIT_5=>0b0010 UNUSED=>0b1111
36:39	RW	FBNPAM1_CFG_FBN_AMAP_COL12: DRAM Col Address Bit 12 (MSB) Values: UNUSED=>0b1111
40:43	RW	FBNPAM1_CFG_FBN_AMAP_COL13: DRAM Col Address Bit 12 (MSB) Values: ADDR_BIT_6=>0b0000 ADDR_BIT_5=>0b0001 ADDR_BIT_4=>0b0010 UNUSED=>0b1111
44:63	RO	constant=0b00000000000000000000 Values: ADDR_BIT_6=>0b0000 ADDR_BIT_5=>0b0001 ADDR_BIT_4=>0b0010 UNUSED=>0b1111

Register Name	***FBIST Nest Hang Pulse Configuration Register***
Mnemonic	FBIST.FBN.FBNHPC
Address	00000000020108A0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:23	RW	FBNHPC_CFG_FBN_ERR_HANG_PULSE: Hang pulse interval. The hang pulse increments every 256 2.4ghz4 clock cycles. For a hang to register, the hang criteria must be in the hang state through an entire hang interval. This means that least amount of time a hang can exist before detection is the duration of the hang pulse and the longest a hang can exist before detection is 2(hang interval) - 1.
24	RW	FBNHPC_CFG_FBN_ERR_HANG_DIS: Hang detection disable Values: ENABLE=>0b0 DISABLE=>0b1
25:63	RO	constant=0b00000000000000000000000000000000000000000 Values: ENABLE=>0b0 DISABLE=>0b1

Register Name	***FBIST Nest User Data Config Registers 0***
Mnemonic	FBIST.FBN.FBNUD0
Address	00000000020108A2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD0_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 1*
Mnemonic	FBIST.FBN.FBNUD1
Address	00000000020108A3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD1_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 2*
Mnemonic	FBIST.FBN.FBNUD2
Address	00000000020108A4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD2_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 3*
Mnemonic	FBIST.FBN.FBNUD3
Address	00000000020108A5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD3_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 4*
Mnemonic	FBIST.FBN.FBNUD4
Address	00000000020108A6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD4_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 5*
Mnemonic	FBIST.FBN.FBNUD5
Address	00000000020108A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD5_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 6*
Mnemonic	FBIST.FBN.FBNUD6
Address	00000000020108A8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD6_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 7*
Mnemonic	FBIST.FBN.FBNUD7
Address	00000000020108A9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD7_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 8*
Mnemonic	FBIST.FBN.FBNUD8
Address	00000000020108AA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD8_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest User Data Config Registers 9***
Mnemonic	FBIST.FBN.FBNUD9
Address	00000000020108AB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD9_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest User Data Config Registers 10***
Mnemonic	FBIST.FBN.FBNUD10
Address	00000000020108AC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD10_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest User Data Config Registers 11***
Mnemonic	FBIST.FBN.FBNUD11
Address	00000000020108AD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD11_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest User Data Config Registers 12***
Mnemonic	FBIST.FBN.FBNUD12
Address	00000000020108AE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD12_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 13*
Mnemonic	FBIST.FBN.FBNUD13
Address	00000000020108AF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD13_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 14*
Mnemonic	FBIST.FBN.FBNUD14
Address	00000000020108B0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD14_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest User Data Config Registers 15*
Mnemonic	FBIST.FBN.FBNUD15
Address	00000000020108B1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNUD15_CFG_FBN_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Address Mask Configuration Register*
Mnemonic	FBIST.FBN.FBNAMC
Address	00000000020108B2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	RW	FBNAMC_CFG_FBN_ADDR_MASK: Address Mask
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest Data Miss Error Counter 0***
Mnemonic	FBIST.FBN.FBNDMEC0
Address	00000000020108B3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBNDMEC0_FBN_ERR_CNTR0: Data miscompare error counter
8:15	ROX	FBNDMEC0_FBN_ERR_CNTR1: Data miscompare error counter
16:23	ROX	FBNDMEC0_FBN_ERR_CNTR2: Data miscompare error counter
24:31	ROX	FBNDMEC0_FBN_ERR_CNTR3: Data miscompare error counter
32:39	ROX	FBNDMEC0_FBN_ERR_CNTR4: Data miscompare error counter
40:47	ROX	FBNDMEC0_FBN_ERR_CNTR5: Data miscompare error counter
48:55	ROX	FBNDMEC0_FBN_ERR_CNTR6: Data miscompare error counter
56:63	ROX	FBNDMEC0_FBN_ERR_CNTR7: Data miscompare error counter

Register Name	***FBIST Nest Data Miss Error Counter 1***
Mnemonic	FBIST.FBN.FBNDMEC1
Address	00000000020108B4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBNDMEC1_FBN_ERR_CNTR8: Data miscompare error counter
8:15	ROX	FBNDMEC1_FBN_ERR_CNTR9: Data miscompare error counter
16:23	ROX	FBNDMEC1_FBN_ERR_CNTR10: Data miscompare error counter
24:31	ROX	FBNDMEC1_FBN_ERR_CNTR11: Data miscompare error counter
32:39	ROX	FBNDMEC1_FBN_ERR_CNTR12: Data miscompare error counter
40:47	ROX	FBNDMEC1_FBN_ERR_CNTR13: Data miscompare error counter
48:55	ROX	FBNDMEC1_FBN_ERR_CNTR14: Data miscompare error counter
56:63	ROX	FBNDMEC1_FBN_ERR_CNTR15: Data miscompare error counter

Register Name	***FBIST Nest Data Miss Error Counter 2***
Mnemonic	FBIST.FBN.FBNDMEC2
Address	00000000020108B5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBNDMEC2_FBN_ERR_CNTR16: Data miscompare error counter
8:15	ROX	FBNDMEC2_FBN_ERR_CNTR17: Data miscompare error counter

Bits	SCOM	Field Mnemonic: Description
16:23	ROX	FBNDMEC2_FBN_ERR_CNTR18: Data miscompare error counter
24:31	ROX	FBNDMEC2_FBN_ERR_CNTR19: Data miscompare error counter
32:39	ROX	FBNDMEC2_FBN_ERR_CNTR20: Data miscompare error counter
40:47	ROX	FBNDMEC2_FBN_ERR_CNTR21: Data miscompare error counter
48:55	ROX	FBNDMEC2_FBN_ERR_CNTR22: Data miscompare error counter
56:63	ROX	FBNDMEC2_FBN_ERR_CNTR23: Data miscompare error counter

Register Name	***FBIST Nest Data Miss Error Counter 3***
Mnemonic	FBIST.FBN.FBNDMEC3
Address	00000000020108B6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBNDMEC3_FBN_ERR_CNTR24: Data miscompare error counter
8:15	ROX	FBNDMEC3_FBN_ERR_CNTR25: Data miscompare error counter
16:23	ROX	FBNDMEC3_FBN_ERR_CNTR26: Data miscompare error counter
24:31	ROX	FBNDMEC3_FBN_ERR_CNTR27: Data miscompare error counter
32:39	ROX	FBNDMEC3_FBN_ERR_CNTR28: Data miscompare error counter
40:47	ROX	FBNDMEC3_FBN_ERR_CNTR29: Data miscompare error counter
48:55	ROX	FBNDMEC3_FBN_ERR_CNTR30: Data miscompare error counter
56:63	ROX	FBNDMEC3_FBN_ERR_CNTR31: Data miscompare error counter

Register Name	***FBIST Nest Error Mask And Status Register***
Mnemonic	FBIST.FBN.FBNEMS
Address	00000000020108B7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	FBNEMS_RESERVED_0: Reserved
1	ROX	FBNEMS_RESERVED_1: Reserved
2	ROX	FBNEMS_FBIST_IP: Hardware sets to 1 when FBIST is in progress
3	ROX	FBNEMS_FBIST_DONE: Hardware sets to 1 when FBIST has completed
4	ROX	FBNEMS_FBIST_FAIL: Hardware sets to 1 when FBIST has failed
5:31	ROX	FBNEMS_RESERVED_5_31: RESERVED
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***FBIST Nest Data Compare Mask Register 0***
Mnemonic	FBIST.FBN.FBNDCM0
Address	00000000020108B8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM0_CFG_FBN_DATA_CMP_MASK0: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 1***
Mnemonic	FBIST.FBN.FBNDCM1
Address	00000000020108B9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM1_CFG_FBN_DATA_CMP_MASK1: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 2***
Mnemonic	FBIST.FBN.FBNDCM2
Address	00000000020108BA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM2_CFG_FBN_DATA_CMP_MASK2: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 3***
Mnemonic	FBIST.FBN.FBNDCM3
Address	00000000020108BB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM3_CFG_FBN_DATA_CMP_MASK3: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 4*
Mnemonic	FBIST.FBN.FBNDCM4
Address	00000000020108BC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM4_CFG_FBN_DATA_CMP_MASK4: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 5*
Mnemonic	FBIST.FBN.FBNDCM5
Address	00000000020108BD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM5_CFG_FBN_DATA_CMP_MASK5: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 6*
Mnemonic	FBIST.FBN.FBNDCM6
Address	00000000020108BE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM6_CFG_FBN_DATA_CMP_MASK6: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 7*
Mnemonic	FBIST.FBN.FBNDCM7
Address	00000000020108BF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM7_CFG_FBN_DATA_CMP_MASK7: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 8***
Mnemonic	FBIST.FBN.FBNDCM8
Address	00000000020108C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM8_CFG_FBN_DATA_CMP_MASK8: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 9***
Mnemonic	FBIST.FBN.FBNDCM9
Address	00000000020108C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM9_CFG_FBN_DATA_CMP_MASK9: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 10***
Mnemonic	FBIST.FBN.FBNDCM10
Address	00000000020108C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM10_CFG_FBN_DATA_CMP_MASK10: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Data Compare Mask Register 11***
Mnemonic	FBIST.FBN.FBNDCM11
Address	00000000020108C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM11_CFG_FBN_DATA_CMP_MASK11: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 12*
Mnemonic	FBIST.FBN.FBNDCM12
Address	00000000020108C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM12_CFG_FBN_DATA_CMP_MASK12: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 13*
Mnemonic	FBIST.FBN.FBNDCM13
Address	00000000020108C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM13_CFG_FBN_DATA_CMP_MASK13: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 14*
Mnemonic	FBIST.FBN.FBNDCM14
Address	00000000020108C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM14_CFG_FBN_DATA_CMP_MASK14: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Data Compare Mask Register 15*
Mnemonic	FBIST.FBN.FBNDCM15
Address	00000000020108C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBNDCM15_CFG_FBN_DATA_CMP_MASK15: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 0***
Mnemonic	FBIST.FBN.FBNED0
Address	00000000020108C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED0_FBN_DATA_EXP0: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 1***
Mnemonic	FBIST.FBN.FBNED1
Address	00000000020108C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED1_FBN_DATA_EXP1: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 2***
Mnemonic	FBIST.FBN.FBNED2
Address	00000000020108CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED2_FBN_DATA_EXP2: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 3***
Mnemonic	FBIST.FBN.FBNED3
Address	00000000020108CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED3_FBN_DATA_EXP3: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 4*
Mnemonic	FBIST.FBN.FBNED4
Address	00000000020108CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED4_FBN_DATA_EXP4: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 5*
Mnemonic	FBIST.FBN.FBNED5
Address	00000000020108CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED5_FBN_DATA_EXP5: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 6*
Mnemonic	FBIST.FBN.FBNED6
Address	00000000020108CE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED6_FBN_DATA_EXP6: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 7*
Mnemonic	FBIST.FBN.FBNED7
Address	00000000020108CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED7_FBN_DATA_EXP7: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 8***
Mnemonic	FBIST.FBN.FBNED8
Address	00000000020108D0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED8_FBN_DATA_EXProcessor: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 9***
Mnemonic	FBIST.FBN.FBNED9
Address	00000000020108D1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED9_FBN_DATA_EXP9: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 10***
Mnemonic	FBIST.FBN.FBNED10
Address	00000000020108D2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED10_FBN_DATA_EXP10: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Expected Data Register 11***
Mnemonic	FBIST.FBN.FBNED11
Address	00000000020108D3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED11_FBN_DATA_EXP11: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 12*
Mnemonic	FBIST.FBN.FBNED12
Address	00000000020108D4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED12_FBN_DATA_EXP12: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 13*
Mnemonic	FBIST.FBN.FBNED13
Address	00000000020108D5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED13_FBN_DATA_EXP13: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 14*
Mnemonic	FBIST.FBN.FBNED14
Address	00000000020108D6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED14_FBN_DATA_EXP14: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Expected Data Register 15*
Mnemonic	FBIST.FBN.FBNED15
Address	00000000020108D7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNED15_FBN_DATA_EXP15: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 0***
Mnemonic	FBIST.FBN.FBNRD0
Address	00000000020108D8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD0_FBN_DATA_RX0: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 1***
Mnemonic	FBIST.FBN.FBNRD1
Address	00000000020108D9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD1_FBN_DATA_RX1: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 2***
Mnemonic	FBIST.FBN.FBNRD2
Address	00000000020108DA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD2_FBN_DATA_RX2: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 3***
Mnemonic	FBIST.FBN.FBNRD3
Address	00000000020108DB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD3_FBN_DATA_RX3: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 4*
Mnemonic	FBIST.FBN.FBNRD4
Address	00000000020108DC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD4_FBN_DATA_RX4: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 5*
Mnemonic	FBIST.FBN.FBNRD5
Address	00000000020108DD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD5_FBN_DATA_RX5: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 6*
Mnemonic	FBIST.FBN.FBNRD6
Address	00000000020108DE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD6_FBN_DATA_RX6: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 7*
Mnemonic	FBIST.FBN.FBNRD7
Address	00000000020108DF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD7_FBN_DATA_RX7: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 8***
Mnemonic	FBIST.FBN.FBNRD8
Address	00000000020108E0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD8_FBN_DATA_RX8: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 9***
Mnemonic	FBIST.FBN.FBNRD9
Address	00000000020108E1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD9_FBN_DATA_RX9: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 10***
Mnemonic	FBIST.FBN.FBNRD10
Address	00000000020108E2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD10_FBN_DATA_RX10: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Received Data Register 11***
Mnemonic	FBIST.FBN.FBNRD11
Address	00000000020108E3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD11_FBN_DATA_RX11: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 12*
Mnemonic	FBIST.FBN.FBNRD12
Address	00000000020108E4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD12_FBN_DATA_RX12: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 13*
Mnemonic	FBIST.FBN.FBNRD13
Address	00000000020108E5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD13_FBN_DATA_RX13: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 14*
Mnemonic	FBIST.FBN.FBNRD14
Address	00000000020108E6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD14_FBN_DATA_RX14: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Nest Received Data Register 15*
Mnemonic	FBIST.FBN.FBNRD15
Address	00000000020108E7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBNRD15_FBN_DATA_RX15: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Nest Error Address Register***
Mnemonic	FBIST.FBN.FBNEA
Address	00000000020108E8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	ROX	FBNEA_CFG_FBN_ERR_ADDR: Holds value of the Address associated with the first data comp error
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest Error Info Register***
Mnemonic	FBIST.FBN.FBNEIR
Address	00000000020108E9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBNEIR_FBN_ERR_CMD_TAG: Reports the cmd tag associated with the data miscompare error. Bit 0 is not used
8:15	ROX	FBNEIR_FBN_ERR_DATA_PAT: Reports the data pattern associated with the data miscompare error. Bit 0:1 first DW of cache line with error Bit 2 RMW Commands Bit 3 Data inversion Bit 4:7 Data pattern
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***FBIST Nest Base Address Configuration Register***
Mnemonic	FBIST.FBN.FBNBAC
Address	00000000020108EA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	RW	FBNBAC_CFG_FBN_ADDR_BASE: Base address used in address generation formula
40:63	RO	constant=0b000000000000000000000000

Register Name	***FBIST Nest Random Address Mask Register***
Mnemonic	FBIST.FBN.FBNRAMR
Address	00000000020108EB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:39	RW	FBNRAMR_CFG_FBN_ADDR_RND_MASK: Bits 0:39 of the random address lfsr mask register
40:63	RO	constant=0b000000000000000000000000

Register Name	*FBIST Nest Random Data Seed Register 0*
Mnemonic	FBIST.FBN.FBNRDSR0
Address	00000000020108EC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED0: DW0 Random Data Seed, 8 bit seed used to generate 64b of data for DW0
8:15	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED1: DW1 Random Data Seed, 8 bit seed used to generate 64b of data for DW1
16:23	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED2: DW2 Random Data Seed, 8 bit seed used to generate 64b of data for DW2
24:31	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED3: DW3 Random Data Seed, 8 bit seed used to generate 64b of data for DW3
32:39	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED4: DW4 Random Data Seed, 8 bit seed used to generate 64b of data for DW4
40:47	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED5: DW5 Random Data Seed, 8 bit seed used to generate 64b of data for DW5
48:55	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED6: DW6 Random Data Seed, 8 bit seed used to generate 64b of data for DW6
56:63	RWX	FBNRDSR0_CFG_FBN_DATA_RND_SEED7: DW7 Random Data Seed, 8 bit seed used to generate 64b of data for DW7

Register Name	*FBIST Nest Random Data Seed Register 1*
Mnemonic	FBIST.FBN.FBNRDSR1
Address	00000000020108ED (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEED8: DW8 Random Data Seed, 8 bit seed used to generate 64b of data for DW8
8:15	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEED9: DW9 Random Data Seed, 8 bit seed used to generate 64b of data for DW9
16:23	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEEDA: DWA Random Data Seed, 8 bit seed used to generate 64b of data for DWA
24:31	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEEDB: DWB Random Data Seed, 8 bit seed used to generate 64b of data for DWB
32:39	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEEDC: DWC Random Data Seed, 8 bit seed used to generate 64b of data for DWC
40:47	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEEDD: DWD Random Data Seed, 8 bit seed used to generate 64b of data for DWD
48:55	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEEDE: DWE Random Data Seed, 8 bit seed used to generate 64b of data for DWE
56:63	RW	FBNRDSR1_CFG_FBN_DATA_RND_SEEDF: DWF Random Data Seed, 8 bit seed used to generate 64b of data for DWF

Register Name	***FBIST Nest Random Address Start Register***
Mnemonic	FBIST.FBN.FBNRASR
Address	00000000020108EE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:32	RW	FBNRASR_CFG_FBN_ADDR_RND_START: Start address for random address forward End Address for random address reverse
33:63	RO	constant=0b00000000000000000000000000000000

Register Name	***FBIST Nest Random Address End Register***
Mnemonic	FBIST.FBN.FBNRAER
Address	00000000020108EF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:32	RW	FBNRAER_CFG_FBN_ADDR_RND_END: End address for random address forward Start Address for random address reverse
33:63	RO	constant=0b00000000000000000000000000000000

Register Name	***FBIST Nest MISR0 Register***
Mnemonic	FBIST.FBN.FBNM0
Address	00000000020108F0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	FBNM0_FBN_DS_DATA_MISR: Downstream data MISR
12:35	ROX	FBNM0_FBN_DS_CMD_MISR: Downstream command MISR
36:47	ROX	FBNM0_FBN_US_DATA_MISR: Upstream data MISR
48:63	RO	constant=0b0000000000000000

Register Name	***FBIST Nest MISR1 Register***
Mnemonic	FBIST.FBN.FBNM1
Address	00000000020108F1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	FBNM1_FBN_US_CMD_MISR: Upstream cmd MISR (bit0 is always 0, not used)
24:59	ROX	FBNM1_FBN_DS_ADDR_MISR: Downstream address MISR (bits 24-26 are always 0, not used)
60:63	RO	constant=0b0000

Register Name	***Trace Array High Data Register***
Mnemonic	TCN.TRA.MBITRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000002010C40 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	***Trace Array Low Data Register***
Mnemonic	TCN.TRA.MBITRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000002010C41 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	***MBS FIR Register***
Mnemonic	MBU.MBS.MBS_FIR_REG
Address	0000000002011400 (SCOM) 0000000002011401 (SCOM1) 0000000002011402 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_HOST_PROTOCOL_ERROR: Observed an unexpected Down Stream protocol error such as an unexpected command or write data tag, invalid command encoding, or invalid command sequence.
1	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INT_PROTOCOL_ERROR: Internal logic to the MBS unit experienced a unrecoverable protocol error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INVALID_ADDRESS_ERROR: Address detected that does not translate to a DRAM location.
3	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_EXTERNAL_TIMEOUT: Shadow Machine has timed-out waiting on cresp on a speculative command or have not obtained write data on a write command. If there is no channel replay timeout, we can be certain the timeout is due to the host processor. If there is a replay timeout, the channel will checkstop.
4	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INTERNAL_TIMEOUT: Shadow Machine time-out but not waiting on cresp and not waiting on data, plus a Prefetch timeout or Cleaner timeout. If there is not a replay timeout, this will indicate a problem in the memory buffer.
5	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INT_BUFFER_CE: CE detected in Shadow Write Buffer, Prefetch buffer, or Inband Buffer
6	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INT_BUFFER_UE: UE detected in Shadow Write Buffer, Prefetch buffer, or Inband Buffer
7	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INT_BUFFER_SUE: SUE detected in Shadow Write Buffer, Prefetch buffer, or Inband Buffer
8	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INT_PARITY_ERROR: A parity error was detected by MBS logic, either on an MBS interface or internal to the MBS logic
9	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_CACHE_SRW_CE: CE detected on Shadow read (read port1) Note: PRD counts the number of these within a window of time and may decide to line delete the next CE.
10	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_CACHE_SRW_UE: UE detected on Shadow read (read port1)
11	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_CACHE_SRW_SUE: SUE detected on Shadow read (read port1)
12	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_CACHE_CO_CE: CE detected on a Cleaner or Castout read (read port0)
13	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_CACHE_CO_UE: UE detected on a Cleaner or Castout read (read port0)
14	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_CACHE_CO_SUE: SUE detected on a Cleaner or Castout read (read port0)
15	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_DIR_CE: Directory CE occurred on at least one member during a directory read. An attempt will be made to fix the single bit error.
16	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_DIR_UE: Directory UE occurred on at least one member during a directory read. NOTE: The cache will treat a Directory UE the same as CE in that it will keep trying to fix the error and therefore a timeout will eventually be reported.
17	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_DIR_MEMBER_DELETED: A directory member has been deleted. This can be HW or FW initiated. HW will delete if there is a cache UE on a cache read. FW can setup HW to delete on the next cache CE if the number of CEs exceed a threshold, but FW must monitor the maximum deleted members observed in any congruence class to ensure we do not exceed 15 members deleted in a set.
18	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_DIR_ALL_MEMBERS_DELETED: All 16 members within a particular congruence class have been deleted. This could be due to a UE in each member or PRD allowed too many line deletes on CE.
19	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_LRU_ERROR: invalid LRU value, most likely due to SRAM error. This may impact the performance of the cache, but it is a recoverable error and therefore should not cause a checkstop.
20	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_EDRAM_ERROR: internal eDRAM command collision or eDRAM refresh timeout.
21	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_EMERGENCY_THROTTLE_SET: Emergency Throttle Set

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_HOST_INBAND_READ_ERROR: A PIB error or inband buffer error was detected on a host inband read operation.
23	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_HOST_INBAND_WRITE_ERROR: A PIB error or inband buffer error was detected on a host inband write operation.
24	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_OCC_INBAND_READ_ERROR: A PIB error or inband buffer error was detected on a OCC inband read operation.
25	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_OCC_INBAND_WRITE_ERROR: A PIB error or inband buffer error was detected on a OCC inband write operation.
26	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_SRB_BUFFER_CE: CE detected in Shadow Read Buffer
27	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_SRB_BUFFER_UE: UE detected in Shadow Read Buffer
28	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_SRB_BUFFER_SUE: SUE detected in Shadow Read Buffer
29	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred
30	RWX	WOX_AND	WOX_OR	MBS_FIR_REG_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
31:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000

Register Name	***MBS FIR Mask Register***
Mnemonic	MBU.MBS.MBS_FIR_MASK_REG
Address	0000000002011403 (SCOM) 0000000002011404 (SCOM1) 0000000002011405 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_HOST_PROTOCOL_ERROR: Observed an unexpected Down Stream protocol error such as an unexpected command or write data tag, invalid command encoding, or invalid command sequence.
1	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INT_PROTOCOL_ERROR: Internal logic to the MBS unit experienced a unrecoverable protocol error.
2	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INVALID_ADDRESS_ERROR: Address detected that does not translate to a DRAM location.
3	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_EXTERNAL_TIMEOUT: Shadow Machine has timed-out waiting on cresp on a speculative command or have not obtained write data on a write command. If there is no channel replay timeout, we can be certain the timeout is due to the host processor. If there is a replay timeout, the channel will checkstop.
4	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INTERNAL_TIMEOUT: Shadow Machine time-out but not waiting on cresp and not waiting on data, plus a Prefetch timeout or Cleaner timeout. If there is not a replay timeout, this will indicate a problem in the memory buffer.
5	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INT_BUFFER_CE: CE detected in Shadow Write Buffer, Prefetch buffer, or Inband Buffer
6	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INT_BUFFER_UE: UE detected in Shadow Write Buffer, Prefetch buffer, or Inband Buffer
7	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INT_BUFFER_SUE: SUE detected in Shadow Write Buffer, Prefetch buffer, or Inband Buffer

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INT_PARITY_ERROR: A parity error was detected by MBS logic, either on an MBS interface or internal to the MBS logic
9	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_CACHE_SRW_CE: CE detected on Shadow read (read port1) Note: PRD counts the number of these within a window of time and may decide to line delete the next CE.
10	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_CACHE_SRW_UE: UE detected on Shadow read (read port1)
11	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_CACHE_SRW_SUE: SUE detected on Shadow read (read port1)
12	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_CACHE_CO_CE: CE detected on a Cleaner or Castout read (read port0) Note: PRD counts the number of these within a window of time and may decide to line delete the next CE.
13	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_CACHE_CO_UE: UE detected on a Cleaner or Castout read (read port0)
14	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_CACHE_CO_SUE: SUE detected on a Cleaner or Castout read (read port0)
15	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_DIR_CE: Directory CE occurred on at least one member during a directory read. An attempt will be made to fix the single bit error.
16	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_DIR_UE: Directory UE occurred on at least one member during a directory read. NOTE: The cache will treat a Directory UE the same as CE in that it will keep trying to fix the error and therefore a timeout will eventually be reported.
17	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_DIR_MEMBER_DELETED: A directory member has been deleted. This can be HW or FW initiated. HW will delete if there is a cache UE on a cache read. FW can setup HW to delete on the next cache CE if the number of CEs exceed a threshold, but FW must monitor the maximum deleted members observed in any congruence class to ensure we do not exceed 15 members deleted in a set.
18	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_DIR_ALL_MEMBERS_DELETED: All 16 members within a particular congruence class have been deleted. This could be due to a UE in each member or PRD allowed too many line deletes on CE.
19	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_LRU_ERROR: invalid LRU value, most likely due to SRAM error. This may impact the performance of the cache, but it is a recoverable error and therefore should not cause a checkstop.
20	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_EDRAM_ERROR: internal eDRAM command collision or eDRAM refresh timeout.
21	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_EMERGENCY_THROTTLE_SET: Emergency Throttle Set
22	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_HOST_INBAND_READ_ERROR: A PIB error or inband buffer error was detected on a host inband read operation.
23	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_HOST_INBAND_WRITE_ERROR: A PIB error or inband buffer error was detected on a host inband write operation.
24	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_OCC_INBAND_READ_ERROR: A PIB error or inband buffer error was detected on a OCC inband read operation.
25	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_OCC_INBAND_WRITE_ERROR: A PIB error or inband buffer error was detected on a OCC inband write operation.
26	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_SRB_BUFFER_CE: CE detected in Shadow Read Buffer
27	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_SRB_BUFFER_UE: UE detected in Shadow Read Buffer

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
28	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_SRB_BUFFER_SUE: SUE detected in Shadow Read Buffer
29	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred
30	RW	WO_AND	WO_OR	MBS_FIR_MASK_REG_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
31:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000

Register Name	***MBS FIR Action 0 Register***
Mnemonic	MBU.MBS.MBS_FIR_ACTION0_REG
Address	0000000002011406 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:30	RO	MBS_FIR_ACTION0_REG_FIR_ACTION0: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,0) = checkstop (0,1,0) = recoverable error (1,0,0) = report unused (1,1,0) = machine check (x,x,1) = error is masked
31:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBS FIR Action 1 Register***
Mnemonic	MBU.MBS.MBS_FIR_ACTION1_REG
Address	0000000002011407 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:30	RO	MBS_FIR_ACTION1_REG_FIR_ACTION1: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,0) = checkstop (0,1,0) = recoverable error (1,0,0) = report unused (1,1,0) = machine check (x,x,1) = error is masked
31:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBS FIR WOF Register***
Mnemonic	MBU.MBS.MBS_FIR_WOF
Address	0000000002011408 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:30	RWX_WCLRREG	MBS_FIR_WOF_FIR_WOF: WOF Register locks on first error..RWX_WCLRREG
31:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBS Address Translate Control Register (MBSXCR)***
Mnemonic	MBU.MBS.ARB.RXLT.MBSXCRQ
Address	000000000201140A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSXCRQ_MBA_ADDRESS_INTERLEAVE_MODE: Controls which the memory buffer address bit is used as the MBA unit select, for address interleave mode: Values: NO_MBA_INTERLEAVE=>0b00000 MBA_SELECT_IS_CENTAUR_ADDRESS_23=>0b10000 MBA_SELECT_IS_CENTAUR_ADDRESS_24=>0b10001 MBA_SELECT_IS_CENTAUR_ADDRESS_25=>0b10010 MBA_SELECT_IS_CENTAUR_ADDRESS_26=>0b10011 MBA_SELECT_IS_CENTAUR_ADDRESS_27=>0b10100 MBA_SELECT_IS_CENTAUR_ADDRESS_28=>0b10101 MBA_SELECT_IS_CENTAUR_ADDRESS_29=>0b10110 MBA_SELECT_IS_CENTAUR_ADDRESS_30=>0b10111 MBA_SELECT_IS_CENTAUR_ADDRESS_31=>0b11000 MBA_SELECT_IS_CENTAUR_ADDRESS_32=>0b11001
5	RW	MBSXCRQ_Z_MODE_CENTAUR_ADDR4_SELECT: Z-only mode. When reset, slave rank 0 is connected to memory buffer address 4. When set, C13 is connected to Centaur address 4 (for ddr3 mode), or R16 is connected to memory buffer address 4 (for ddr4 mode).
6	RW	MBSXCRQ_USE_ALT_CLEANER_CONFIG: When set, use bits 7 to 12 for cleaner rank type, mrank settings
7:8	RW	MBSXCRQ_ALT_CLEANER_RANK_TYPE: Alternate Cleaner Rank Type Setting
9:10	RW	MBSXCRQ_ALT_CLEANER_MRANK0: Alternate Cleaner Master Rank 0 Setting
11:12	RW	MBSXCRQ_ALT_CLEANER_MRANK1: Alternate Cleaner Master Rank 1 Setting
13	RW	MBSXCRQ_USE_ALT_PREFETCH_CONFIG: When set, use bits 14 to 20 for prefetch refresh avoidance settings
14:17	RW	MBSXCRQ_ALT_PREFETCH_RANK_LOCATION: Alternate Prefetch Rank Location Setting
18:20	RW	MBSXCRQ_ALT_PREFETCH_RANK_TYPE: Alternate Prefetch Rank Type Setting
21:31	RW	MBSXCRQ_RESERVED_21_31: Reserved
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBA01 Address Translate Control Register (MBAXCR01)***
Mnemonic	MBU.MBS.ARB.RXLT.MBAXCR01Q
Address	000000000201140B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAXCR01Q_MBA01_CONFIG_TYPE: Specifies memory configuration type: Values: NO_MEMORY_POPULATED_BEHIND_MBA01=>0b0000 TYPE1_MEMORY_POPULATED_BEHIND_MBA01=>0b0001 TYPE2_MEMORY_POPULATED_BEHIND_MBA01=>0b0010 TYPE3_MEMORY_POPULATED_BEHIND_MBA01=>0b0011 TYPE4_MEMORY_POPULATED_BEHIND_MBA01=>0b0100 TYPE5_MEMORY_POPULATED_BEHIND_MBA01=>0b0101 TYPE6_MEMORY_POPULATED_BEHIND_MBA01=>0b0110 TYPE7_MEMORY_POPULATED_BEHIND_MBA01=>0b0111 TYPE8_MEMORY_POPULATED_BEHIND_MBA01=>0b1000
4:5	RW	MBAXCR01Q_MBA01_CONFIG_SUBTYPE: Specifies memory configuration subtype: Values: SUBTYPE_A=>0b00 SUBTYPE_B=>0b01 SUBTYPE_C=>0b10 SUBTYPE_D=>0b11
6:7	RW	MBAXCR01Q_MBA01_DRAM_SIZE: DRAM size: 11 = Reserved Values: 2GB=>0b00 4GB=>0b01 8GB=>0b10
8	RW	MBAXCR01Q_MBA01_CONFIGURATION: Memory Configuration: Values: CENTAUR_OR_PLANAR_DIMM_WITH_ONLY_DIMM_SLOT0_POPULATED=>0b0 PLANAR_DIMM_WITH_BOTH_DIMM_SLOTS_0_AND_1_POPULATED=>0b1
9	RW	MBAXCR01Q_MBA01_DRAM_WIDTH: DRAM width: Values: X8=>0b0 X4=>0b1
10:11	RW	MBAXCR01Q_MBA01_HASH_MODE: Hash mode select 11 = reserved Values: HASH_MODE_0=>0b00 HASH_MODE_1=>0b01 HASH_MODE_2=>0b10
12	RW	MBAXCR01Q_MBA01_INTERLEAVE_MODE: Interleave mode - when set, column bit 3 maps to MBA address 32, else bankbank group bits map to MBA address 32
13:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	***MBA23 Address Translate Control Register (MBAXCR23)***
Mnemonic	MBU.MBS.ARB.RXLT.MBAXCR23Q
Address	000000000201140C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAXCR23Q_MBA23_CONFIG_TYPE: Specifies memory configuration type: Values: NO_MEMORY_POPULATED_BEHIND_MBA23=>0b0000 TYPE1_MEMORY_POPULATED_BEHIND_MBA23=>0b0001 TYPE2_MEMORY_POPULATED_BEHIND_MBA23=>0b0010 TYPE3_MEMORY_POPULATED_BEHIND_MBA23=>0b0011 TYPE4_MEMORY_POPULATED_BEHIND_MBA23=>0b0100 TYPE5_MEMORY_POPULATED_BEHIND_MBA23=>0b0101 TYPE6_MEMORY_POPULATED_BEHIND_MBA23=>0b0110 TYPE7_MEMORY_POPULATED_BEHIND_MBA23=>0b0111 TYPE8_MEMORY_POPULATED_BEHIND_MBA23=>0b1000
4:5	RW	MBAXCR23Q_MBA23_CONFIG_SUBTYPE: Specifies memory configuration subtype: Values: SUBTYPE_A=>0b00 SUBTYPE_B=>0b01 SUBTYPE_C=>0b10 SUBTYPE_D=>0b11
6:7	RW	MBAXCR23Q_MBA23_DRAM_SIZE: DRAM size: 11 = Reserved Values: 2GB=>0b00 4GB=>0b01 8GB=>0b10
8	RW	MBAXCR23Q_MBA23_CONFIGURATION: Memory Configuration: Values: CENTAUR_OR_PLANAR_DIMM_WITH_ONLY_DIMM_SLOT0_POPULATED=>0b0 PLANAR_DIMM_WITH_BOTH_DIMM_SLOTS_0_AND_1_POPULATED=>0b1
9	RW	MBAXCR23Q_MBA23_DRAM_WIDTH: DRAM width: Values: X8=>0b0 X4=>0b1
10:11	RW	MBAXCR23Q_MBA23_HASH_MODE: Hash mode select 11 = reserved Values: HASH_MODE_0=>0b00 HASH_MODE_1=>0b01 HASH_MODE_2=>0b10
12	RW	MBAXCR23Q_MBA23_INTERLEAVE_MODE: Interleave mode - when set, column bit 3 maps to MBA address 32, else bankbank group bits map to MBA address 32
13:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Swizzle Control Register (MBAXCRMS)***
Mnemonic	MBU.MBS.ARB.RXLT.MBAXCRMSQ
Address	000000000201140D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MBAXCRMSQ_MBA01_MASTER_RANK_0_SELECT: Values: MASTER_RANK_0_IS_M0=>0b000 MASTER_RANK_0_IS_M1=>0b001 MASTER_RANK_0_IS_M2=>0b010 MASTER_RANK_0_IS_S0=>0b011 MASTER_RANK_0_IS_S1=>0b100 MASTER_RANK_0_IS_S2=>0b101 MASTER_RANK_0_IS_B2_DDR3__B0_DDR4=>0b110 MASTER_RANK_0_IS_B0_DDR3__B1_DDR4=>0b111
3:5	RW	MBAXCRMSQ_MBA01_MASTER_RANK_1_SELECT: Values: MASTER_RANK_1_IS_M0=>0b000 MASTER_RANK_1_IS_M1=>0b001 MASTER_RANK_1_IS_M2=>0b010 MASTER_RANK_1_IS_S0=>0b011 MASTER_RANK_1_IS_S1=>0b100 MASTER_RANK_1_IS_S2=>0b101 MASTER_RANK_1_IS_B2_DDR3__B0_DDR4=>0b110 MASTER_RANK_1_IS_B0_DDR3__B1_DDR4=>0b111
6:8	RW	MBAXCRMSQ_MBA01_MASTER_RANK_2_SELECT: Values: MASTER_RANK_2_IS_M0=>0b000 MASTER_RANK_2_IS_M1=>0b001 MASTER_RANK_2_IS_M2=>0b010 MASTER_RANK_2_IS_S0=>0b011 MASTER_RANK_2_IS_S1=>0b100 MASTER_RANK_2_IS_S2=>0b101 MASTER_RANK_2_IS_B2_DDR3__B0_DDR4=>0b110 MASTER_RANK_2_IS_B0_DDR3__B1_DDR4=>0b111
9:11	RW	MBAXCRMSQ_MBA01_SLAVE_RANK_0_SELECT: Values: SLAVE_RANK_0_IS_M0=>0b000 SLAVE_RANK_0_IS_M1=>0b001 SLAVE_RANK_0_IS_M2=>0b010 SLAVE_RANK_0_IS_S0=>0b011 SLAVE_RANK_0_IS_S1=>0b100 SLAVE_RANK_0_IS_S2=>0b101 SLAVE_RANK_0_IS_B2_DDR3__B0_DDR4=>0b110 SLAVE_RANK_0_IS_B0_DDR3__B1_DDR4=>0b111
12:14	RW	MBAXCRMSQ_MBA01_SLAVE_RANK_1_SELECT: Values: SLAVE_RANK_1_IS_M0=>0b000 SLAVE_RANK_1_IS_M1=>0b001 SLAVE_RANK_1_IS_M2=>0b010 SLAVE_RANK_1_IS_S0=>0b011 SLAVE_RANK_1_IS_S1=>0b100 SLAVE_RANK_1_IS_S2=>0b101 SLAVE_RANK_1_IS_B2_DDR3__B0_DDR4=>0b110 SLAVE_RANK_1_IS_B0_DDR3__B1_DDR4=>0b111
15:17	RW	MBAXCRMSQ_MBA01_SLAVE_RANK_2_SELECT: Values: SLAVE_RANK_2_IS_M0=>0b000 SLAVE_RANK_2_IS_M1=>0b001 SLAVE_RANK_2_IS_M2=>0b010 SLAVE_RANK_2_IS_S0=>0b011 SLAVE_RANK_2_IS_S1=>0b100 SLAVE_RANK_2_IS_S2=>0b101 SLAVE_RANK_2_IS_B2_DDR3__B0_DDR4=>0b110 SLAVE_RANK_2_IS_B0_DDR3__B1_DDR4=>0b111

Bits	SCOM	Field Mnemonic: Description
18:20	RW	MBAXCRMSQ_MBA01_B2_DDR3_B0_DDR4_SELECT: Values: B2B0_IS_M0=>0b000 B2B0_IS_M1=>0b001 B2B0_IS_M2=>0b010 B2B0_IS_S0=>0b011 B2B0_IS_S1=>0b100 B2B0_IS_S2=>0b101 B2B0_IS_B2_DDR3__B0_DDR4=>0b110 B2B0_IS_B0_DDR3__B1_DDR4=>0b111
21:23	RW	MBAXCRMSQ_MBA01_B0_DDR3_B1_DDR4_SELECT: Values: B0B1_IS_M0=>0b000 B0B1_IS_M1=>0b001 B0B1_IS_M2=>0b010 B0B1_IS_S0=>0b011 B0B1_IS_S1=>0b100 B0B1_IS_S2=>0b101 B0B1_IS_B2_DDR3__B0_DDR4=>0b110 B0B1_IS_B0_DDR3__B1_DDR4=>0b111
24:26	RW	MBAXCRMSQ_MBA23_MASTER_RANK_0_SELECT: Values: MASTER_RANK_0_IS_M0=>0b000 MASTER_RANK_0_IS_M1=>0b001 MASTER_RANK_0_IS_M2=>0b010 MASTER_RANK_0_IS_S0=>0b011 MASTER_RANK_0_IS_S1=>0b100 MASTER_RANK_0_IS_S2=>0b101 MASTER_RANK_0_IS_B2_DDR3__B0_DDR4=>0b110 MASTER_RANK_0_IS_B0_DDR3__B1_DDR4=>0b111
27:29	RW	MBAXCRMSQ_MBA23_MASTER_RANK_1_SELECT: Values: MASTER_RANK_1_IS_M0=>0b000 MASTER_RANK_1_IS_M1=>0b001 MASTER_RANK_1_IS_M2=>0b010 MASTER_RANK_1_IS_S0=>0b011 MASTER_RANK_1_IS_S1=>0b100 MASTER_RANK_1_IS_S2=>0b101 MASTER_RANK_1_IS_B2_DDR3__B0_DDR4=>0b110 MASTER_RANK_1_IS_B0_DDR3__B1_DDR4=>0b111
30:32	RW	MBAXCRMSQ_MBA23_MASTER_RANK_2_SELECT: Values: MASTER_RANK_2_IS_M0=>0b000 MASTER_RANK_2_IS_M1=>0b001 MASTER_RANK_2_IS_M2=>0b010 MASTER_RANK_2_IS_S0=>0b011 MASTER_RANK_2_IS_S1=>0b100 MASTER_RANK_2_IS_S2=>0b101 MASTER_RANK_2_IS_B2_DDR3__B0_DDR4=>0b110 MASTER_RANK_2_IS_B0_DDR3__B1_DDR4=>0b111
33:35	RW	MBAXCRMSQ_MBA23_SLAVE_RANK_0_SELECT: Values: SLAVE_RANK_0_IS_M0=>0b000 SLAVE_RANK_0_IS_M1=>0b001 SLAVE_RANK_0_IS_M2=>0b010 SLAVE_RANK_0_IS_S0=>0b011 SLAVE_RANK_0_IS_S1=>0b100 SLAVE_RANK_0_IS_S2=>0b101 SLAVE_RANK_0_IS_B2_DDR3__B0_DDR4=>0b110 SLAVE_RANK_0_IS_B0_DDR3__B1_DDR4=>0b111

Bits	SCOM	Field Mnemonic: Description
36:38	RW	MBAXCRMSQ_MBA23_SLAVE_RANK_1_SELECT: Values: SLAVE_RANK_1_IS_M0=>0b000 SLAVE_RANK_1_IS_M1=>0b001 SLAVE_RANK_1_IS_M2=>0b010 SLAVE_RANK_1_IS_S0=>0b011 SLAVE_RANK_1_IS_S1=>0b100 SLAVE_RANK_1_IS_S2=>0b101 SLAVE_RANK_1_IS_B2_DDR3__B0_DDR4=>0b110 SLAVE_RANK_1_IS_B0_DDR3__B1_DDR4=>0b111
39:41	RW	MBAXCRMSQ_MBA23_SLAVE_RANK_2_SELECT: Values: SLAVE_RANK_2_IS_M0=>0b000 SLAVE_RANK_2_IS_M1=>0b001 SLAVE_RANK_2_IS_M2=>0b010 SLAVE_RANK_2_IS_S0=>0b011 SLAVE_RANK_2_IS_S1=>0b100 SLAVE_RANK_2_IS_S2=>0b101 SLAVE_RANK_2_IS_B2_DDR3__B0_DDR4=>0b110 SLAVE_RANK_2_IS_B0_DDR3__B1_DDR4=>0b111
42:44	RW	MBAXCRMSQ_MBA23_B2_DDR3_B0_DDR4_SELECT: Values: B2B0_IS_M0=>0b000 B2B0_IS_M1=>0b001 B2B0_IS_M2=>0b010 B2B0_IS_S0=>0b011 B2B0_IS_S1=>0b100 B2B0_IS_S2=>0b101 B2B0_IS_B2_DDR3__B0_DDR4=>0b110 B2B0_IS_B0_DDR3__B1_DDR4=>0b111
45:47	RW	MBAXCRMSQ_MBA23_B0_DDR3_B1_DDR4_SELECT: Values: B0B1_IS_M0=>0b000 B0B1_IS_M1=>0b001 B0B1_IS_M2=>0b010 B0B1_IS_S0=>0b011 B0B1_IS_S1=>0b100 B0B1_IS_S2=>0b101 B0B1_IS_B2_DDR3__B0_DDR4=>0b110 B0B1_IS_B0_DDR3__B1_DDR4=>0b111
48:63	RO	constant=0b0000000000000000 Values: B0B1_IS_M0=>0b000 B0B1_IS_M1=>0b001 B0B1_IS_M2=>0b010 B0B1_IS_S0=>0b011 B0B1_IS_S1=>0b100 B0B1_IS_S2=>0b101 B0B1_IS_B2_DDR3__B0_DDR4=>0b110 B0B1_IS_B0_DDR3__B1_DDR4=>0b111

Register Name	***MBS Error Injection Register***
Mnemonic	MBU.MBS.MBSEINJQ
Address	000000000201140E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSEINJQ_CACHE_WP0_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note that this injection is applied to write port 0 of the cache, of which there are two write ports. The types of operations that use write port 0 include DS Writes, DS Partial Writes, and DS Read Miss allocations due to SFstat updates, while Prefetch and all other Read Miss allocations use write port 1. Note that if the cache is disabled, this will inject errors in the write data path to the MBA. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
1	RW	MBSEINJQ_CACHE_WP0_ERR_INJECT_CE: Inject a CE when writing into write port0 of the eDRAM cache.
2	RW	MBSEINJQ_CACHE_WP0_ERR_INJECT_UE: Inject a UE when writing into write port0 of the eDRAM cache.
3	RW	MBSEINJQ_CACHE_WP0_ERR_INJECT_SUE: Inject a SUE when writing into write port0 of the eDRAM cache.
4	RW	MBSEINJQ_DIRECTORY_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
5	RW	MBSEINJQ_DIRECTORY_ERR_INJECT_CE: Inject a CE when reading the SRAM directory.
6	RW	MBSEINJQ_DIRECTORY_ERR_INJECT_UE: Inject a UE when reading the SRAM directory.
7	RW	MBSEINJQ_SWB_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note this injection is applied to the data buffer that holds Downstream write data and is referred to as the Shadow Write Buffer. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
8	RW	MBSEINJQ_SWB_ERR_INJECT_CE: Inject a CE when writing into the SWB.
9	RW	MBSEINJQ_SWB_ERR_INJECT_UE: Inject a UE when writing into the SWB.
10	RW	MBSEINJQ_SRB_RP0_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note that this injection is applied to the read port 0 of the data buffer that holds Shadow read data, of which there are two read ports. Read Port 0 is used to transfer read data Upstream. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
11	RW	MBSEINJQ_SRB_RP0_ERR_INJECT_CE: Inject a CE when reading the SRB read port 0.
12	RW	MBSEINJQ_SRB_RP0_ERR_INJECT_UE: Inject a UE when reading the SRB read port 0.
13	RW	MBSEINJQ_SRB_RP1_ERROR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note that this injection is applied to the read port 1 of the data buffer that holds Shadow read data, of which there are two read ports. Read Port 1 is used to service a read cache miss allocation, a partial write merge with SWB data, or SFstat update on a DS read. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
14	RW	MBSEINJQ_SRB_RP1_ERROR_INJECT_CE: Inject a CE when reading the SRB read port 1.
15	RW	MBSEINJQ_SRB_RP1_ERROR_INJECT_UE: Inject a UE when reading the SRB read port 1.
16	RW	MBSEINJQ_PFB_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note that this injection is applied to the Prefetch read data buffer, which is used to write prefetch data into the cache. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
17	RW	MBSEINJQ_PFB_ERR_INJECT_CE: Inject a CE when reading the PFB.
18	RW	MBSEINJQ_PFB_ERR_INJECT_UE: Inject a UE when reading the PFB.

Bits	SCOM	Field Mnemonic: Description
19	RW	MBSEINJQ_SPWA_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Not that this injection is applied to the Shadow Partial Write Attributes buffer, which is used to store DS partial write command attributes such as tsize and function. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
20	RW	MBSEINJQ_SPWA_ERR_INJECT_PERR: Inject a parity error when writing the SPWA
21	RW	MBSEINJQ_CO_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note that this injection is applied to the cache read port 0, which is used for casting out data from the cache to MBA. The cache read port 1 is used to read data into the Shadow Read Buffer. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
22	RW	MBSEINJQ_CO_ERR_INJECT_CE: Inject a CE when performing a CO of the cache.
23	RW	MBSEINJQ_CO_ERR_INJECT_UE: Inject a UE when performing a CO of the cache.
24	RW	MBSEINJQ_INT_RESET_KEEPER: Writing this bit to a 1 will pulse the reset of the hold latches in the MBS c_err_rpt's.
25	RW	MBSEINJQ_RESERVED_25: reserved
26	RW	MBSEINJQ_RESERVED_26: reserved
27	RW	MBSEINJQ_IB_BFR_ERR_INJECT_MODE: Used to control whether the error injection is once or continuous. Note that this injection is applied to the inband read/write buffer. Values: ONE_SHOT=>0b0 CONTINUOUS=>0b1
28	RW	MBSEINJQ_IB_BFR_ERR_INJECT_CE: Inject a CE when performing an inband read or write operation.
29	RW	MBSEINJQ_IB_BFR_ERR_INJECT_UE: Inject a UE when performing an inband read or write operation.
30	RW	MBSEINJQ_DIRECTORY_ERR_INJECT_ADDR_PERR: Inject an Address parity error when reading the SRAM directory. Used in conjunction with directory_err_inject_mode (bit 5 of this register) to control pulse or level.
31	RW	MBSEINJQ_RRQ_POP_INJECT_POP: Inject an unexpected rrq pop to drive internal protocol error MBS FIR. Used in conjunction with directory_err_inject_mode (bit 5 of this register) to control pulse or level.
32	RW	MBSEINJQ_RRQ_POP_INJECT_PERR: Inject an error on the MBX->MBS RRQ pop interface for both MBA23 and MBA01 to set internal parity error MBS FIR.
33	RW	MBSEINJQ_SHORT_HANG_TIMER: When set, reduce the SRWPFCLN hang timer to 32 MBS cycles or 27ns
34	RW	MBSEINJQ_LRU_ERR_INJ: When set, inject an error in the lru information
35:63	RO	constant=0b00000000000000000000000000000

Register Name	***MBC Configuration Register***
Mnemonic	MBU.MBS.MBCCFGQ
Address	000000000201140F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBCCFGQ_CACHE_ENABLE: 1-Enable the MBC cache 0-disable the MBC cache
1	RW	MBCCFGQ_CFG_DYN_WHAP_EN: 0- whap algorithm uses programmed values for miss allocate and hit increment reference counts. 1- whap algorithm can dynamically override the programmed values for miss allocate and hit increment reference counts based on history.

Bits	SCOM	Field Mnemonic: Description
2	RW	MBCCFGQ_CLEANER_ENABLE: Turns on the cache cleaner functionality. Note that that the cleaner should not be turned on if the memory buffer is not setup to have 32KB address hashing. 00 = OFF 11 = ON
3	RW	MBCCFGQ_CACHE_ONLY_ENABLE: Special system configuration where the cache is enabled, but the DRAM is not initialized. Software is responsible that MBC does not need to perform a Castout of Modified data. If a CO is started, this mode will prevent the CO from actually making it to the MBA.
4	RW	MBCCFGQ_LRU_DMAP_EN: Enable direct mapped LRU mode. Do not set this in conjunction with lru_random_en or lru_single_mem_en.
5	RW	MBCCFGQ_LRU_RANDOM_EN: Enable random LRU mode. Do not set this in conjunction with lru_dmap_en or lru_single_mem_en.
6	RW	MBCCFGQ_LRU_SINGLE_MEM_EN: Enables only member 0 in each congruence class. Do not set this in conjunction with lru_dmap_en or lru_random_en. NOTE: there are scan only modes to disable each member on an individual basis and these modes should NOT be used in conjunction with lru_dmap_en, lru_random_en, or lru_single_mem_en. NOTE: Purge cannot be used in conjunction with this mode being set as this mode is only for hw stress.
7	RW	MBCCFGQ_CFG_SRW_DELETE_UE_EN: When set, the Shadow RW machine will line-delete a cache entry by writing to the Id state (instead of I) when purging a cache-line that experienced a cache UE.
8	RW	MBCCFGQ_SRW_LINE_DELETE_NEXT_CE_EN: When set, the Shadow RW machine will line-delete a cache entry by writing to the Id state (instead of I) during the next purge associated with a cache CE. In addition, cache_srw_ce and cache_co_ce MBSFIR bits will not be set if a cache CE is detected between setting srw_line_delete_next_ce_en and the Shadow machine performing a line delete.
9	RW	MBCCFGQ_ONLY_LOG_ECC_UE: When set, we will only log Cache UE errors. Default
10	RW	MBCCFGQ_ONLY_LOG_ECC_CE: When set, we will only log Cache CE errors
11	RW	MBCCFGQ_SRW_PREFETCH_DIS: When the cache is enabled, disable SRW machines from linking with Prefetch machines to create a 256B prefetch operation in conjunction with a down stream prefetch command.
12	RW	MBCCFGQ_PRQ_PREFETCH_DIS: Setting this bit will disable the extended prefetch engine (PRQ) regardless of the DS command encoding.
13:16	RW	MBCCFGQ_CLN_PAGE_MODE_BUNDLE_MAX_CNT_0_3: Maximum number extra cache lines bundled with the original cleaned line in a rank group transfer to MBA which map to the same DRAM page.
17:22	RW	MBCCFGQ_CLN_WRQ_TGT_ALLOC_0_5: Programmable target allocation in wrq for a given rank group. Range is from 1 to 32. Typically, will allow this to equal 8 for 8 rank group config, 16 for 4 rank group config, and 32 for 2 rank group config. Default is 8.
23:28	RW	MBCCFGQ_CLN_WR_PRIORITY_WRQ_HWMARK_0_5: Programmable hi-water mark for the cleaner shadow wrq count for write priority purposes. Indicates that a max number of wrq count has been detected for a given rank group such that there is enough work for the mba to drain a bundle when in write priority mode. Range is from 2 to cln_wrq_tgt_alloc-1. Default is 6.
29:34	RW	MBCCFGQ_CLN_WR_PRIORITY_WRQ_LWMARK_0_5: Programmable low-water mark for the cleaner shadow wrq count for write priority purposes. Indicates that a min number of wrq count has been detected for a given rank group such that the write priority signal can be dropped and mba returned to normal. Range is from 1 to cln_wr_priority_wrq_hwmark-1.Default is 4.
35:48	RW	MBCCFGQ_CLN_WR_PRIORITY_DV_HWMARK_0_13: The cleaner will tell the MBA to make writes high priority if the number of cgc's that are dirty are greater than the value stored in this field. The Cleaner will maintain this high priority write signal until the number of dirty sets goes below the value stored in MBS_cln_wr_priority_dv_lwmark. The Range is from drain_length to 8k-1, where drain_length is the difference between MBS_cln_wr_priority_dv_hwmark and MBS_cln_wr_priority_dv_lwmark. Default is 4k.
49:62	RW	MBCCFGQ_CLN_WR_PRIORITY_DV_LWMARK_0_13: Once triggerd by cln_wr_priority_dv_hwmark, the Cleaner will maintain the high priority write signal until the number of dirty sets goes below the value stored in this value. Range is from 1 to 8k-drain_length, where drain_length is the difference between MBS_cln_wr_priority_dv_hwmark and cln_wr_priority_dv_lwmark. Default is 4k-16.
63	RW	MBCCFGQ_RESERVED_63: Reserved bits that do not actually exist

Register Name	*MBCD Charge Pump Mode Register*
Mnemonic	MBU.MBS.MBCDCPMQ
Address	0000000002011410 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBCDCPMQ_MBCD0_CP_UTIL_EN_DC: When set, enables charge pump monitoring
1:2	RW	MBCDCPMQ_MBCD0_CP_UTIL_SEL_DC_0_1: Selects internal reference source for charge pump monitoring.
3:5	RW	MBCDCPMQ_MBCD0_CP_UTIL_EXT_SEL_0_2: Extent selects for charge pump monitoring
6:11	ROX	MBCDCPMQ_MBCD0_CP_UTIL_MON_BITS_0_5: Charge pump monitor outputs
12	RW	MBCDCPMQ_MBCD1_CP_UTIL_EN_DC: When set, enables charge pump monitoring
13:14	RW	MBCDCPMQ_MBCD1_CP_UTIL_SEL_DC_0_1: Selects internal reference source for charge pump monitoring.
15:17	RW	MBCDCPMQ_MBCD1_CP_UTIL_EXT_SEL_0_2: Extent selects for charge pump monitoring
18:23	ROX	MBCDCPMQ_MBCD1_CP_UTIL_MON_BITS_0_5: Charge pump monitor outputs
24:63	RO	constant=0b000000000000000000000000000000000000000000000000

Register Name	*MBS Configuration Register*
Mnemonic	MBU.MBS.MBSCFGQ
Address	0000000002011411 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSCFGQ_ECCBP_EXIT_SEL: When written from a 0 to a 1, the following sequence will be invoked: 1.) flush all outstanding DRAM reads and writes in the MBA units 2.) select ECC bypass exit point 1 for ecc bypass dataflow 3.) set MBSSQ(1)=eccbp_exit1_selected. When written from a 1 to a 0, the following sequence will be invoked: 1.) flush all outstanding DRAM reads and writes in the MBA units 2.) select ECC bypass exit point 0 for ecc bypass data flow. 3.) clear MBSSQ(1)=eccbp_exit1_selected.
1	RW	MBSCFGQ_DRAM_ECC_BYPASS_DIS: When this bit is set, POWER8 Processor DRAM ECC bypass is disabled
2:6	RW	MBSCFGQ_RSV2_6: reserved
7:10	RW	MBSCFGQ_OCC_DEADMAN_TIMER_SEL: selects one of 8 time-out values for the occ dead man timer. If the OCC is idle for the programmed time-out value, the MBS will issue an emergency throttle command to the MBA. Value Time 0000 Disabled 0001 100 ms 0010 448 ms 0011 896 ms 0100 1792 ms 0101 3584 ms 0110 7168 ms 0111 14336 ms 1000 28672 ms 1001 to 1111 are unused.
11	RW	MBSCFGQ_SYNC_FSYNC_MBA_STROBE_EN: Enable fsync after pll lock when the memory buffer is configured to run MBA synchronous with MBS.
12	RW	MBSCFGQ_HCA_TIMEBASE_OP_MODE: When set, the hca timebase pulses every 116 of a second. When reset, the hca timebase pulses every 2048 MBS clocks. Memory buffer only.

Bits	SCOM	Field Mnemonic: Description
13:15	RW	MBSCFGQ_HCA_LOCAL_TIMER_INC_SELECT: Selects number of hca timebase pulses for each local timer increment. Memory buffer only Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100

Register Name	***MBS HCA Accumulator Register***
Mnemonic	MBU.MBS.MBSACUMQ
Address	0000000002011412 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RWX	MBSACUMQ_HCA_DECAY_UPDATE_EVENDW: HCA decay update accumulator latch for even doublewords
16:31	RWX	MBSACUMQ_HCA_DECAY_UPDATE_ODDDW: HCA decay update accumulator latch for odd doublewords
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBS Error Report Hold Register1***
Mnemonic	MBU.MBS.MBSCERR1Q
Address	0000000002011413 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBSCERR1Q_MBCD0_RP0_CE: MBSFIR(12) : MBC Read Port0 CE (Castout) cerr_hold
1	RWX	MBSCERR1Q_MBCD0_RP0_UE: MBSFIR(13) : MBC Read Port0 UE (Castout) cerr_hold
2	RWX	MBSCERR1Q_MBCD0_RP0_SUE: MBSFIR(14) : MBC Read Port0 SUE (Castout) cerr_hold
3	RWX	MBSCERR1Q_MBCD1_RP0_CE: MBSFIR(12) : MBC Read Port0 CE (Castout) cerr_hold
4	RWX	MBSCERR1Q_MBCD1_RP0_UE: MBSFIR(13) : MBC Read Port0 UE (Castout) cerr_hold
5	RWX	MBSCERR1Q_MBCD1_RP0_SUE: MBSFIR(14) : MBC Read Port0 SUE (Castout) cerr_hold
6	RWX	MBSCERR1Q_MBCD0_RP1_CE: MBSFIR(9) : MBC Read Port1 CE (Shadow) cerr_hold
7	RWX	MBSCERR1Q_MBCD0_RP1_UE: MBSFIR(10) : MBC Read Port1 UE (Shadow) cerr_hold
8	RWX	MBSCERR1Q_MBCD0_RP1_SUE: MBSFIR(11) : MBC Read Port1 SUE (Shadow) cerr_hold
9	RWX	MBSCERR1Q_MBCD1_RP1_CE: MBSFIR(9) : MBC Read Port1 CE (Shadow) cerr_hold
10	RWX	MBSCERR1Q_MBCD1_RP1_UE: MBSFIR(10) : MBC Read Port1 UE (Shadow) cerr_hold

Bits	SCOM	Field Mnemonic: Description
11	RWX	MBSCERR1Q_MBCD1_RP1_SUE: MBSFIR(11) : MBC Read Port1 SUE (Shadow) cerr_hold
12	RWX	MBSCERR1Q_SRB_RP0_EVEN_CE: MBSFIR(26) : Shadow Read Buffer Read Port 0 CE (US) cerr_hold
13	RWX	MBSCERR1Q_SRB_RP0_EVEN_UE: MBSFIR(27) : Shadow Read Buffer Read Port 0 UE (US) cerr_hold
14	RWX	MBSCERR1Q_SRB_RP0_EVEN_SUE: MBSFIR(28) : Shadow Read Buffer Read Port 0 SUE (US) cerr_hold
15	RWX	MBSCERR1Q_SRB_RP0_ODD_CE: MBSFIR(26) : Shadow Read Buffer Read Port 0 CE (US) cerr_hold
16	RWX	MBSCERR1Q_SRB_RP0_ODD_UE: MBSFIR(27) : Shadow Read Buffer Read Port 0 UE (US) cerr_hold
17	RWX	MBSCERR1Q_SRB_RP0_ODD_SUE: MBSFIR(28) : Shadow Read Buffer Read Port 0 SUE (US) cerr_hold
18	RWX	MBSCERR1Q_SRB_RP1_EVEN_CE: MBSFIR(26) : Shadow Read Buffer Read Port 1 CE (RMW, Allocate) cerr_hold
19	RWX	MBSCERR1Q_SRB_RP1_EVEN_UE: MBSFIR(27) : Shadow Read Buffer Read Port 1 UE (RMW, Allocate) cerr_hold
20	RWX	MBSCERR1Q_SRB_RP1_EVEN_SUE: MBSFIR(28) : Shadow Read Buffer Read Port 1 SUE (RMW, Allocate) cerr_hold
21	RWX	MBSCERR1Q_SRB_RP1_ODD_CE: MBSFIR(26) : Shadow Read Buffer Read Port 1 CE (RMW, Allocate) cerr_hold
22	RWX	MBSCERR1Q_SRB_RP1_ODD_UE: MBSFIR(27) : Shadow Read Buffer Read Port 1 UE (RMW, Allocate) cerr_hold
23	RWX	MBSCERR1Q_SRB_RP1_ODD_SUE: MBSFIR(28) : Shadow Read Buffer Read Port 1 SUE (RMW, Allocate) cerr_hold
24	RWX	MBSCERR1Q_PFB0_CE: MBSFIR(5) : Prefetch Read Buffer CE cerr_hold
25	RWX	MBSCERR1Q_PFB0_UE: MBSFIR(6) : Prefetch Read Buffer UE cerr_hold
26	RWX	MBSCERR1Q_PFB0_SUE: MBSFIR(7) : Prefetch Read Buffer SUE cerr_hold
27	RWX	MBSCERR1Q_PFB1_CE: MBSFIR(5) : Prefetch Read Buffer CE cerr_hold
28	RWX	MBSCERR1Q_PFB1_UE: MBSFIR(6) : Prefetch Read Buffer UE cerr_hold
29	RWX	MBSCERR1Q_PFB1_SUE: MBSFIR(7) : Prefetch Read Buffer SUE cerr_hold
30	RWX	MBSCERR1Q_PFB2_CE: MBSFIR(5) : Prefetch Read Buffer CE cerr_hold
31	RWX	MBSCERR1Q_PFB2_UE: MBSFIR(6) : Prefetch Read Buffer UE cerr_hold
32	RWX	MBSCERR1Q_PFB2_SUE: MBSFIR(7) : Prefetch Read Buffer SUE cerr_hold
33	RWX	MBSCERR1Q_PFB3_CE: MBSFIR(5) : Prefetch Read Buffer CE cerr_hold
34	RWX	MBSCERR1Q_PFB3_UE: MBSFIR(6) : Prefetch Read Buffer UE cerr_hold
35	RWX	MBSCERR1Q_PFB3_SUE: MBSFIR(7) : Prefetch Read Buffer SUE cerr_hold
36	RWX	MBSCERR1Q_WRQA01_PE: MBSFIR(8) : WRQ 01Address Parity error cerr_hold
37	RWX	MBSCERR1Q_WRQA23_PE: MBSFIR(8) : WRQ 23Address Parity error cerr_hold
38	RWX	MBSCERR1Q_SRWADD_PE: MBSFIR(8) : Shadow RQ Address Parity error cerr_hold
39	RWX	MBSCERR1Q_DADDP_PE: MBSFIR(8) : Dispatch Address Pipe Parity error cerr_hold
40	RWX	MBSCERR1Q_SWPAB_PE: MBSFIR(8) : Shadow RMW Attribute Buffer Parity error cerr_hold
41	RWX	MBSCERR1Q_SWB_EVEN_CE: MBSFIR(5) : Shadow Write Buffer CE cerr_hold
42	RWX	MBSCERR1Q_SWB_EVEN_UE: MBSFIR(6) : Shadow Write Buffer UE cerr_hold
43	RWX	MBSCERR1Q_SWB_EVEN_SUE: MBSFIR(7) : Shadow Write Buffer SUE cerr_hold
44	RWX	MBSCERR1Q_SWB_ODD_CE: MBSFIR(5) : Shadow Write Buffer CE cerr_hold
45	RWX	MBSCERR1Q_SWB_ODD_UE: MBSFIR(6) : Shadow Write Buffer UE cerr_hold
46	RWX	MBSCERR1Q_SWB_ODD_SUE: MBSFIR(7) : Shadow Write Buffer SUE cerr_hold

Bits	SCOM	Field Mnemonic: Description
47	RWX	MBSCERR1Q_SRW_PWRT_SIZE_ERR: MBSFIR(0) : Incorrect size on DS partial write command
48	RWX	MBSCERR1Q_WBMGR_WRQ01_IDX_ERR: MBSFIR(1) : WRQ01 index protocol error with MBS
49	RWX	MBSCERR1Q_WBMGR_WRQ23_IDX_ERR: MBSFIR(1) : WRQ23 index protocol error with MBS
50	RWX	MBSCERR1Q_CLNFSM_TIMEOUT_ERR: MBSFIR(4) : Cleaner FSM timeout
51	RWX	MBSCERR1Q_COADD_ADDR_ERR: MBSFIR(2) : Castout address translation error
52	RWX	MBSCERR1Q_DIR_ADDR_PARITY_ERR: MBSFIR(8) : Directory address bus parity error
53	RWX	MBSCERR1Q_DISP_INVALID_DS_CMD_ERR: MBSFIR(0) : invalid ds cmd
54	RWX	MBSCERR1Q_DISP_INVALID_ADDR_ERR: MBSFIR(2) : invalid ds addr
55	RWX	MBSCERR1Q_DISP_INVALID_CAC_ONLY_ERR: MBSFIR(0) : invalid cache only mode error, such as valid CO, PF, or CLN FSM operation in disp pipe.
56	RWX	MBSCERR1Q_DISP_LRU_ID_ERR: MBSFIR(19) : disp given deleted LRU victim
57	RWX	MBSCERR1Q_DISP_RRQ01_CNT_PARITY_ERR: MBSFIR(8) : disp rrq01 counter parity error
58	RWX	MBSCERR1Q_DISP_RRQ23_CNT_PARITY_ERR: MBSFIR(8) : disp rrq23counter parity error
59	RWX	MBSCERR1Q_DISP_RRQ01_OVERFLOW_ERR: MBSFIR(1) : disp rrq01 counter overflow error
60	RWX	MBSCERR1Q_DISP_RRQ23_OVERFLOW_ERR: MBSFIR(1) : disp rrq23 counter overflow error
61:63	RWX	MBSCERR1Q_RESERVED_61_63: rsvd

Register Name	***MBC Purge Command Register***
Mnemonic	MBU.MBS.MBCPRGQ
Address	0000000002011414 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBCPRGQ_PURGE_ENTIRE_CACHE: When bit is set, the purge engine will go through every member in the cache, cast-out the entry to DRAM if it is Dirty, and write the directory to Invalid if it was not a deleted entry, else leave the entry in the Id state. When the purge is completed, the purge_cmd_done (bit 4 of this register) will be set. NOTE: the purge_cache_start_address and purge_cache_end_address fields are ignored when purging the entire cache.
1	RW	MBCPRGQ_PURGE_CACHE_RANGE: Setting this bit will cause the purge engine to behave exactly like the purge_entire_cache command, with the exception that the purge will begin at the purge_cache_start_address and end at the purge_cache_end_address fields in this register.
2	RW	MBCPRGQ_PURGE_SINGLE_MEMBER_AND_INVALIDATE: Setting this bit will cause the purge engine to purge a specific cache entry (castout the data to DRAM if directory indicates it is Dirty), write the LRU to be MRU, and write the directory state to invalid (I). The address used for this operation needs to be written to the purge_cache_start_(member,cgc) and purge_cache_end_(member, cgc) fields of this register. NOTE: If the line was previously in the deleted state, the purge engine will maintain the deleted state after the purge.
3	RW	MBCPRGQ_PURGE_SINGLE_MEMBER_AND_DELETE: Setting this bit will cause the purge engine to purge a specific cache entry (castout the data to DRAM if directory indicates it is Dirty), write the LRU to be MRU, and write the directory state to deleted state (Id). The address for used for this operation needs to be written to the purge_cache_start_(member,cgc) and purge_cache_end_(member, cgc) fields of this register.
4:7	RW	MBCPRGQ_PURGE_CACHE_START_MEMBER: Start cache address associated with purging a range in the cache - select one of sixteen members, corresponding to address(16:19).
8:20	RW	MBCPRGQ_PURGE_CACHE_START_CGC: Start cache address associated with purging a range in the cache - select one of 8192 sets (cgcs), corresponding to address(20:32).

Bits	SCOM	Field Mnemonic: Description
21:24	RW	MBCPRGQ_PURGE_CACHE_END_MEMBER: End cache address associated with purging a range in the cache - select one of sixteen members, corresponding to address(16:19). NOTE1: Set this value must be written to the same value in the purge_cache_start_member field of this register when purging a single member. NOTE2:When purging a range, only the members from purge_cache_start_member to purge_cache_end_member will be purged in each of the cgc's in that range. If you want to purge all members, set start member to zero and end member to 0xF.
25:37	RW	MBCPRGQ_PURGE_CACHE_END_CGC: End cache address associated with purging a range in the cache - select one of 8192 sets (cgcs), corresponding to address(20:32). NOTE: Set this value must be written to the same value in the purge_cache_start_cgc field of this register when purging a single member.
38:63	RO	constant=0b00000000000000000000000000

Register Name	***MBC Purge Status Register***
Mnemonic	MBU.MBS.MBCPRGSQ
Address	0000000002011415 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	MBCPRGSQ_MAX_DELETED_MEMBERS: Maximum number of members deleted in any particular congruence class in the cache.
4	ROX	MBCPRGSQ_PURGE_ENGINE_IS_BUSY: Purge Engine is Busy working on a previous command indicated by the Purge, Delete & and inject Command register.
5	ROX	MBCPRGSQ_PURGE_CMD_ERROR: Purge engine was busy when it saw a new purge command OR purge command is invalid due to multiple command bits(0:3) being set.
6:22	RWX	MBCPRGSQ_PURGE_CACHE_ADDRESS_16_32: Address of last line purged. 6:9 select one of sixteen members. 10:22 select a congruence class.
23	RWX	MBCPRGSQ_RSVD: reserved
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***MBC ECC Error Log Register***
Mnemonic	MBU.MBS.MBCELOGQ
Address	0000000002011416 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBCELOGQ_VALID_ECC_ERR: There was an MBC cache error detected. The error log information is written into this register based on the first error observed. The error log information will be held in this scom register until this bit is cleared. Note that there is the capability mask CE, UE, or SUEs from updating this register.
1	RWX	MBCELOGQ_CE: The valid error stored in this register is associated with a cache CE error. This bit should be cleared when the Valid_error bit is cleared.
2	RWX	MBCELOGQ_UE: The valid error stored in this register is associated with a cache UE error. This bit should be cleared when the Valid_error bit is cleared.
3	RWX	MBCELOGQ_SUE: The valid error stored in this register is associated with a cache SUE error. This bit should be cleared when the Valid_error bit is cleared.

Bits	SCOM	Field Mnemonic: Description
4	ROX	MBCELOGQ_MBCD_READ_PORT: Indicates which read port the error was associated with. A value of 0b0 indicates read port 0, which is used for castouts. A value of 0b1 indicates a read for read port 1.
5:12	ROX	MBCELOGQ_ECC_SYNDROME: the ECC syndrome(0:7) associated with the valid error.
13:15	ROX	MBCELOGQ_RSVD: reserved
16	ROX	MBCELOGQ_EDRAM_BNK_3: eDRAM bank address(3), corresponding to cgc member(0). Note that this corresponds to the member whose directory tag(0:19) matched the memory buffer address(0:19) and indicated a cache hit.
17:19	ROX	MBCELOGQ_EDRAM_CA_0_2: eDRAM column address(0:2), corresponding to cgc member(1:3). Note that this corresponds to the member whose directory tag(0:19) matched the memory buffer address(0:19) and indicated a cache hit.
20:27	ROX	MBCELOGQ_EDRAM_RA_2_9: eDRAM row address(2:9), which corresponds to memory buffer address(20:27)
28:29	ROX	MBCELOGQ_EDRAM_RA_0_1: eDRAM row address(0:1), which corresponds to memory buffer address(28:29)
30:32	ROX	MBCELOGQ_EDRAM_BNK_0_2: eDRAM bank address(0:2), which corresponds to memory buffer address(31:32)
33:36	ROX	MBCELOGQ_EDRAM_DW: eDRAM 8Byte address within the 128B cache line. See register description for an example of determining which eDRAM macro caused the error.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	***MBS Status Register***
Mnemonic	MBU.MBS.MBSSQ
Address	0000000002011417 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBSSQ_ALL_QUEUES_EMPTY: When this bit is set, all MBS state machines are idle, including srw, pf, cln, and co.
1	ROX	MBSSQ_ECCBP_EXIT1_SELECTED: Indicates the hardware is currently selecting exit1 as the path for dram 64B ecc bypass.
2	RWX	MBSSQ_IML_COMPLETE: Indicates the IML process is complete for the memory buffer chip.
3:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBSPMU0CFG***
Mnemonic	MBU.MBS.MBSPMU0CFGQ
Address	0000000002011418 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSPMU0CFGQ_PMU0_COUNTER0_ENABLE: Enable counter0
1	RW	MBSPMU0CFGQ_PMU0_COUNTER1_ENABLE: Enable counter1
2	RW	MBSPMU0CFGQ_PMU0_COUNTER2_ENABLE: Enable counter0
3	RW	MBSPMU0CFGQ_PMU0_COUNTER3_ENABLE: Enable counter1

Bits	SCOM	Field Mnemonic: Description
4:6	RW	MBSPMU0CFGQ_PMU0_PRESCALER_SEL: Determines prescaler counter to 16bit pmu counter. Values are defined below: 0 = 16b_prescaler 1 = 8b_prescaler 2 = 20b_prescaler 7 = no_prescaler
7	RW	MBSPMU0CFGQ_PMU0_COUNTER_FREEZE_MODE: If this bit is zero, the PMU counters will roll-over once they reach a maximum count. If this bit is set, all PMU counters will freeze when any one of the counters reaches a max count and is about to overflow. Values: ROLL_OVER_ON_MAX_COUNT=>0b0 FREEZE_ON_MAX_COUNT=>0b1
8	RW	MBSPMU0CFGQ_PMU0_COUNTER_RESET_MODE: Indicates how counter should reset. If this bit is set, the counters will reset whenever a read is done to the PMU count register (MBSPMU0CNT). When this bit is clear, the counters are free running if freeze mode is not enabled. Values: DO_NOT_RESET_ON_SCOM_READ=>0b0 RESET_ON_SCOM_READ=>0b1
9:12	RW	MBSPMU0CFGQ_PMU0_COUNTER0_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter0. Encodes 4-15 are unused 0 = event0_event1 1 = event2_event3 2 = event4_event5 3 = event6_event7
13	RW	MBSPMU0CFGQ_PMU0_COUNTER0_POSEDGE_SEL: If set, pmu will only count the event rising edge.
14:15	RW	MBSPMU0CFGQ_PMU0_COUNTER0_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this pmu counter. 0 = only_bit0 1 = only_bit1 2 = bit0_and_bit1 3 = bit0_plus_bit1
16:19	RW	MBSPMU0CFGQ_PMU0_COUNTER1_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter1. Encodes 4-15 are unused. 0 = event0_event1 1 = event2_event3 2 = event4_event5 3 = event6_event7
20	RW	MBSPMU0CFGQ_PMU0_COUNTER1_POSEDGE_SEL: If set, pmu will only count the event rising edge.
21:22	RW	MBSPMU0CFGQ_PMU0_COUNTER1_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this pmu counter. 0 = only_bit0 1 = only_bit1 2 = bit0_and_bit1 3 = bit0_plus_bit1
23:26	RW	MBSPMU0CFGQ_PMU0_COUNTER2_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter2. Encodes 4-15 are unused. 0 = event0_event1 1 = event2_event3 2 = event4_event5 3 = event6_event7
27	RW	MBSPMU0CFGQ_PMU0_COUNTER2_POSEDGE_SEL: If set, pmu will only count the event rising edge.
28:29	RW	MBSPMU0CFGQ_PMU0_COUNTER2_BIT_PAIR_SEL: Indicates how the event pairs should be combined to increment this pmu counter. 0 = only_bit0 1 = only_bit1 2 = bit0_and_bit1 3 = bit0_plus_bit1
30:33	RW	MBSPMU0CFGQ_PMU0_COUNTER3_EVENT_SEL: Indication of which of the 4 event pairs (8 total events) to count in counter3. Encodes 4-15 are unused. 0 = event0_event1 1 = event2_event3 2 = event4_event5 3 = event6_event7
34	RW	MBSPMU0CFGQ_PMU0_COUNTER3_POSEDGE_SEL: If set, pmu will only count the event rising edge.
35:36	RW	MBSPMU0CFGQ_PMU0_COUNTER3_BIT_PAIR_SEL: Indicates how the event bit pairs should be combined to increment this pmu counter. 0 = only_bit0 1 = only_bit1 2 = bit0_and_bit1 3 = bit0_plus_bit1
37:63	RO	constant=0b00000000000000000000000000

Register Name	***MBSPMU0CNT***
Mnemonic	MBU.MBS.MBSPMU0CNTQ
Address	0000000002011419 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	MBSPMU0CNTQ_PMU0_CNT0: PMU counter0(0:15)
16:31	ROX	MBSPMU0CNTQ_PMU0_CNT1: PMU counter1(0:15)

Bits	SCOM	Field Mnemonic: Description
32:47	ROX	MBSPMU0CNTQ_PMU0_CNT2: PMU counter2(0:15)
48:63	ROX	MBSPMU0CNTQ_PMU0_CNT3: PMU counter3(0:15)

Register Name	***MBUPMUSEL***
Mnemonic	MBU.MBS.MBSPMUSELQ
Address	000000000201141A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBSPMUSELQ_PMU_EVENT0_IN_SEL: Selects hardware event to drive event0
6:11	RW	MBSPMUSELQ_PMU_EVENT1_IN_SEL: Selects hardware event to drive event1
12:17	RW	MBSPMUSELQ_PMU_EVENT2_IN_SEL: Selects hardware event to drive event2
18:23	RW	MBSPMUSELQ_PMU_EVENT3_IN_SEL: Selects hardware event to drive event3
24:29	RW	MBSPMUSELQ_PMU_EVENT4_IN_SEL: Selects hardware event to drive event4
30:35	RW	MBSPMUSELQ_PMU_EVENT5_SIN_EL: Selects hardware event to drive event5
36:41	RW	MBSPMUSELQ_PMU_EVENT6_IN_SEL: Selects hardware event to drive event6
42:47	RW	MBSPMUSELQ_PMU_EVENT7_IN_SEL: Selects hardware event to drive event7
48	RW	MBSPMUSELQ_PMU_RANK_FILTER_EN: Enables filtering PMU events in the MBA bandwidth group by which master rank the commands translate to.
49:51	RW	MBSPMUSELQ_PMU_RANK_FILTER: If pmu_mrank_filter_en is set, this 3bit field selects which Master Rank translation will be used to filter PMU events in the MBA bw group.
52:55	RW	MBSPMUSELQ_PMU_SPARE: Spare PMU select modes
56:63	RO	constant=0b00000000

Register Name	***MBSIBERR0***
Mnemonic	MBU.MBS.MBSIBERR0Q
Address	000000000201141B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	MBSIBERR0Q_IB_HOST_ADDRESS: This is the 32 bit scom address that was being accessed when the error was detected.
32	RWX	MBSIBERR0Q_IB_HOST_ERROR_VALID: Indicates there was an PIB error on an Inband read or write scom access generated by the host. This register will lock on the first error and set the valid bit. PRD can clear the valid bit to allow new errors to be captured.
33:35	RWX	MBSIBERR0Q_IB_HOST_ERROR_STATUS: This is the PIB operation status field. If this field is 000, but the valid bit is on, an inband buffer CEUE occurred instead of a PIB error.
36	RWX	MBSIBERR0Q_IB_HOST_WRITE_NOT_READ: Indicates Inband error was for a write scom access, else a read scom access.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	***MBSIBERR1***
Mnemonic	MBU.MBS.MBSIBERR1Q
Address	000000000201141C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	MBSIBERR1Q_OCC_IB_ADDRESS: This is the 32 bit scom address that was being accessed when the error was detected.
32	RWX	MBSIBERR1Q_OCC_IB_ERROR_VALID: Indicates there was an PIB error on an Inband read or write scom access generated by the OCC. This register will lock on the first error and set the valid bit. PRD can clear the valid bit to allow new errors to be captured.
33:35	RWX	MBSIBERR1Q_OCC_IB_ERROR_STATUS: This is the PIB operation status field. If this field is 000, but the valid bit is on, an inband buffer CEUE occurred instead of a PIB error.
36	RWX	MBSIBERR1Q_OCC_IB_WRITE_NOT_READ: Indicates Inband error was for a write scom access, else a read scom access.
37:63	RO	constant=0b00000000000000000000000000

Register Name	***MBSIBWRSTAT***
Mnemonic	MBU.MBS.MBSIBWRSTATQ
Address	000000000201141D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBSIBWRSTATQ_SPARE0: Reserved
8:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Secure Fault Isolation Register (MCSSFIR)***
Mnemonic	MBU.MBS.ARB.RXLT.MBSSIRQ
Address	000000000201141E (SCOM) 000000000201141F (SCOM1) 0000000002011420 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBSSIRQ_INVALID_MBSXCR_ACCESS: If set, a non-inband write access to MBSXCR was detected with protection_en active
1	RWX	WOX_AND	WOX_OR	MBSSIRQ_INVALID_MBAXCR01_ACCESS: If set, a non-inband write access to MBAXCR01 was detected with protection_en active
2	RWX	WOX_AND	WOX_OR	MBSSIRQ_INVALID_MBAXCR23_ACCESS: If set, a non-inband write access to MBAXCR23 was detected with protection_en active
3	RWX	WOX_AND	WOX_OR	MBSSIRQ_INVALID_MBAXCRMS_ACCRESS: If set, a non-inband write access to MBAXCRMS1 was detected with protection_en active
4	RWX	WOX_AND	WOX_OR	MBSSIRQ_SPARE: Spare

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	MBSSIRQ_INVALID_SIR_MASK_OR_ACTION_REGISTER_ACCESS: If set, a non-inband write access to the MBSSIR mask or action registers was detected with protection_en active
6:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBS Secure Fault Isolation Mask Register (MBSSIRMASK)***
Mnemonic	MBU.MBS.ARB.RXLT.MBSSIRMASK
Address	0000000002011421 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RO	MBSSIRMASK_INVALID_MBSXCR_ACCESS: Masks SIR(0)
1	RO	MBSSIRMASK_INVALID_MBAXCR01_ACCESS: Masks SIR(1)
2	RO	MBSSIRMASK_INVALID_MBAXCR23_ACCESS: Masks SIR(2)
3	RO	MBSSIRMASK_INVALID_MBAXCRMS_ACCRESS: Masks SIR(3)
4	RO	MBSSIRMASK_SPARE: Masks SIR(4)
5	RO	MBSSIRMASK_INVALID_SIR_MASK_OR_ACTION_REGISTER_ACCESS: Masks SIR(5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBS Secure Fault Isolation Action0 Register (MBSSIRACT0)***
Mnemonic	MBU.MBS.ARB.RXLT.MBSSIRACT0
Address	0000000002011424 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBSSIRACT0_ACTION_0: Action 0 for SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBS Secure Fault Isolation Action0 Register (MBSSIRACT1)***
Mnemonic	MBU.MBS.ARB.RXLT.MBSSIRACT1
Address	0000000002011425 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBSSIRACT1_ACTION_1: Action 1 for SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBS OCC Threshold Count Register*
Mnemonic	MBU.MBS.MBSOCCITCQ
Address	0000000002011428 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	MBSOCCITCQ_OCC_CENT_IDLE_TH_CNT: OCC counter that counts Idle intervals that exceed a programmable threshold that ranges from 100uS to 100ms. This is a free running counter.
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	*MBS OCC Cache Hit 01 Count Register*
Mnemonic	MBU.MBS.MBSOCC01HQ
Address	0000000002011429 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBSOCC01HQ_OCC_01_RD_HIT: OCC counter that counts Downstream read commands that hit the cache and that translate to MBA01. This is a free running counter.
32:63	ROX	MBSOCC01HQ_OCC_01_WR_HIT: OCC counter that counts Downstream read commands that hit the cache and that translate to MBA01. This is a free running counter.

Register Name	*MBS OCC Cache Hit 23 Count Register*
Mnemonic	MBU.MBS.MBSOCC23HQ
Address	000000000201142A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBSOCC23HQ_OCC_23_RD_HIT: OCC counter that counts Downstream read commands that hit the cache and that translate to MBA23. This is a free running counter.
32:63	ROX	MBSOCC23HQ_OCC_23_WR_HIT: OCC counter that counts Downstream read commands that hit the cache and that translate to MBA23. This is a free running counter.

Register Name	*MBS OCC Speculative Cancel Count Register*
Mnemonic	MBU.MBS.MBSOCCSCANQ
Address	000000000201142B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBSOCCSCANQ_OCC_01_SPEC_CAN: OCC counter that counts speculative Downstream commands that are canceled and that translate to MBA01. This is a free running counter.
32:63	ROX	MBSOCCSCANQ_OCC_23_SPEC_CAN: OCC counter that counts speculative Downstream commands that are canceled and that translate to MBA23. This is a free running counter.

Register Name	***MBS Error Report Hold Register2***
Mnemonic	MBU.MBS.MBSCERR2Q
Address	000000000201142C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBSCERR2Q_PFFSM_TIMEOUT: MBSFIR(4) : pffsm timeout
1	RWX	MBSCERR2Q_PRQ_PROTOCOL_ERR: MBSFIR(1) : prq protocol error
2	RWX	MBSCERR2Q_PFFSM_PROTOCOL_ERR: MBSFIR(1) : pffsm protocol error
3	RWX	MBSCERR2Q_PFARB_PROTOCOL_ERR: MBSFIR(1) : pfarb protocol error
4	RWX	MBSCERR2Q_SRWFSM_UNEXPECTED_DS_CRESP: MBSFIR(0) : unexpected ds cresp in srwfsm
5	RWX	MBSCERR2Q_SRWFSM_UNEXPECTED_DS_CMD: MBSFIR(0) : unexpected ds cmd in srwfsm
6	RWX	MBSCERR2Q_SRWFSM_EXT_TIMOUT: MBSFIR(3) : srwfsm_ext_timeout_err
7	RWX	MBSCERR2Q_SRWFSM_INT_TIMEOUT: MBSFIR(4) : srwfsm_int_timeout_err
8	RWX	MBSCERR2Q_SRWFSM_PURGE_LINE_DEL: MBSFIR(17) : srwfsm purge and line_del entry
9	RWX	MBSCERR2Q_SRWFSM_PURGE_CLEAN_UE: MBSFIR(10) : srwfsm purge clean_ue entry
10	RWX	MBSCERR2Q_SRWFSM_PURGE_DIRTY_UE: MBSFIR(10) : srwfsm purge dirty_ue entry
11	RWX	MBSCERR2Q_SWDONE_WDONE_P_ERR: MBSFIR(8) : mbx_mbs wdone parity error
12	RWX	MBSCERR2Q_SWPAB_DS_TSIZE_ERR_HOLD: MBSFIR(0) : srw partial write tsize error
13	RWX	MBSCERR2Q_SWB_DS_WDATA_ERR0_HOLD: MBSFIR(0) : swb overflow
14	RWX	MBSCERR2Q_SWB_DS_WDATA_ERR1_HOLD: MBSFIR(0) : swb overflow
15	RWX	MBSCERR2Q_MBX_MBS_RDTAG_PERR: MBSFIR(8) : mbx rdtag perr
16	RWX	MBSCERR2Q_RDTAG_FIFO_PERR: MBSFIR(8) : mbs_mbx_rdtag delay fifo parity error
17	RWX	MBSCERR2Q_DS_FRAME_SEG_ERR: MBSFIR(0) : Downstream frame segment protocol error
18	RWX	MBSCERR2Q_DS_INVALID_DATA_SUE_ERR: MBSFIR(0) : Downstream sue bit is set but data valid is not set in a frame
19	RWX	MBSCERR2Q_US_READ_DATA_PERR: MBSFIR(8) : Upstream read data parity error
20	RWX	MBSCERR2Q_US_READ_DATA_INFO_PERR: MBSFIR(8) : Upstream read data info parity error
21	RWX	MBSCERR2Q_IBB_CE: MBSFIR(05) : inband buffer CE
22	RWX	MBSCERR2Q_IBB_UE: MBSFIR(06) : inband buffer UE
23	RWX	MBSCERR2Q_IBB_SUE: MBSFIR(07) : inband buffer SUE
24	RWX	MBSCERR2Q_IBB_DS_CE: MBSFIR(05) : Downdstream to inband buffer CE
25	RWX	MBSCERR2Q_IBB_DS_PROTOCOL_ERR: MBSFIR(0) : ds to ibb protocol error
26	RWX	MBSCERR2Q_CLNFSM_SCOMFIR_CERR_HOLD: MBSFIR(10) : srwfsm purge dirty_ue entry
27	RWX	MBSCERR2Q_SPARE: rsvd
28	RWX	MBSCERR2Q_RXLT_SIR_PERR: MBSFIR(8) : sir parity error

Bits	SCOM	Field Mnemonic: Description
29	RWX	MBSCERR2Q_CACTL_ADDRESS_ERR: MBSFIR(2) : address error
30	RWX	MBSCERR2Q_EMER_THROTTLE_CERR: MBSFIR(21) : emergency throttle
31	RWX	MBSCERR2Q_MAX_LINE_DEL_ERR: MBSFIR(18) : max line del
32	RWX	MBSCERR2Q_MBCD0_DW02_13BNK_DRAM_ERR: MBSFIR(20) : eDRAM error
33	RWX	MBSCERR2Q_MBCD0_DW46_57BNK_ERR: MBSFIR(20) : eDRAM error
34	RWX	MBSCERR2Q_MBCD0_DW8A_9BBNK_ERR: MBSFIR(20) : eDRAM error
35	RWX	MBSCERR2Q_MBCD0_DWCE_DFBNK_ERR: MBSFIR(20) : eDRAM error
36	RWX	MBSCERR2Q_MBCD1_DW02_13BNK_ERR: MBSFIR(20) : eDRAM error
37	RWX	MBSCERR2Q_MBCD1_DW46_57BNK_ERR: MBSFIR(20) : eDRAM error
38	RWX	MBSCERR2Q_MBCD1_DW8A_9BBNK_ERR: MBSFIR(20) : eDRAM error
39	RWX	MBSCERR2Q_MBCD1_DWCE_DFBNK_ERR: MBSFIR(20) : eDRAM error
40	RWX	MBSCERR2Q_RXLAT_PERR: MBSFIR(8) : rxlt parity error
41	RWX	MBSCERR2Q_CLNADD_PERR: MBSFIR(8) : cln address parity error
42	RWX	MBSCERR2Q_COADDR_PERR: MBSFIR(8) : co address parity error
43	RWX	MBSCERR2Q_PFADDR_PERR: MBSFIR(8) : pf address parity error
44	RWX	MBSCERR2Q_PRQADDR_PERR: MBSFIR(8) : prq address parity error
45:63	ROX	MBSCERR2Q_RESERVED_45_63: rsvd

Register Name	***Memory Buffer Emergency Throttle Register***
Mnemonic	MBU.MBS.MBSEMERTHROQ
Address	000000000201142D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSEMERTHROQ_EMERGENCY_THROTTLE_IN_PROGRESS: If 1 the memory buffer MBA will throttle commands to the memory DIMMs continuously until this bit is reset by software. This bit can be set from the OCC.
1:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	***MBS ECC Decoder FIR Register***
Mnemonic	MBU.MBS.ECC01.MBECCFIR
Address	0000000002011440 (SCOM) 0000000002011441 (SCOM1) 0000000002011442 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_MPE_RANK_0_7: This bit is set when a memory Mark Place Error is detected on rank 0:7 on a non-maintenance read op. While set, SCOM write operations to MBMSRX are blocked, and bypass mode for the rank is disabled

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8:15	RWX	WOX_AND	WOX_OR	MBECCFIR_RESERVED_8_15: Reserved
16	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_NCE: This bit is set when a memory new CE is detected on a non-maintenance read op.
17	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_RCE: This bit is set when a memory retry CE is detected on a non-maintenance read op.
18	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_SUE: This bit is set when a memory SUE is detected on a non-maintenance read op. SUE is always determined from the corrected data, irrespective of MBSECCQ(1).
19	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_UE: This bit is set when a memory UE is detected on a non-maintenance read op.
20:27	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINT_MPE_RANK_0_7: This bit is set when a memory Mark Place Err is detected on rank 0:7, on a maintenance read op. While set, SCOM write operations to MBMSRX are blocked, and bypass mode for the rank is disabled
28:35	RWX	WOX_AND	WOX_OR	MBECCFIR_RESERVED_28_35: Reserved
36	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_NCE: This bit is set when a memory new CE is detected on a maintenance read op.
37	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_SCE: This bit is set when a memory symbol CE is detected on a maintenance read op.
38	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_MCE: This bit is set when a memory mark CE is detected on a maintenance read op.
39	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_RCE: This bit is set when a memory retry CE is detected on a maintenance read op.
40	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_SUE: This bit is set when a memory SUE is detected on a maintenance read op. SUE is always determined from the corrected data, irrespective of MBSECCQ(1). Maintenance SUE is not set during MCBIST
41	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_UE: This bit is set when a memory UE is detected on a maintenance read op.
42	RWX	WOX_AND	WOX_OR	MBECCFIR_MPE_DURING_USE_MAINTENANCE_MARK_MODE: This bit is set when a memory Mark Place Error is detected on a maintenance read op, while maintenance mark mode is set.
43	RWX	WOX_AND	WOX_OR	MBECCFIR_PREFETCH_MEMORY_UE: This bit is set when a memory UE from a prefect read is detected.
44	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_RCD_PARITY_ERROR_: This bit is set when a RCD parity error occurred on a shadow retry read.
45	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_RCD_PARITY_ERROR_: This bit is set when a RCD parity error occurred on a maintenance retry read (Set on first read for SFRead and MCBIST which do not retry).
46	RWX	WOX_AND	WOX_OR	MBECCFIR_RECOVERABLE_CONFIGURATION_REGISTER_PARITY_ERROR: This bit is set when a parity error is detected in a mark store register (MBMS[n] or MBMMR) or bit steer control register (MBSBS[n]).
47	RWX	WOX_AND	WOX_OR	MBECCFIR_UNRECOVERABLE_CONFIGURATION_REGISTER_PARITY_ERROR: This bit is set when a parity error is detected in the MBSECC control register.
48	RWX	WOX_AND	WOX_OR	MBECCFIR_MASKABLE_CONFIGURATION_REGISTER_PARITY_ERROR: This bit is set when a parity error is detected in the mark shadow register (MBSMSR) or RCE error inject control register (MBRCEICR)
49	RWX	WOX_AND	WOX_OR	MBECCFIR_ECC_DATAPATH_PARITY_ERROR: This bit is set when a parity error is detected in the ecc datapath
50	RWX	WOX_AND	WOX_OR	MBECCFIR_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
51	RWX	WOX_AND	WOX_OR	MBECCFIR_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
52:63	RO	N/A	N/A	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR Mask Register (MBECCFIR_MASK)***
Mnemonic	MBU.MBS.ECC01.MBECCFIR_MASK
Address	0000000002011443 (SCOM) 0000000002011444 (SCOM1) 0000000002011445 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:51	RW	WO_AND	WO_OR	MBECCFIR_MASK_FIR_MASK: MASK for MBSECCFIR bits 0:51
52:63	RO	N/A	N/A	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR Action 0 Register (MBECCFIR_ACTION0)***
Mnemonic	MBU.MBS.ECC01.MBECCFIR_ACTION0
Address	0000000002011446 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:51	RO	MBECCFIR_ACTION0_FIR_ACTION0: MBSECCFIR action0 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
52:63	RO	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR Action 1 Register (MBECCFIR_ACTION1)***
Mnemonic	MBU.MBS.ECC01.MBECCFIR_ACTION1
Address	0000000002011447 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:51	RO	MBECCFIR_ACTION1_FIR_ACTION1: MBSECCFIR action1 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
52:63	RO	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR WOF Register***
Mnemonic	MBU.MBS.ECC01.MBECCFIR_WOF
Address	0000000002011448 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:51	RWX_WCLRREG	MBECCFIR_WOF_FIR_WOF: WOF Register locks on first error..RWX_W..CLRREG
52:63	RO	constant=0b000000000000

Register Name	***MBS Memory ECC Control Register***
Mnemonic	MBU.MBS.ECC01.MBSECCQ
Address	000000002201144A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSECCQ_DISABLE_MEMORY_ECC_CHECK_CORRECT: When set, memory ECC check and correct is disabled. When memory ECC checking is disabled, the SUE injecting into the 8B data bus ECC is also disabled.
1	RW	MBSECCQ_DISABLE_MEMORY_ECC_CORRECT: When set, memory ECC correct is disabled (memory ECC checking is not disabled)
2	RW	MBSECCQ_RESERVED_2: Reserved
3	RW	MBSECCQ_ENABLE_64BYTE_DATA_CHECKBIT_INVERSION: When set, even (address) 64-byte data pieces are inverted, and odd (address) 64-bytes ecc checkbits and the 65th byte are inverted, between memory and the ecc check logic, and between the ecc gen logic and memory.
4	RW	MBSECCQ_USE_MAINTENANCE_MARK: When set, maintenance read operations use the mark value in MBMMR. If a MPE is detected during a maintenance read operation and this bit is set, the mark update is written only to MBMMR. This bit must not be set for MCBIST operations.
5	RW	MBSECCQ_DISABLE_MARK_STORE_WRITE: When set, the MBMSx registers are never written by the ECC decoder hardware.
6	RW	MBSECCQ_ENABLE_FIRST_SHADOW_READ_UE: When set, the ECC checkers will ignore the state of the retry read valid and set the Memory_UE FIR bit upon first detection of a shadow read memory_ue.
7:9	RW	MBSECCQ_ECC_METADATA_MODE: Number of metadata bits in 65th byte. Values: 0_METADATA_8_CHECKBITS=>0b000 1_METADATA_7_CHECKBITS=>0b100 2_METADATA_6_CHECKBITS=>0b010 6_METADATA_2_CHECKBITS___DEFAULT_FOR_VENICE__CENTAUR__=>0b011
10	RW	MBSECCQ_SINGLE_WIRE_MODE: When set and a chipkill is marked then any new error corrected can be single wire only. (default is '1' for POWER8 processor and memory buffer)
11	RW	MBSECCQ_INT_RESET_KEEPER: When set the reset pulse will be applied to MBSECC c_err_rpt hold latches.
12	NC	MBSECCQ_INJECT_SCOM_PARITY_ERROR: When set, scom writes to any ecc scom register (except the MBSECCFIR* registers) will set incorrect parity, causing the corresponding parity error.
13	NC	MBSECCQ_INJECT_MARK_STORE_SYMBOL_PARITY_ERROR: When set, scom writes to the mark store registers MBMS0-8 will set incorrect parity for the symbol mark, causing the corresponding parity error.

Bits	SCOM	Field Mnemonic: Description
14	NC	MBSECCQ_INJECT_MARK_STORE_CHIP_PARITY_ERROR: When set, scom writes to the mark store registers MBMS0-8 will set incorrect parity for the chip mark, causing the corresponding parity error.
15:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 0***
Mnemonic	MBU.MBS.ECC01.MBMS0
Address	000000000201144B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS0_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS0_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 1***
Mnemonic	MBU.MBS.ECC01.MBMS1
Address	000000000201144C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS1_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS1_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 2***
Mnemonic	MBU.MBS.ECC01.MBMS2
Address	000000000201144D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS2_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS2_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 3***
Mnemonic	MBU.MBS.ECC01.MBMS3
Address	000000000201144E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS3_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS3_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 4***
Mnemonic	MBU.MBS.ECC01.MBMS4
Address	000000000201144F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS4_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS4_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 5***
Mnemonic	MBU.MBS.ECC01.MBMS5
Address	0000000002011450 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS5_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS5_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 6***
Mnemonic	MBU.MBS.ECC01.MBMS6
Address	0000000002011451 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS6_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)

Bits	SCOM	Field Mnemonic: Description
8:15	RWX	MBMS6_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 7***
Mnemonic	MBU.MBS.ECC01.MBMS7
Address	0000000002011452 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS7_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS7_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	***MBS Maintenance Mark Register***
Mnemonic	MBU.MBS.ECC01.MBMMRQ
Address	000000000201145B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMMRQ_SYMBOL_MAINTENANCE_MARK_VALUE: Symbol mark value for maintenance mark (FW written)
8:15	RWX	MBMMRQ_CHIP_MAINTENANCE_MARK_VALUE: Chip maintenance mark value - if a maintenance op detects a MPE while maintenance mark mode is set, the update mark will be written only to this register.
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	***MBS Mark Register Shadow***
Mnemonic	MBU.MBS.ECC01.MBSMSRQ
Address	000000000201145C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RO	MBSMSRQ_MARK_VALUE: Value of last mark generated by ECC decoder
16:18	RO	MBSMSRQ_MARK_SHADOW_RANK: Rank associated with last mark generated by the ECC decoder
19:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	***MBS RCE Error Inject Control Register***
Mnemonic	MBU.MBS.ECC01.MBRCEICRQ
Address	000000000201145D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MBRCEICRQ_ADDRESS: Address to inject RCE. Compared with read data address. 0:2 = mrank(0:2) 3:5 = srank(0:2) 6:9 = bank(0:3) 10:26 = row(0:16) 27:37 = col(1:11)
38	RWX	MBRCEICRQ_ENABLE_RCE_INJECT: When set, a UE error is forced when the read data address matches bits (0:37) of this register, subject to the masks selected in bits 55:62. After the UE error is forced, this bit is reset. The single UE error forced causes the memory ECC logic to retry the read - since the UE error is only forced once, the retried read data will be clean, causing a RCE error to be reported.
39	RW	MBRCEICRQ_ENABLE_SCRUB_INJECT: When set, an error is injected for scrub reads when the read data address matches bits (0:37) of this register, subject to the masks selected in bits 55:62. This enable bit does not automatically reset.
40:44	RW	MBRCEICRQ_READ1_ERROR_TYPE: Selects the error to be injected for scrub read 1 (read 1 may include a retry read after an UE) The error type is a 5 bit field consisting of the following bits: R C0 S0 C1 S1 R causes a retry by causing an UE (as if C0,S0,C1,S1 are all 1) C0 causes a chip error by injecting errors in symbols 69 and 68 S0 causes a symbol error in symbol 67 C1 causes a chip error by injecting errors in symbols 37 and 36 S1 causes a symbol error in symbol 35
45:49	RW	MBRCEICRQ_READ2_ERROR_TYPE: Selects the error to be injected for scrub read 2. same bit definitions as above.
50:54	RW	MBRCEICRQ_READ3_ERROR_TYPE: Selects the error to be injected for scrub read 3. same bit definitions as above.
55:56	RW	MBRCEICRQ_BANK_MASK_SELECT: selects masking of bank bits from address compare Values: COMPARE_BANK_BITS_0_TO_3=>0b00 COMPARE_BANK_BITS_1_TO_3=>0b01 COMPARE_BANK_BITS_2_TO_3=>0b10 COMPARE_BANK_BIT_3=>0b11
57:59	RW	MBRCEICRQ_ROW_MASK_SELECT: selects masking of row bits from address compare Values: COMPARE_ROW_BITS_0_TO_16=>0b000 COMPARE_ROW_BITS_1_TO_16=>0b001 COMPARE_ROW_BITS_2_TO_16=>0b010 COMPARE_ROW_BITS_3_TO_16=>0b011 COMPARE_ROW_BITS_4_TO_16=>0b100 COMPARE_ROW_BITS_5_TO_16=>0b101 COMPARE_ROW_BITS_6_TO_16=>0b110 COMPARE_ROW_BITS_7_TO_16=>0b111
60:62	RW	MBRCEICRQ_COLUMN_MASK_SELECT: selects masking of column bits from address compare Values: COMPARE_COLUMN_BITS_1_TO_11=>0b000 COMPARE_COLUMN_BITS_2_TO_11=>0b001 COMPARE_COLUMN_BITS_3_TO_11=>0b010 COMPARE_COLUMN_BITS_4_TO_11=>0b011 COMPARE_COLUMN_BITS_5_TO_11=>0b100 COMPARE_COLUMN_BITS_6_TO_11=>0b101 COMPARE_COLUMN_BITS_7_TO_11=>0b110 COMPARE_COLUMN_BITS_8_TO_11=>0b111
63	RW	MBRCEICRQ_DATAPATH_PARITY_ERROR_INJECT: When set, a datapath parity error (FIR 49) is injected for reads when the read data address matches bits (0:37) of this register, subject to the masks selected in bits 55:62. This enable bit does not automatically reset.

Register Name	*MBS Bit Steer Control Register 0*
Mnemonic	MBU.MBS.ECC01.MBSBS0
Address	000000000201145E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS0_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS0_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS0_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 1***
Mnemonic	MBU.MBS.ECC01.MBSBS1
Address	000000000201145F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS1_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS1_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS1_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 2***
Mnemonic	MBU.MBS.ECC01.MBSBS2
Address	0000000002011460 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS2_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS2_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS2_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 3***
Mnemonic	MBU.MBS.ECC01.MBSBS3
Address	0000000002011461 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS3_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS3_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS3_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 4***
Mnemonic	MBU.MBS.ECC01.MBSBS4
Address	0000000002011462 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS4_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS4_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS4_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 5***
Mnemonic	MBU.MBS.ECC01.MBSBS5
Address	0000000002011463 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS5_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS5_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS5_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 6***
Mnemonic	MBU.MBS.ECC01.MBSBS6
Address	0000000002011464 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS6_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS6_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS6_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 7***
Mnemonic	MBU.MBS.ECC01.MBSBS7
Address	0000000002011465 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS7_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS7_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS7_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS ECC Error Report Hold Register 0***
Mnemonic	MBU.MBS.ECC01.MBSECCERR0
Address	0000000002011466 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:32	RO	constant=0b00000000000000000000000000000000
33	ROX	MBSECCERR0_MBMS0_CHIP_PARITY: MBECCFIR(46) : mark_store0_chip_parity
34	ROX	MBSECCERR0_MBMS0_SYMBOL_PARITY: MBECCFIR(46) : mark_store0_symbol_parity
35	ROX	MBSECCERR0_MBMS0_PARITY: MBECCFIR(46) : mark_store0_parity
36	ROX	MBSECCERR0_MBMS1_CHIP_PARITY: MBECCFIR(46) : mark_store1_chip_parity
37	ROX	MBSECCERR0_MBMS1_SYMBOL_PARITY: MBECCFIR(46) : mark_store1_symbol_parity
38	ROX	MBSECCERR0_MBMS1_PARITY: MBECCFIR(46) : mark_store1_parity
39	ROX	MBSECCERR0_MBMS2_CHIP_PARITY: MBECCFIR(46) : mark_store2_chip_parity
40	ROX	MBSECCERR0_MBMS2_SYMBOL_PARITY: MBECCFIR(46) : mark_store2_symbol_parity

Bits	SCOM	Field Mnemonic: Description
41	ROX	MBSECCERR0_MBMS2_PARITY: MBECCFIR(46) : mark_store2_parity
42	ROX	MBSECCERR0_MBMS3_CHIP_PARITY: MBECCFIR(46) : mark_store3_chip_parity
43	ROX	MBSECCERR0_MBMS3_SYMBOL_PARITY: MBECCFIR(46) : mark_store3_symbol_parity
44	ROX	MBSECCERR0_MBMS3_PARITY: MBECCFIR(46) : mark_store3_parity
45	ROX	MBSECCERR0_MBMS4_CHIP_PARITY: MBECCFIR(46) : mark_store4_chip_parity
46	ROX	MBSECCERR0_MBMS4_SYMBOL_PARITY: MBECCFIR(46) : mark_store4_symbol_parity
47	ROX	MBSECCERR0_MBMS4_PARITY: MBECCFIR(46) : mark_store4_parity
48	ROX	MBSECCERR0_MBMS5_CHIP_PARITY: MBECCFIR(46) : mark_store5_chip_parity
49	ROX	MBSECCERR0_MBMS5_SYMBOL_PARITY: MBECCFIR(46) : mark_store5_symbol_parity
50	ROX	MBSECCERR0_MBMS5_PARITY: MBECCFIR(46) : mark_store5_parity
51	ROX	MBSECCERR0_MBMS6_CHIP_PARITY: MBECCFIR(46) : mark_store6_chip_parity
52	ROX	MBSECCERR0_MBMS6_SYMBOL_PARITY: MBECCFIR(46) : mark_store6_symbol_parity
53	ROX	MBSECCERR0_MBMS6_PARITY: MBECCFIR(46) : mark_store6_parity
54	ROX	MBSECCERR0_MBMS7_CHIP_PARITY: MBECCFIR(46) : mark_store7_chip_parity
55	ROX	MBSECCERR0_MBMS7_SYMBOL_PARITY: MBECCFIR(46) : mark_store7_symbol_parity
56	ROX	MBSECCERR0_MBMS7_PARITY: MBECCFIR(46) : mark_store7_parity
57:63	RO	constant=0b0000000

Register Name	***MBS ECC Error Report Hold Register 1***
Mnemonic	MBU.MBS.ECC01.MBSECCERR1
Address	0000000002011467 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	MBSECCERR1_MEMORY_BIT_STEER_PARITY: MBECCFIR(46) : bit_steer_register_parity
8	RO	constant=0b0
9	ROX	MBSECCERR1_MBMMR_PARITY: MBECCFIR(46) : mbmmr_register_parity
10	RO	constant=0b0
11	ROX	MBSECCERR1_MBRCEICR_PARITY: MBECCFIR(48) : mbrceicr_register_parity
12:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS ECC Decoder FIR Register***
Mnemonic	MBU.MBS.ECC23.MBECCFIR
Address	0000000002011480 (SCOM) 0000000002011481 (SCOM1) 0000000002011482 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:7	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_MPE_RANK_0_7: This bit is set when a memory Mark Place Error is detected on rank 0:7 on a non-maintenance read op. While set, SCOM write operations to MBMSRX are blocked, and bypass mode for the rank is disabled
8:15	RWX	WOX_AND	WOX_OR	MBECCFIR_RESERVED_8_15: Reserved
16	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_NCE: This bit is set when a memory new CE is detected on a non-maintenance read op.
17	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_RCE: This bit is set when a memory retry CE is detected on a non-maintenance read op.
18	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_SUE: This bit is set when a memory SUE is detected on a non-maintenance read op. SUE is always determined from the corrected data, irrespective of MBSECCQ(1).
19	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_UE: This bit is set when a memory UE is detected on a non-maintenance read op.
20:27	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINT_MPE_RANK_0_7: This bit is set when a memory Mark Place Err is detected on rank 0:7, on a maintenance read op. While set, SCOM write operations to MBMSRX are blocked, and bypass mode for the rank is disabled
28:35	RWX	WOX_AND	WOX_OR	MBECCFIR_RESERVED_28_35: Reserved
36	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_NCE: This bit is set when a memory new CE is detected on a maintenance read op.
37	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_SCE: This bit is set when a memory symbol CE is detected on a maintenance read op.
38	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_MCE: This bit is set when a memory mark CE is detected on a maintenance read op.
39	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_RCE: This bit is set when a memory retry CE is detected on a maintenance read op.
40	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_SUE: This bit is set when a memory SUE is detected on a maintenance read op. SUE is always determined from the corrected data, irrespective of MBSECCQ(1). Maintenance SUE is not set during MCBIST
41	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_UE: This bit is set when a memory UE is detected on a maintenance read op.
42	RWX	WOX_AND	WOX_OR	MBECCFIR_MPE_DURING_USE_MAINTENANCE_MARK_MODE: This bit is set when a memory Mark Place Error is detected on a maintenance read op, while maintenance mark mode is set.
43	RWX	WOX_AND	WOX_OR	MBECCFIR_PREFETCH_MEMORY_UE: This bit is set when a memory UE from a prefect read is detected.
44	RWX	WOX_AND	WOX_OR	MBECCFIR_MEMORY_RCD_PARITY_ERROR_: This bit is set when a RCD parity error occurred on a shadow retry read.
45	RWX	WOX_AND	WOX_OR	MBECCFIR_MAINTENANCE_RCD_PARITY_ERROR_: This bit is set when a RCD parity error occurred on a maintenance retry read (Set on first read for SFRead and MCBIST which do not retry).
46	RWX	WOX_AND	WOX_OR	MBECCFIR_RECOVERABLE_CONFIGURATION_REGISTER_PARITY_ERROR: This bit is set when a parity error is detected in a mark store register (MBMS[n] or MBMMR) or bit steer control register (MBSBS[n]).
47	RWX	WOX_AND	WOX_OR	MBECCFIR_UNRECOVERABLE_CONFIGURATION_REGISTER_PARITY_ERROR: This bit is set when a parity error is detected in the MBSECC control register.
48	RWX	WOX_AND	WOX_OR	MBECCFIR_MASKABLE_CONFIGURATION_REGISTER_PARITY_ERROR: This bit is set when a parity error is detected in the mark shadow register (MBSMSR) or RCE error inject control register (MBRCEICR)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
49	RWX	WOX_AND	WOX_OR	MBECCFIR_ECC_DATAPATH_PARITY_ERROR: This bit is set when a parity error is detected in the ecc datapath
50	RWX	WOX_AND	WOX_OR	MBECCFIR_INTERNAL_SCOM_ERROR: When set, an internal SCOM error has occurred
51	RWX	WOX_AND	WOX_OR	MBECCFIR_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
52:63	RO	N/A	N/A	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR Mask Register (MBECCFIR_MASK)***
Mnemonic	MBU.MBS.ECC23.MBECCFIR_MASK
Address	0000000002011483 (SCOM) 0000000002011484 (SCOM1) 0000000002011485 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:51	RW	WO_AND	WO_OR	MBECCFIR_MASK_FIR_MASK: MASK for MBSECCFIR bits 0:51
52:63	RO	N/A	N/A	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR Action 0 Register (MBECCFIR_ACTION0)***
Mnemonic	MBU.MBS.ECC23.MBECCFIR_ACTION0
Address	0000000002011486 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:51	RO	MBECCFIR_ACTION0_FIR_ACTION0: MBSECCFIR action0 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
52:63	RO	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR Action 1 Register (MBECCFIR_ACTION1)***
Mnemonic	MBU.MBS.ECC23.MBECCFIR_ACTION1
Address	0000000002011487 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:51	RO	MBECCFIR_ACTION1_FIR_ACTION1: MBSECCFIR action1 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
52:63	RO	constant=0b000000000000

Register Name	***MBS ECC Decoder FIR WOF Register***
Mnemonic	MBU.MBS.ECC23.MBECCFIR_WOF
Address	0000000002011488 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:51	RWX_WCLRREG	MBECCFIR_WOF_FIR_WOF: WOF Register locks on first error..RWX_W..CLRREG
52:63	RO	constant=0b000000000000

Register Name	***MBS Memory ECC Control Register***
Mnemonic	MBU.MBS.ECC23.MBSECCQ
Address	000000002201148A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSECCQ_DISABLE_MEMORY_ECC_CHECK_CORRECT: When set, memory ECC check and correct is disabled. When memory ECC checking is disabled, the SUE injecting into the 8B data bus ECC is also disabled.
1	RW	MBSECCQ_DISABLE_MEMORY_ECC_CORRECT: When set, memory ECC correct is disabled (memory ECC checking is not disabled)
2	RW	MBSECCQ_RESERVED_2: Reserved
3	RW	MBSECCQ_ENABLE_64BYTE_DATA_CHECKBIT_INVERSION: When set, even (address) 64-byte data pieces are inverted, and odd (address) 64-bytes ecc checkbits and the 65th byte are inverted, between memory and the ecc check logic, and between the ecc gen logic and memory.
4	RW	MBSECCQ_USE_MAINTENANCE_MARK: When set, maintenance read operations use the mark value in MBMMR. If a MPE is detected during a maintenance read operation and this bit is set, the mark update is written only to MBMMR. This bit must not be set for MCBIST operations.
5	RW	MBSECCQ_DISABLE_MARK_STORE_WRITE: When set, the MBMSx registers are never written by the ECC decoder hardware.
6	RW	MBSECCQ_ENABLE_FIRST_SHADOW_READ_UE: When set, the ECC checkers will ignore the state of the retry read valid and set the Memory_UE FIR bit upon first detection of a shadow read memory_ue.
7:9	RW	MBSECCQ_ECC_METADATA_MODE: Number of metadata bits in 65th byte. Values: 0_METADATA_8_CHECKBITS=>0b000 1_METADATA_7_CHECKBITS=>0b100 2_METADATA_6_CHECKBITS=>0b010 6_METADATA_2_CHECKBITS___DEFAULT_FOR_VENICE__CENTAUR__=>0b011
10	RW	MBSECCQ_SINGLE_WIRE_MODE: When set and a chipkill is marked then any new error corrected can be single wire only. (default is '1' for POWER8 processor and memory buffer)
11	RW	MBSECCQ_INT_RESET_KEEPER: When set the reset pulse will be applied to MBSECC c_err_rpt hold latches.
12	NC	MBSECCQ_INJECT_SCOM_PARITY_ERROR: When set, scom writes to any ecc scom register (except the MBSECCFIR* registers) will set incorrect parity, causing the corresponding parity error.
13	NC	MBSECCQ_INJECT_MARK_STORE_SYMBOL_PARITY_ERROR: When set, scom writes to the mark store registers MBMS0-8 will set incorrect parity for the symbol mark, causing the corresponding parity error.

Bits	SCOM	Field Mnemonic: Description
14	NC	MBSECCQ_INJECT_MARK_STORE_CHIP_PARITY_ERROR: When set, scom writes to the mark store registers MBMS0-8 will set incorrect parity for the chip mark, causing the corresponding parity error.
15:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 0***
Mnemonic	MBU.MBS.ECC23.MBMS0
Address	000000000201148B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS0_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS0_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 1***
Mnemonic	MBU.MBS.ECC23.MBMS1
Address	000000000201148C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS1_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS1_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS Memory ECC Mark StoreX Register 2***
Mnemonic	MBU.MBS.ECC23.MBMS2
Address	000000000201148D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS2_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS2_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*MBS Memory ECC Mark StoreX Register 3*
Mnemonic	MBU.MBS.ECC23.MBMS3
Address	000000000201148E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS3_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS3_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000

Register Name	*MBS Memory ECC Mark StoreX Register 4*
Mnemonic	MBU.MBS.ECC23.MBMS4
Address	000000000201148F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS4_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS4_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000

Register Name	*MBS Memory ECC Mark StoreX Register 5*
Mnemonic	MBU.MBS.ECC23.MBMS5
Address	0000000002011490 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS5_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS5_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000

Register Name	*MBS Memory ECC Mark StoreX Register 6*
Mnemonic	MBU.MBS.ECC23.MBMS6
Address	0000000002011491 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS6_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)

Bits	SCOM	Field Mnemonic: Description
8:15	RWX	MBMS6_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	*MBS Memory ECC Mark StoreX Register 7*
Mnemonic	MBU.MBS.ECC23.MBMS7
Address	0000000002011492 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMS7_SYMBOL_MARK_VALUE_FOR_RANKX: Symbol Mark value for rank X (FW written)
8:15	RWX	MBMS7_CHIP_MARK_VALUE_FOR_RANKX: Chip Mark value for rank X (HW written)
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	*MBS Maintenance Mark Register*
Mnemonic	MBU.MBS.ECC23.MBMMRQ
Address	000000000201149B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBMMRQ_SYMBOL_MAINTENANCE_MARK_VALUE: Symbol mark value for maintenance mark (FW written)
8:15	RWX	MBMMRQ_CHIP_MAINTENANCE_MARK_VALUE: Chip maintenance mark value - if a maintenance op detects a MPE while maintenance mark mode is set, the update mark will be written only to this register.
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	*MBS Mark Register Shadow*
Mnemonic	MBU.MBS.ECC23.MBSMSRQ
Address	000000000201149C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RO	MBSMSRQ_MARK_VALUE: Value of last mark generated by ECC decoder
16:18	RO	MBSMSRQ_MARK_SHADOW_RANK: Rank associated with last mark generated by the ECC decoder
19:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	***MBS RCE Error Inject Control Register***
Mnemonic	MBU.MBS.ECC23.MBRCEICRQ
Address	000000000201149D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MBRCEICRQ_ADDRESS: Address to inject RCE. Compared with read data address. 0:2 = mrank(0:2) 3:5 = srank(0:2) 6:9 = bank(0:3) 10:26 = row(0:16) 27:37 = col(1:11)
38	RWX	MBRCEICRQ_ENABLE_RCE_INJECT: When set, a UE error is forced when the read data address matches bits (0:37) of this register, subject to the masks selected in bits 55:62. After the UE error is forced, this bit is reset. The single UE error forced causes the memory ECC logic to retry the read - since the UE error is only forced once, the retried read data will be clean, causing a RCE error to be reported.
39	RW	MBRCEICRQ_ENABLE_SCRUB_INJECT: When set, an error is injected for scrub reads when the read data address matches bits (0:37) of this register, subject to the masks selected in bits 55:62. This enable bit does not automatically reset.
40:44	RW	MBRCEICRQ_READ1_ERROR_TYPE: Selects the error to be injected for scrub read 1 (read 1 may include a retry read after an UE) The error type is a 5 bit field consisting of the following bits: R C0 S0 C1 S1 R causes a retry by causing an UE (as if C0,S0,C1,S1 are all 1) C0 causes a chip error by injecting errors in symbols 69 and 68 S0 causes a symbol error in symbol 67 C1 causes a chip error by injecting errors in symbols 37 and 36 S1 causes a symbol error in symbol 35
45:49	RW	MBRCEICRQ_READ2_ERROR_TYPE: Selects the error to be injected for scrub read 2. same bit definitions as above.
50:54	RW	MBRCEICRQ_READ3_ERROR_TYPE: Selects the error to be injected for scrub read 3. same bit definitions as above.
55:56	RW	MBRCEICRQ_BANK_MASK_SELECT: selects masking of bank bits from address compare Values: COMPARE_BANK_BITS_0_TO_3=>0b00 COMPARE_BANK_BITS_1_TO_3=>0b01 COMPARE_BANK_BITS_2_TO_3=>0b10 COMPARE_BANK_BIT_3=>0b11
57:59	RW	MBRCEICRQ_ROW_MASK_SELECT: selects masking of row bits from address compare Values: COMPARE_ROW_BITS_0_TO_16=>0b000 COMPARE_ROW_BITS_1_TO_16=>0b001 COMPARE_ROW_BITS_2_TO_16=>0b010 COMPARE_ROW_BITS_3_TO_16=>0b011 COMPARE_ROW_BITS_4_TO_16=>0b100 COMPARE_ROW_BITS_5_TO_16=>0b101 COMPARE_ROW_BITS_6_TO_16=>0b110 COMPARE_ROW_BITS_7_TO_16=>0b111
60:62	RW	MBRCEICRQ_COLUMN_MASK_SELECT: selects masking of column bits from address compare Values: COMPARE_COLUMN_BITS_1_TO_11=>0b000 COMPARE_COLUMN_BITS_2_TO_11=>0b001 COMPARE_COLUMN_BITS_3_TO_11=>0b010 COMPARE_COLUMN_BITS_4_TO_11=>0b011 COMPARE_COLUMN_BITS_5_TO_11=>0b100 COMPARE_COLUMN_BITS_6_TO_11=>0b101 COMPARE_COLUMN_BITS_7_TO_11=>0b110 COMPARE_COLUMN_BITS_8_TO_11=>0b111
63	RW	MBRCEICRQ_DATAPATH_PARITY_ERROR_INJECT: When set, a datapath parity error (FIR 49) is injected for reads when the read data address matches bits (0:37) of this register, subject to the masks selected in bits 55:62. This enable bit does not automatically reset.

Register Name	***MBS Bit Steer Control Register 0***
Mnemonic	MBU.MBS.ECC23.MBSBS0
Address	000000000201149E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS0_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS0_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS0_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 1***
Mnemonic	MBU.MBS.ECC23.MBSBS1
Address	000000000201149F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS1_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS1_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS1_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 2***
Mnemonic	MBU.MBS.ECC23.MBSBS2
Address	00000000020114A0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS2_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS2_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS2_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 3***
Mnemonic	MBU.MBS.ECC23.MBSBS3
Address	00000000020114A1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS3_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS3_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS3_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 4***
Mnemonic	MBU.MBS.ECC23.MBSBS4
Address	00000000020114A2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS4_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS4_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS4_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 5***
Mnemonic	MBU.MBS.ECC23.MBSBS5
Address	00000000020114A3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS5_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS5_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS5_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 6***
Mnemonic	MBU.MBS.ECC23.MBSBS6
Address	00000000020114A4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS6_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS6_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS6_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS Bit Steer Control Register 7***
Mnemonic	MBU.MBS.ECC23.MBSBS7
Address	00000000020114A5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBSBS7_READ_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBSBS7_READ_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBSBS7_READ_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBS ECC Error Report Hold Register 0***
Mnemonic	MBU.MBS.ECC23.MBSECCERR0
Address	00000000020114A6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:32	RO	constant=0b00000000000000000000000000000000
33	ROX	MBSECCERR0_MBMS0_CHIP_PARITY: MBECCFIR(46) : mark_store0_chip_parity
34	ROX	MBSECCERR0_MBMS0_SYMBOL_PARITY: MBECCFIR(46) : mark_store0_symbol_parity
35	ROX	MBSECCERR0_MBMS0_PARITY: MBECCFIR(46) : mark_store0_parity
36	ROX	MBSECCERR0_MBMS1_CHIP_PARITY: MBECCFIR(46) : mark_store1_chip_parity
37	ROX	MBSECCERR0_MBMS1_SYMBOL_PARITY: MBECCFIR(46) : mark_store1_symbol_parity
38	ROX	MBSECCERR0_MBMS1_PARITY: MBECCFIR(46) : mark_store1_parity
39	ROX	MBSECCERR0_MBMS2_CHIP_PARITY: MBECCFIR(46) : mark_store2_chip_parity
40	ROX	MBSECCERR0_MBMS2_SYMBOL_PARITY: MBECCFIR(46) : mark_store2_symbol_parity

Bits	SCOM	Field Mnemonic: Description
41	ROX	MBSECCERR0_MBMS2_PARITY: MBECCFIR(46) : mark_store2_parity
42	ROX	MBSECCERR0_MBMS3_CHIP_PARITY: MBECCFIR(46) : mark_store3_chip_parity
43	ROX	MBSECCERR0_MBMS3_SYMBOL_PARITY: MBECCFIR(46) : mark_store3_symbol_parity
44	ROX	MBSECCERR0_MBMS3_PARITY: MBECCFIR(46) : mark_store3_parity
45	ROX	MBSECCERR0_MBMS4_CHIP_PARITY: MBECCFIR(46) : mark_store4_chip_parity
46	ROX	MBSECCERR0_MBMS4_SYMBOL_PARITY: MBECCFIR(46) : mark_store4_symbol_parity
47	ROX	MBSECCERR0_MBMS4_PARITY: MBECCFIR(46) : mark_store4_parity
48	ROX	MBSECCERR0_MBMS5_CHIP_PARITY: MBECCFIR(46) : mark_store5_chip_parity
49	ROX	MBSECCERR0_MBMS5_SYMBOL_PARITY: MBECCFIR(46) : mark_store5_symbol_parity
50	ROX	MBSECCERR0_MBMS5_PARITY: MBECCFIR(46) : mark_store5_parity
51	ROX	MBSECCERR0_MBMS6_CHIP_PARITY: MBECCFIR(46) : mark_store6_chip_parity
52	ROX	MBSECCERR0_MBMS6_SYMBOL_PARITY: MBECCFIR(46) : mark_store6_symbol_parity
53	ROX	MBSECCERR0_MBMS6_PARITY: MBECCFIR(46) : mark_store6_parity
54	ROX	MBSECCERR0_MBMS7_CHIP_PARITY: MBECCFIR(46) : mark_store7_chip_parity
55	ROX	MBSECCERR0_MBMS7_SYMBOL_PARITY: MBECCFIR(46) : mark_store7_symbol_parity
56	ROX	MBSECCERR0_MBMS7_PARITY: MBECCFIR(46) : mark_store7_parity
57:63	RO	constant=0b0000000

Register Name	***MBS ECC Error Report Hold Register 1***
Mnemonic	MBU.MBS.ECC23.MBSECCERR1
Address	00000000020114A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	MBSECCERR1_MEMORY_BIT_STEER_PARITY: MBECCFIR(46) : bit_steer_register_parity
8	RO	constant=0b0
9	ROX	MBSECCERR1_MBMMR_PARITY: MBECCFIR(46) : mbmmr_register_parity
10	RO	constant=0b0
11	ROX	MBSECCERR1_MBRCEICR_PARITY: MBECCFIR(48) : mbrceicr_register_parity
12:63	RO	constant=0b0000000000000000000000000000000000000000000000000000

Register Name	***SensorCache_LFIR***
Mnemonic	SCAC.SCAC_LFIR
Address	00000000020115C0 (SCOM) 00000000020115C1 (SCOM1) 00000000020115C2 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMINVADDR: I2CM(0) Invalid Address
1	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMINVWRITE: I2CM(1) Invalid Write
2	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMINVREAD: I2CM(2) Invalid Read,
3	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMAPAR: I2CM(3) Pib Address Parity Error
4	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMPAR: I2CM(4) Pib Parity Error
5	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMLBPAR: I2CM(5) LB parity error
6:9	RWX	WOX_AND	WOX_OR	SCAC_LFIR_EXPANSION: Reserved at 0 for external macro expansion reporting.
10	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMINVCMD: I2CM(45) : Invalid Command
11	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMPERR: I2CM(46) : Parity Error
12	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMOVERRUN: I2CM(47): Backend Overrun Error
13	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMACCESS: I2CM(48): Backend Access Error
14	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMARB: I2CM(49): Arbitration Lost Error
15	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMNACK: I2CM(50): Nack Received Error
16	RWX	WOX_AND	WOX_OR	SCAC_LFIR_I2CMSTOP: I2CM(53): Stop Error
17	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB1: Local PIB Response code 1 (decoded)
18	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB2: Local PIB Response code 2 (decoded)
19	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB3: Local PIB Response code 3 (decoded)
20	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB4: Local PIB Response code 4 (decoded)
21	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB5: Local PIB Response code 5 (decoded)
22	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB6: Local PIB Response code 6 (decoded)
23	RWX	WOX_AND	WOX_OR	SCAC_LFIR_LOCALPIB7: Local PIB Response code 7 (decoded)
24	RWX	WOX_AND	WOX_OR	SCAC_LFIR_STALLERROR: Stall Threshold Error The number of stall errors is larger than the stall error threshold defined in the Config Register. A stall error is when the Cache did not complete reading an enabled sensor within the the Timer Interval.
25	RWX	WOX_AND	WOX_OR	SCAC_LFIR_REGPARERR: Parity Error On internal Register (not including the PIBTarget register, see also RegParErrX)
26	RWX	WOX_AND	WOX_OR	SCAC_LFIR_REGPARERRX: Parity Error on PibTarget Register. A dedicated FIR is provided for this register since this register determines the target address the PIB Master will be used. A failure in this register could result in an inappropriate access anywhere on the chip. Checkstop might be considered actionable for this error.
27:31	RWX	WOX_AND	WOX_OR	SCAC_LFIR_RESERVED_27_31: Reserved
32	RWX	WOX_AND	WOX_OR	SCAC_LFIR_SMERR: State Machine Kaput Ctrl Logic Error. Went Bye Bye.
33	RWX	WOX_AND	WOX_OR	SCAC_LFIR_REGACCERR: A write to either SensorAddressMap, I2CMCtrl or PIBtarget registers occurred while the Master Enable was on. This has the potential to corrupt the PIB bus.
34	RWX	WOX_AND	WOX_OR	SCAC_LFIR_RESETERR: A PIB Error occurred while attempting to initiate a RESET command to the I2CM
35	RWX	WOX_AND	WOX_OR	SCAC_LFIR_INTERNAL_SCOM_ERROR: Internal Scom Error
36	RWX	WOX_AND	WOX_OR	SCAC_LFIR_INTERNAL_SCOM_ERROR_CLONE: Internal Som Error Clone
37:63	RO	N/A	N/A	constant=0b00000000000000000000000000

Register Name	*SensorCache FIR Mask Register*
Mnemonic	SCAC.SCAC_FIRMASK
Address	00000000020115C3 (SCOM) 00000000020115C4 (SCOM1) 00000000020115C5 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:36	RW	WO_AND	WO_OR	SCAC_FIRMASK_FIRMASK: See corresponding FIR bit positions.
37:63	RO	N/A	N/A	constant=0b00000000000000000000000000000

Register Name	*SensorCache FIR Action 0 Register*
Mnemonic	SCAC.SCAC_FIRACTION0
Address	00000000020115C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:36	RO	SCAC_FIRACTION0_FIRACTION0: See corresponding FIR bit positions.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	*SensorCache FIR Action 1 Register*
Mnemonic	SCAC.SCAC_FIRACTION1
Address	00000000020115C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:36	RO	SCAC_FIRACTION1_FIRACTION1: See corresponding FIR bit positions.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	*SensorCache FIR WOF Register*
Mnemonic	SCAC.SCAC_FIRWOF
Address	00000000020115C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:36	RWX_WCLRREG	SCAC_FIRWOF_FIRWOF: See corresponding FIR bit positions.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	***SensorCache_Data0_3***
Mnemonic	SCAC.SCAC_DATA0_3
Address	00000000020115CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	SCAC_DATA0_3_CRITTRIP0: Critical Trip Alarm for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
1	ROX	SCAC_DATA0_3_ABOVETRIP0: Above Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Upper Alarm Trip Value This must be cleared by firmware in the sensor.
2	ROX	SCAC_DATA0_3_BELOWTRIP0: Below Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
3	ROX	SCAC_DATA0_3_SIGNBIT0: Sign Bit for Sensor 0 0: Positive 1 : Negative
4:13	ROX	SCAC_DATA0_3_TEMPERATURE0: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
14:15	ROX	SCAC_DATA0_3_STATUS0: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11
16	ROX	SCAC_DATA0_3_CRITTRIP1: Critical Trip Alarm for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
17	ROX	SCAC_DATA0_3_ABOVETRIP1: Above Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Upper Alarm Trip Value This must be cleared by firmware in the sensor.
18	ROX	SCAC_DATA0_3_BELOWTRIP1: Below Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
19	ROX	SCAC_DATA0_3_SIGNBIT1: Sign Bit for Sensor 0 0: Positive 1 : Negative
20:29	ROX	SCAC_DATA0_3_TEMPERATURE1: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
30:31	ROX	SCAC_DATA0_3_STATUS1: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11
32	ROX	SCAC_DATA0_3_CRITTRIP2: Critical Trip Alarm for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
33	ROX	SCAC_DATA0_3_ABOVETRIP2: Above Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Upper Alarm Trip Value This must be cleared by firmware in the sensor.

Bits	SCOM	Field Mnemonic: Description
34	ROX	SCAC_DATA0_3_BELOWTRIP2: Below Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
35	ROX	SCAC_DATA0_3_SIGNBIT2: Sign Bit for Sensor 0 0: Positive 1 : Negative
36:45	ROX	SCAC_DATA0_3_TEMPERATURE2: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
46:47	ROX	SCAC_DATA0_3_STATUS2: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11
48	ROX	SCAC_DATA0_3_CRITTRIP3: Critical Trip Alarm for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
49	ROX	SCAC_DATA0_3_ABOVETRIP3: Above Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature exceeded the Upper Alarm Trip Value This must be cleared by firmware in the sensor.
50	ROX	SCAC_DATA0_3_BELOWTRIP3: Below Alarm Window for Sensor 0 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
51	ROX	SCAC_DATA0_3_SIGNBIT3: Sign Bit for Sensor 0 0: Positive 1 : Negative
52:61	ROX	SCAC_DATA0_3_TEMPERATURE3: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
62:63	ROX	SCAC_DATA0_3_STATUS3: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11

Register Name	***SensorCache_Data4_7***
Mnemonic	SCAC.SCAC_DATA4_7
Address	00000000020115CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	SCAC_DATA4_7_CRITTRIP4: Critical Trip Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
1	ROX	SCAC_DATA4_7_ALARMTRIP4: Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Alarm Trip Value This must be cleared by firmware in the sensor.

Bits	SCOM	Field Mnemonic: Description
2	ROX	SCAC_DATA4_7_BELOWTRIP4: Below Alarm Window for Sensor 4 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
3	ROX	SCAC_DATA4_7_SIGNBIT4: Sign Bit for Sensor 4 0: Positive 1 : Negative
4:13	ROX	SCAC_DATA4_7_TEMPERATURE4: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
14:15	ROX	SCAC_DATA4_7_STATUS4: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11
16	ROX	SCAC_DATA4_7_CRITTRIP5: Critical Trip Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
17	ROX	SCAC_DATA4_7_ALARMTRIP5: Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Alarm Trip Value This must be cleared by firmware in the sensor.
18	ROX	SCAC_DATA4_7_BELOWTRIP5: Below Alarm Window for Sensor 4 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
19	ROX	SCAC_DATA4_7_SIGNBIT5: Sign Bit for Sensor 4 0: Positive 1 : Negative
20:29	ROX	SCAC_DATA4_7_TEMPERATURE5: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
30:31	ROX	SCAC_DATA4_7_STATUS5: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11
32	ROX	SCAC_DATA4_7_CRITTRIP6: Critical Trip Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
33	ROX	SCAC_DATA4_7_ALARMTRIP6: Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Alarm Trip Value This must be cleared by firmware in the sensor.
34	ROX	SCAC_DATA4_7_BELOWTRIP6: Below Alarm Window for Sensor 4 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
35	ROX	SCAC_DATA4_7_SIGNBIT6: Sign Bit for Sensor 4 0: Positive 1 : Negative
36:45	ROX	SCAC_DATA4_7_TEMPERATURE6: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)

Bits	SCOM	Field Mnemonic: Description
46:47	ROX	SCAC_DATA4_7_STATUS6: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11
48	ROX	SCAC_DATA4_7_CRITTRIP7: Critical Trip Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Critical Trip Value This must be cleared by firmware in the sensor
49	ROX	SCAC_DATA4_7_ALARMTRIP7: Alarm for Sensor 4 0 : normal 1 : Sensor reports temperature exceeded the Alarm Trip Value This must be cleared by firmware in the sensor.
50	ROX	SCAC_DATA4_7_BELOWTRIP7: Below Alarm Window for Sensor 4 0 : normal 1 : Sensor reports temperature below the Lower Alarm Trip Value This must be cleared by firmware in the sensor.
51	ROX	SCAC_DATA4_7_SIGNBIT7: Sign Bit for Sensor 4 0: Positive 1 : Negative
52:61	ROX	SCAC_DATA4_7_TEMPERATURE7: Temperature Let A=(4:11), B=(12:13). Temperature is A + B4 (Celsius)
62:63	ROX	SCAC_DATA4_7_STATUS7: Status Indicator Next Sampling Period began before this sensor was read or the Master Enable is off, of the individual Sensor is Disabled. If the subsequent read completes on time, this will return to valid reading SensorData may be accurate, but stale. If due to a stall, the StallError FIR will be set. The SensorData was not returned correctly either due to parity error or PIB Bus Error code. Will return to valid if next PIB access to this sensor is valid, but a FIR will be set; Refer to FIR for exact error. Sensor Data should not be considered valid while this enum is present. Sensor Data is valid, and has been valid since the last time this register was read. Sensor Data is valid and has not yet been read by a SCOM. This field will return to 10 after this register is read. Bits 0:13 always return the PIB Return data irregardless of error. Values: STALLED__OR_DISABLED_=>0b00 ERROR_=>0b01 VALID_READING_=>0b10 VALID_READING_NEW=>0b11

Register Name	***SensorCache_Enable***
Mnemonic	SCAC.SCAC_ENABLE
Address	00000000020115CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	SCAC_ENABLE_ENABLESENSOR0: Enable Sensor Device Mapped to SensorMap0 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
1	RW	SCAC_ENABLE_ENABLESENSOR1: Enable Sensor Device Mapped to SensorMap1 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
2	RW	SCAC_ENABLE_ENABLESENSOR2: Enable Sensor Device Mapped to SensorMap2 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
3	RW	SCAC_ENABLE_ENABLESENSOR3: Enable Sensor Device Mapped to SensorMap3 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
4	RW	SCAC_ENABLE_ENABLESENSOR4: Enable Sensor Device Mapped to SensorMap4 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.

Bits	SCOM	Field Mnemonic: Description
5	RW	SCAC_ENABLE_ENABLESENSOR5: Enable Sensor Device Mapped to SensorMap5 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
6	RW	SCAC_ENABLE_ENABLESENSOR6: Enable Sensor Device Mapped to SensorMap6 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
7	RW	SCAC_ENABLE_ENABLESENSOR7: Enable Sensor Device Mapped to SensorMap7 (See SensorMap Register) 0: The sensor will not be read. 1: The sensor will be read.
8:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***SensorCache_AddressMap***
Mnemonic	SCAC.SCAC_ADDRMAP
Address	00000000020115CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	SCAC_ADDRMAP_SENSORMAP0: Address Map for Sensor Data 0
4:7	RW	SCAC_ADDRMAP_SENSORMAP1: Address Map for Sensor Data 1
8:11	RW	SCAC_ADDRMAP_SENSORMAP2: Address Map for Sensor Data 2
12:15	RW	SCAC_ADDRMAP_SENSORMAP3: Address Map for Sensor Data 3
16:19	RW	SCAC_ADDRMAP_SENSORMAP4: Address Map for Sensor Data 4
20:23	RW	SCAC_ADDRMAP_SENSORMAP5: Address Map for Sensor Data 5
24:27	RW	SCAC_ADDRMAP_SENSORMAP6: Address Map for Sensor Data 6
28:31	RW	SCAC_ADDRMAP_SENSORMAP7: Address Map for Sensor Data 7
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***SensorCache_Config***
Mnemonic	SCAC.SCAC_CONFIG
Address	00000000020115CE (SCOM) 00000000020115CF (SCOM1) 00000000020115D0 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_MASTERENABLE: Master Enable & Reset. 0: The Sensor Cache is disabled Reset. 1: The sensor cache is enabled.
1	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_SYNCSELECT: Sync Selection 0: The timer is activated by a Hang pulse 1: The timer is activated by an external signal. Typically this would be the OCC_Read signal that the performance counters use.
2:7	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_EXPANSION0: Reserved Spares.
8:10	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_EXPANSION1: Reserved for future expansion of the interval timer.
11:15	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_INTERVALTIMER: The Interval Timer. Actual Cache Period is this value multiplied by the time-base pulse input. Note... 0 is 32.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
16:23	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_STALLTHRESHOLD: Stall Threshold Counter. Aggregate number of stall errors before the stall_err fir is asserted. Note... 0 is an invalid value. The counter is reset to 128, and the largest acceptable value is 255.
24	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_ERRRESET: Clears all c_err_rpts in the SCAC_LFIR register.
25	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_REGPARINJ: Register Parity Error Inject Pulses a latch that would inject incorrect parity on the addrmap register on the following reg write command. This should activate SCAC_LFIR bit 25.
26	RW	WO_OR	WO_CLEAR	SCAC_CONFIG_SMINJ: State Machine Error Inject Pulses a latch that forces the scac state machine into a non-1hot state. This should activate SCAC_LFIR bit 32.
27:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000

Register Name	***SensorCache_I2CMCtrl***
Mnemonic	SCAC.SCAC_I2CMCTRL
Address	00000000020115D1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	SCAC_I2CMCTRL_I2CCMD: The value that will be sent to I2CM Control Register, bits 0-7 to request the I2C Read of the sensor. Should be set to 10010010, indicating a read with stop and no address or continue.
8:11	RW	SCAC_I2CMCTRL_I2CSEGMENT: The value that will be sent to I2CM Control register, bits 8-11 to request the I2C Read of the sensor. This field contains the device address of the sensor. The actual sensor number will be appended to bits 12:14 by the hardware automatically. This value will be asserted as A6,A5,A4,A3 during the address phase of the I2C transaction. This should normally be set to 0011.
12:14	RW	SCAC_I2CMCTRL_SPARE1: The hardware will automatically put the specific target sensor address into I2CM control register bits 12:14 completing the I2C device 7-bits address field. This will become A2,A1,A0 during the address phase of the I2C transaction. This actual register is does nothing and is just a placeholder for commonality.
15	RW	SCAC_I2CMCTRL_I2CRNW: The value that will be sent to I2CM Control Register bits 15 to request the I2C Read of the sensor. This field contains the read request and should be set to '1'.
16:17	RW	SCAC_I2CMCTRL_I2CSPEED: The value that will be sent to I2CM Contr0l Register bits 16:17 to request the I2C Read of the sensor. This field contains the I2C clock speed. It should be set to 01 00 : 100Khz 01 : 400Khz 10 : 3400Khz 11 : 50Khz.
18:22	RW	SCAC_I2CMCTRL_I2CPORT: The value that will be sent to I2CM Contr0l Register bits 18:22 to request the I2C Read of the sensor. This field contains the PIB Control Register Port Number.
23:24	RW	SCAC_I2CMCTRL_I2CADRLEN: The value that will be sent to I2CM Contr0l Register bits 24:25 to request the I2C Read of the sensor. This field contains the Register Address length and should be set to 00. Bit 23 of the I2CM Control Register is unused.
25	RW	SCAC_I2CMCTRL_I2CENHANCED: The value that will be sent to I2CM Contr0l Register bits 26 to request the I2C Read of the sensor. This field contains the I2CM Enhanced Mode setting and should be set to 0.
26:27	RW	SCAC_I2CMCTRL_CTRLOFFSET: Offset from PibTarget where the I2CM control register is. Should be set to 00
28:29	RW	SCAC_I2CMCTRL_STATOFFSET: Offset from PibTarget where the I2CM status register is. Should be set to 10
30:31	RW	SCAC_I2CMCTRL_RESETOFFSET: Offset from PibTarget where the I2CM reset register is. Should be set to 01

Bits	SCOM	Field Mnemonic: Description
32:63	RW	SCAC_I2CMCTRL_I2CFIFODATA: The value that will be sent to I2CM Control Register bits 32-63 to request the I2C Read of the sensor. This field contains optional FIFO data. Can be used to set the pointer register. Should be set to 05000000.

Register Name	***SensorCache_PibTarget***
Mnemonic	SCAC.SCAC_PIBTARGET
Address	00000000020115D2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RW	SCAC_PIBTARGET_PRIMARYBASE: Base Address of the Primary I2CM. Should be 0x000A0000 on the memory buffer.
32:63	RW	SCAC_PIBTARGET_SPAREBASE: Base Address of the Spare I2CM. Should be 0x000A0020 on the memory buffer.

Register Name	***SensorCache_ActionMask***
Mnemonic	SCAC.SCAC_ACTIONMASK
Address	00000000020115D3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:34	RW	SCAC_ACTIONMASK_ACTIONMASK: Action Masks for FIR. (=1) for Corresponding bit position of FIR enables main state machine to attempt a I2CM Reset to clear the error.
35:63	RO	constant=0b00000000000000000000000000000

Register Name	***SensorCache Error Report Hold Register***
Mnemonic	SCAC.SCAC_ERRRPT
Address	00000000020115D4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	SCAC_ERRRPT_SCAC_ACTIONMASK_PE_HOLD_OUT: SCAC_LFIR(25) : scac action mask parity
1	ROX	SCAC_ERRRPT_SCAC_ADDRMAP_PE_HOLD_OUT: SCAC_LFIR(25) : scac address map parity
2	ROX	SCAC_ERRRPT_SCAC_CONFIG_PE_HOLD_OUT: SCAC_LFIR(25) : scac configuration register parity
3	ROX	SCAC_ERRRPT_SCAC_DATA0_3_PE_HOLD_OUT: SCAC_LFIR(25) : scac sensor data 0-3 register parity
4	ROX	SCAC_ERRRPT_SCAC_DATA_7_PE_HOLD_OUT: SCAC_LFIR(25) : scac sensor data 4-7 register parity
5	ROX	SCAC_ERRRPT_SCAC_ENABLE_PE_HOLD_OUT: SCAC_LFIR(25) : scac enable parity
6	ROX	SCAC_ERRRPT_SCAC_I2CMCTRL_PE_HOLD_OUT: SCAC_LFIR(25) : scac i2cmctrl parity
7	ROX	SCAC_ERRRPT_SCAC_MSM_HOLD_OUT: SCAC_LFIR(32) : scac main state machine 1-hot error

Bits	SCOM	Field Mnemonic: Description
8	ROX	SCAC_ERRRPT_SCAC_PGSM_HOLD_OUT: SCAC_LFIR(32) : scac pib glue state machine 1-hot error
9	ROX	SCAC_ERRRPT_SCAC_PIBTARGET_PE_HOLD_OUT: SCAC_LFIR(25) : scac pib target parity
10:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation Register (MBSFIR)***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSFIRQ
Address	0000000002011600 (SCOM) 0000000002011601 (SCOM1) 0000000002011602 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBSFIRQ_SCOM_PAR_ERRORS: SCOM Parity Errors
1	RWX	WOX_AND	WOX_OR	MBSFIRQ_MBX_PAR_ERRORS: MBX parity Errors
2:14	RWX	WOX_AND	WOX_OR	MBSFIRQ_RESERVED_2_14: RESERVED
15	RWX	WOX_AND	WOX_OR	MBSFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
16	RWX	WOX_AND	WOX_OR	MBSFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation Mask Register (MBSFIRMASK)***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSFIRMASK
Address	0000000002011603 (SCOM) 0000000002011604 (SCOM1) 0000000002011605 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBSFIRMASK_SCOM_PAR_ERRORS: Masks FIR(0)
1	RW	WO_AND	WO_OR	MBSFIRMASK_MBX_PAR_ERRORS: Masks FIR(1)
2:14	RW	WO_AND	WO_OR	MBSFIRMASK_RESERVED_2_14: Reserved
15	RW	WO_AND	WO_OR	MBSFIRMASK_INTERNAL_SCOM_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	MBSFIRMASK_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(16)
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation Action0 Register (MBSFIRACT0)***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSFIRACT0
Address	0000000002011606 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSFIRACT0_SCOM_PAR_ERRORS: Action 0 FIR(0)
1	RW	MBSFIRACT0_MBX_PAR_ERRORS: Action 0 FIR(1)
2:14	RW	MBSFIRACT0_RESERVED_2_14: RESERVED
15	RW	MBSFIRACT0_INTERNAL_SCOM_ERROR: Action 0 FIR(15)
16	RW	MBSFIRACT0_INTERNAL_SCOM_ERROR_CLONE: Action 0 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation Action1 Register (MBSFIRACT1)***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSFIRACT1
Address	0000000002011607 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSFIRACT1_SCOM_PAR_ERRORS: Action 1 FIR(0)
1	RW	MBSFIRACT1_MBX_PAR_ERRORS: Action 1 FIR(1)
2:14	RW	MBSFIRACT1_RESERVED_2_14: RESERVED
15	RW	MBSFIRACT1_INTERNAL_SCOM_ERROR: Action 1 FIR(15)
16	RW	MBSFIRACT1_INTERNAL_SCOM_ERROR_CLONE: Action 1 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation WOF Register (MBSFIRWOF)***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSFIRWOF
Address	0000000002011608 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBSFIRWOF_SCOM_PAR_ERRORS: Who's On First (WOF0) Register
1	ROX	MBSFIRWOF_MBX_PAR_ERRORS: Who's On First (WOF1) Register
2:14	ROX	MBSFIRWOF_RESERVED_2_14: RESERVED
15	ROX	MBSFIRWOF_INTERNAL_SCOM_ERROR: Who's On First (WOF15) Register
16	ROX	MBSFIRWOF_INTERNAL_SCOM_ERROR_CLONE: Who's On First (WOF16) Register
17:63	RO	constant=0b00000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA0
Address	0000000000201160A (SCOM_DUALPORT_WRITE) 0000000003010655 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA0_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA1
Address	0000000000201160B (SCOM_DUALPORT_WRITE) 0000000003010656 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA1_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA2
Address	0000000000201160C (SCOM_DUALPORT_WRITE) 0000000003010657 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA2_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA3
Address	0000000000201160D (SCOM_DUALPORT_WRITE) 0000000003010658 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA3_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA4
Address	000000000201160E (SCOM_DUALPORT_WRITE) 0000000003010659 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA4_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA5
Address	000000000201160F (SCOM_DUALPORT_WRITE) 000000000301065A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA5_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA6
Address	0000000002011610 (SCOM_DUALPORT_WRITE) 000000000301065B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA6_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA7
Address	0000000002011611 (SCOM_DUALPORT_WRITE) 000000000301065C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA7_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data ECC 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC0
Address	0000000002011612 (SCOM_DUALPORT_WRITE) 000000000301065D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC1
Address	0000000002011613 (SCOM_DUALPORT_WRITE) 000000000301065E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC2
Address	0000000002011614 (SCOM_DUALPORT_WRITE) 000000000301065F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC3
Address	0000000002011615 (SCOM_DUALPORT_WRITE) 0000000003010660 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC4
Address	0000000002011616 (SCOM_DUALPORT_WRITE) 0000000003010661 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC5
Address	0000000002011617 (SCOM_DUALPORT_WRITE) 0000000003010662 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC6
Address	0000000002011618 (SCOM_DUALPORT_WRITE) 0000000003010663 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF0_DATA_ECC7
Address	0000000002011619 (SCOM_DUALPORT_WRITE) 0000000003010664 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA0
Address	0000000002011614A (SCOM_DUALPORT_WRITE) 0000000003010665 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA0_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA1
Address	0000000002011615B (SCOM_DUALPORT_WRITE) 0000000003010666 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA1_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA2
Address	0000000002011616C (SCOM_DUALPORT_WRITE) 0000000003010667 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA2_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA3
Address	0000000002011617D (SCOM_DUALPORT_WRITE) 0000000003010668 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA3_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA4
Address	000000000201161E (SCOM_DUALPORT_WRITE) 0000000003010669 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA4_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA5
Address	000000000201161F (SCOM_DUALPORT_WRITE) 000000000301066A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA5_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA6
Address	0000000002011620 (SCOM_DUALPORT_WRITE) 000000000301066B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA6_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA7
Address	0000000002011621 (SCOM_DUALPORT_WRITE) 000000000301066C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA7_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data ECC 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC0
Address	0000000002011622 (SCOM_DUALPORT_WRITE) 000000000301066D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC1
Address	0000000002011623 (SCOM_DUALPORT_WRITE) 000000000301066E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC2
Address	0000000002011624 (SCOM_DUALPORT_WRITE) 000000000301066F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC3
Address	0000000002011625 (SCOM_DUALPORT_WRITE) 0000000003010670 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC4
Address	0000000002011626 (SCOM_DUALPORT_WRITE) 0000000003010671 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC5
Address	0000000002011627 (SCOM_DUALPORT_WRITE) 0000000003010672 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC6
Address	0000000002011628 (SCOM_DUALPORT_WRITE) 0000000003010673 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF1_DATA_ECC7
Address	0000000002011629 (SCOM_DUALPORT_WRITE) 0000000003010674 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA0
Address	0000000002201162A (SCOM_DUALPORT_WRITE) 0000000003010675 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA0_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA1
Address	0000000002201162B (SCOM_DUALPORT_WRITE) 0000000003010676 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA1_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA2
Address	0000000002201162C (SCOM_DUALPORT_WRITE) 0000000003010677 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA2_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA3
Address	0000000002201162D (SCOM_DUALPORT_WRITE) 0000000003010678 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA3_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA4
Address	0000000002011632E (SCOM_DUALPORT_WRITE) 0000000003010679 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA4_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA5
Address	0000000002011632F (SCOM_DUALPORT_WRITE) 000000003301067A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA5_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA6
Address	0000000002011630 (SCOM_DUALPORT_WRITE) 000000003301067B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA6_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA7
Address	0000000002011631 (SCOM_DUALPORT_WRITE) 000000000301067C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA7_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data ECC 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC0
Address	0000000002011632 (SCOM_DUALPORT_WRITE) 000000000301067D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC1
Address	0000000002011633 (SCOM_DUALPORT_WRITE) 000000000301067E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC2
Address	0000000002011634 (SCOM_DUALPORT_WRITE) 000000000301067F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC3
Address	0000000002011635 (SCOM_DUALPORT_WRITE) 0000000003010680 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC4
Address	0000000002011636 (SCOM_DUALPORT_WRITE) 0000000003010681 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC5
Address	0000000002011637 (SCOM_DUALPORT_WRITE) 0000000003010682 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC6
Address	0000000002011638 (SCOM_DUALPORT_WRITE) 0000000003010683 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF2_DATA_ECC7
Address	0000000002011639 (SCOM_DUALPORT_WRITE) 0000000003010684 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA0
Address	0000000002011 63A (SCOM_DUALPORT_WRITE) 0000000003010685 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA0_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA1
Address	0000000002011 63B (SCOM_DUALPORT_WRITE) 0000000003010686 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA1_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA2
Address	0000000002011 63C (SCOM_DUALPORT_WRITE) 0000000003010687 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA2_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA3
Address	0000000002011 63D (SCOM_DUALPORT_WRITE) 0000000003010688 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA3_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA4
Address	0000000002011643E (SCOM_DUALPORT_WRITE) 0000000003010689 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA4_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA5
Address	0000000002011643F (SCOM_DUALPORT_WRITE) 000000000301068A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA5_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA6
Address	0000000002011640 (SCOM_DUALPORT_WRITE) 000000000301068B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA6_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA7
Address	0000000002011641 (SCOM_DUALPORT_WRITE) 000000000301068C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA7_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data ECC 0*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC0
Address	0000000002011642 (SCOM_DUALPORT_WRITE) 000000000301068D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 1*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC1
Address	0000000002011643 (SCOM_DUALPORT_WRITE) 000000000301068E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 2*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC2
Address	0000000002011644 (SCOM_DUALPORT_WRITE) 000000000301068F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 3*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC3
Address	0000000002011645 (SCOM_DUALPORT_WRITE) 0000000003010690 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 4*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC4
Address	0000000002011646 (SCOM_DUALPORT_WRITE) 0000000003010691 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 5*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC5
Address	0000000002011647 (SCOM_DUALPORT_WRITE) 0000000003010692 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC6
Address	0000000002011648 (SCOM_DUALPORT_WRITE) 0000000003010693 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF3_DATA_ECC7
Address	0000000002011649 (SCOM_DUALPORT_WRITE) 0000000003010694 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 0***
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC0
Address	0000000002201164A (SCOM_DUALPORT_WRITE) 0000000003010695 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 1***
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC1
Address	0000000002201164B (SCOM_DUALPORT_WRITE) 0000000003010696 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 2***
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC2
Address	000000000201164C (SCOM_DUALPORT_WRITE) 0000000003010697 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 3***
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC3
Address	0000000002201164D (SCOM_DUALPORT_WRITE) 0000000003010698 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 4***
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC4
Address	0000000002201164E (SCOM_DUALPORT_WRITE) 0000000003010699 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_SPARE_ECC_BITS: Spare ECC bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 5***
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC5
Address	000000000201164F (SCOM_DUALPORT_WRITE) 000000000301069A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_SPARE_ECC_BITS: Spare ECC bits used for future expansion

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	*Maintenance 65th Byte And 64B ECC Register 6*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC6
Address	0000000002011650 (SCOM_DUALPORT_WRITE) 000000000301069B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_SPARE_ECC_BITS: Spare ECC bits used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	*Maintenance 65th Byte And 64B ECC Register 7*
Mnemonic	MBU.MBX.MAINT0.MAINT_BUFF_65TH_BYTE_64B_ECC7
Address	0000000002011651 (SCOM_DUALPORT_WRITE) 000000000301069C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	*MBS Memory Scrub/Read Error Count Register 0*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSEC0Q
Address	0000000002011653 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RWX	MBSEC0Q_SOFT_CE_COUNT: Soft CE Count This is a 12-bit count of soft CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.

Bits	SCOM	Field Mnemonic: Description
12:23	RWX	MBSEC0Q_INTERMITTENT_CE_COUNT: Intermittent CE Count This is a 12-bit count of intermittent CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
24:35	RWX	MBSEC0Q_HARD_CE_COUNT: Hard CE Count This is a 12-bit count of hard CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
36:47	RWX	MBSEC0Q_SCE_COUNT: Symbol CE Count This is a 12-bit count of symbol CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
48:59	RWX	MBSEC0Q_MCE_COUNT: Mark CE Count This is a 12-bit count of mark CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
60:63	RO	constant=0b0000

Register Name	***MBS Memory Scrub/Read Error Count Register 1***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSEC1Q
Address	0000000002011654 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RWX	MBSEC1Q_RCE_COUNT: Retry CE Count This is a 12-bit count of retry CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
12:23	RWX	MBSEC1Q_MPE_COUNT: Mark Place Error Count This is a 12-bit count of mark place error events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
24:35	RWX	MBSEC1Q_UE_COUNT: UE Count This is a 12-bit count of UE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
36:63	RO	constant=0b00000000000000000000000000

Register Name	***MBS Memory Scrub/Read Error Threshold Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSTRQ
Address	0000000002011655 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBSTRQ_SOFT_CE_COUNT_THRESHOLD_ATTN_STOP: Select Soft CE Count Threshold sets ETE Special Attentionstops maint op. When set, ETE special attention is set when Soft_CE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stop s immediately or at the end of the current rank
1	RWX	MBSTRQ_INTERMITTENT_CE_COUNT_THRESHOLD_ATTN_STOP: Select Intermittent CE Count Threshold sets ETE Special Attentionstops maint op. When set, ETE special attention is set when Intermittent_CE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stops immediately or at the end of the current rank

Bits	SCOM	Field Mnemonic: Description
2	RWX	MBSTRQ_HARD_CE_COUNT_THRESHOLD_ATTN_STOP: Select Hard CE Count Threshold sets ETE Special Attention stops maint op. When set, ETE special attention is set when Hard_CE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stops immediately or at the end of the current rank
3	RWX	MBSTRQ_RCE_COUNT_THRESHOLD_ATTN_STOP: Select RCE Count Threshold sets ETE Special Attention stops maint op. When set, ETE special attention is set when RCE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stops immediately or at the end of the current rank
4:15	RWX	MBSTRQ_SOFT_CE_COUNT_THRESHOLD: Soft CE Count Threshold. Compare against the Soft CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
16:27	RWX	MBSTRQ_INTERMITTENT_CE_COUNT_THRESHOLD: Intermittent CE Count Threshold. Compare against the Intermittent CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
28:39	RWX	MBSTRQ_HARD_CE_COUNT_THRESHOLD: Hard CE Count Threshold. Compare against the Hard CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
40:51	RWX	MBSTRQ_RETRY_CE_COUNT_THRESHOLD: Retry CE Count Threshold. Compare against the Retry CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
52	RWX	MBSTRQ_RESET_KEEPER: Reset keeper for MBS clock domain
53	RWX	MBSTRQ_RESET_ALL_ERROR_COUNT_REGISTERS: Reset all error count and symbol error count registers Set to clear registers. Hardware will reset this bit to zero after registers are cleared.
54	RWX	MBSTRQ_DISABLE_RESET_ERROR_REG_RANK_END: Disable reset of error count and symbol error count registers at end of rank When set, the se registers will not be reset at the end of a rank. When this bit is reset to zero, the error registers will be reset when the end of a rank is reached and the MBMACA address has incremented to the next valid rank during execution of a multi-address command. Note: The only way to clear the count and syndrome registers is by setting bit 11 above or incrementing the MBMACA address past the end of a rank during a multi-address command. Starting and stopping scrubs will NOT reset these registers.
55	RWX	MBSTRQ_SOFT_CE_INCR_SYMBOL_COUNT: soft ce increment symbol counters When set, a soft CE detected by a readscrub op will increment one of the 72 8-bit a symbol error counters
56	RWX	MBSTRQ_INTERMIT_INCR_SYMBOL_COUNT: intermittent ce increment symbol counters When set, an intermittent CE detected by a readscrub op will increment one of the 72 8-bit symbol error counters
57	RWX	MBSTRQ_HARD_CE_INCR_SYMBOL_COUNT: Hard ce increment symbol counters When set, a hard CE detected by a readscrub op will increment one of the 72 8-bit a symbol error counters
58	RWX	MBSTRQ_MCE_INCR_SYMBOL_COUNT: MCE increment symbol count (but would need to split out failed symbol info from chip mark....TBD, extra credit)
59	RWX	MBSTRQ_UE_TRAP: Trap data only with UEs enabled When set, only read data with UEs will be saved in the Maint buffers. When not set, all data from a read will be saved into the Maint buffers regardless if it had an error or not.
60:61	RWX	MBSTRQ_RESERVED_60_61: Reserved
62	RWX	MBSTRQ_INTERMITTENT_NCE_INJECT: Intermittent NCE Inject not implemented This logic has been removed and replaced with the error injector in the ECC macro.
63	RWX	MBSTRQ_RESERVED_63: Reserved

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 0***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC0Q
Address	0000000002011656 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC0Q_SYMBOL_0_ERROR_COUNT: Symbol 0 error count
8:15	RWX	MBSSYMEC0Q_SYMBOL_1_ERROR_COUNT: Symbol 1 error count
16:23	RWX	MBSSYMEC0Q_SYMBOL_2_ERROR_COUNT: Symbol 2 error count
24:31	RWX	MBSSYMEC0Q_SYMBOL_3_ERROR_COUNT: Symbol 3 error count
32:39	RWX	MBSSYMEC0Q_SYMBOL_4_ERROR_COUNT: Symbol 4 error count
40:47	RWX	MBSSYMEC0Q_SYMBOL_5_ERROR_COUNT: Symbol 5 error count
48:55	RWX	MBSSYMEC0Q_SYMBOL_6_ERROR_COUNT: Symbol 6 error count
56:63	RWX	MBSSYMEC0Q_SYMBOL_7_ERROR_COUNT: Symbol 7 error count

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 1***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC1Q
Address	0000000002011657 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC1Q_SYMBOL_8_ERROR_COUNT: Symbol 8 error count
8:15	RWX	MBSSYMEC1Q_SYMBOL_9_ERROR_COUNT: Symbol 9 error count
16:23	RWX	MBSSYMEC1Q_SYMBOL_10_ERROR_COUNT: Symbol 10 error count
24:31	RWX	MBSSYMEC1Q_SYMBOL_11_ERROR_COUNT: Symbol 11 error count
32:39	RWX	MBSSYMEC1Q_SYMBOL_12_ERROR_COUNT: Symbol 12 error count
40:47	RWX	MBSSYMEC1Q_SYMBOL_13_ERROR_COUNT: Symbol 13 error count
48:55	RWX	MBSSYMEC1Q_SYMBOL_14_ERROR_COUNT: Symbol 14 error count
56:63	RWX	MBSSYMEC1Q_SYMBOL_15_ERROR_COUNT: Symbol 15 error count

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 2***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC2Q
Address	0000000002011658 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC2Q_SYMBOL_16_ERROR_COUNT: Symbol 16 error count
8:15	RWX	MBSSYMEC2Q_SYMBOL_17_ERROR_COUNT: Symbol 17 error count
16:23	RWX	MBSSYMEC2Q_SYMBOL_18_ERROR_COUNT: Symbol 18 error count
24:31	RWX	MBSSYMEC2Q_SYMBOL_19_ERROR_COUNT: Symbol 19 error count
32:39	RWX	MBSSYMEC2Q_SYMBOL_20_ERROR_COUNT: Symbol 20 error count
40:47	RWX	MBSSYMEC2Q_SYMBOL_21_ERROR_COUNT: Symbol 21 error count
48:55	RWX	MBSSYMEC2Q_SYMBOL_22_ERROR_COUNT: Symbol 22 error count
56:63	RWX	MBSSYMEC2Q_SYMBOL_23_ERROR_COUNT: Symbol 23 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 3*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC3Q
Address	0000000002011659 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC3Q_SYMBOL_24_ERROR_COUNT: Symbol 24 error count
8:15	RWX	MBSSYMEC3Q_SYMBOL_25_ERROR_COUNT: Symbol 25 error count
16:23	RWX	MBSSYMEC3Q_SYMBOL_26_ERROR_COUNT: Symbol 26 error count
24:31	RWX	MBSSYMEC3Q_SYMBOL_27_ERROR_COUNT: Symbol 27 error count
32:39	RWX	MBSSYMEC3Q_SYMBOL_28_ERROR_COUNT: Symbol 28 error count
40:47	RWX	MBSSYMEC3Q_SYMBOL_29_ERROR_COUNT: Symbol 29 error count
48:55	RWX	MBSSYMEC3Q_SYMBOL_30_ERROR_COUNT: Symbol 30 error count
56:63	RWX	MBSSYMEC3Q_SYMBOL_31_ERROR_COUNT: Symbol 31 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 4*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC4Q
Address	000000000201165A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC4Q_SYMBOL_32_ERROR_COUNT: Symbol 32 error count
8:15	RWX	MBSSYMEC4Q_SYMBOL_33_ERROR_COUNT: Symbol 33 error count
16:23	RWX	MBSSYMEC4Q_SYMBOL_34_ERROR_COUNT: Symbol 34 error count
24:31	RWX	MBSSYMEC4Q_SYMBOL_35_ERROR_COUNT: Symbol 35 error count
32:39	RWX	MBSSYMEC4Q_SYMBOL_36_ERROR_COUNT: Symbol 36 error count
40:47	RWX	MBSSYMEC4Q_SYMBOL_37_ERROR_COUNT: Symbol 37 error count
48:55	RWX	MBSSYMEC4Q_SYMBOL_38ERROR_COUNT: Symbol 38error count
56:63	RWX	MBSSYMEC4Q_SYMBOL_39_ERROR_COUNT: Symbol 39 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 5*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC5Q
Address	000000000201165B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC5Q_SYMBOL_40_ERROR_COUNT: Symbol 40 error count
8:15	RWX	MBSSYMEC5Q_SYMBOL_41_ERROR_COUNT: Symbol 41 error count

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	MBSSYMEC5Q_SYMBOL_42_ERROR_COUNT: Symbol 42 error count
24:31	RWX	MBSSYMEC5Q_SYMBOL_43_ERROR_COUNT: Symbol 43 error count
32:39	RWX	MBSSYMEC5Q_SYMBOL_44_ERROR_COUNT: Symbol 44 error count
40:47	RWX	MBSSYMEC5Q_SYMBOL_45_ERROR_COUNT: Symbol 45 error count
48:55	RWX	MBSSYMEC5Q_SYMBOL_46_ERROR_COUNT: Symbol 46 error count
56:63	RWX	MBSSYMEC5Q_SYMBOL_47_ERROR_COUNT: Symbol 47 error count

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 6***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC6Q
Address	000000000201165C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC6Q_SYMBOL_48_ERROR_COUNT: Symbol 48 error count
8:15	RWX	MBSSYMEC6Q_SYMBOL_49_ERROR_COUNT: Symbol 49 error count
16:23	RWX	MBSSYMEC6Q_SYMBOL_50_ERROR_COUNT: Symbol 50 error count
24:31	RWX	MBSSYMEC6Q_SYMBOL_51_ERROR_COUNT: Symbol 51 error count
32:39	RWX	MBSSYMEC6Q_SYMBOL_52_ERROR_COUNT: Symbol 52 error count
40:47	RWX	MBSSYMEC6Q_SYMBOL_53_ERROR_COUNT: Symbol 53 error count
48:55	RWX	MBSSYMEC6Q_SYMBOL_54_ERROR_COUNT: Symbol 54 error count
56:63	RWX	MBSSYMEC6Q_SYMBOL_55_ERROR_COUNT: Symbol 55 error count

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 7***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC7Q
Address	000000000201165D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC7Q_SYMBOL_56_ERROR_COUNT: Symbol 56 error count
8:15	RWX	MBSSYMEC7Q_SYMBOL_57_ERROR_COUNT: Symbol 57 error count
16:23	RWX	MBSSYMEC7Q_SYMBOL_58_ERROR_COUNT: Symbol 58 error count
24:31	RWX	MBSSYMEC7Q_SYMBOL_59_ERROR_COUNT: Symbol 59 error count
32:39	RWX	MBSSYMEC7Q_SYMBOL_60_ERROR_COUNT: Symbol 60 error count
40:47	RWX	MBSSYMEC7Q_SYMBOL_61_ERROR_COUNT: Symbol 61 error count
48:55	RWX	MBSSYMEC7Q_SYMBOL_62_ERROR_COUNT: Symbol 62 error count
56:63	RWX	MBSSYMEC7Q_SYMBOL_63_ERROR_COUNT: Symbol 63 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 8*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSSYMEC8Q
Address	000000000201165E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC8Q_SYMBOL_64_ERROR_COUNT: Symbol 64 error count
8:15	RWX	MBSSYMEC8Q_SYMBOL_65_ERROR_COUNT: Symbol 65 error count
16:23	RWX	MBSSYMEC8Q_SYMBOL_66_ERROR_COUNT: Symbol 66 error count
24:31	RWX	MBSSYMEC8Q_SYMBOL_67_ERROR_COUNT: Symbol 67 error count
32:39	RWX	MBSSYMEC8Q_SYMBOL_68_ERROR_COUNT: Symbol 68 error count
40:47	RWX	MBSSYMEC8Q_SYMBOL_69_ERROR_COUNT: Symbol 69 error count
48:55	RWX	MBSSYMEC8Q_SYMBOL_70_ERROR_COUNT: Symbol 70 error count
56:63	RWX	MBSSYMEC8Q_SYMBOL_71_ERROR_COUNT: Symbol 71 error count

Register Name	*MBS Memory Error Vector Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBSEVRQ
Address	000000000201165F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RWX	MBSEVRQ_ERR_VECTOR0: Error Vector 0 This is the 56-bit error vector associated with the last memory error detected. 0:7 - E1 8:15 - E2 16:23 - E3 24:31 - E4 32:39 - E 40:47 - R 48:55 - Error Mask E1 is the error magnitude for the symbol pointed to by the mark x1 E2 is the error magnitude for the symbol pointed to by the mark x2 E3 is the error magnitude for the symbol pointed to by the mark x3 E4 is the error magnitude for the symbol pointed to by the mark x4 E is the error magnitude for a NEW error (associated with NCE) R is the error location, coded as a Galois Field index, for the new error (associated with NCE) Error Mask is the 8bit xor mask that indicates which bits in the corrected symbol were flipped in order to the correct the SCE
56:63	RO	constant=0b00000000

Register Name	*MBS Memory NCE Error Address Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBNCERQ
Address	0000000002011660 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBNCERQ_RD_NCE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBNCERQ_RD_NCE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.

Bits	SCOM	Field Mnemonic: Description
7:10	RWX	MBNCERQ_RD_NCE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBNCERQ_RD_NCE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBNCERQ_RD_NCE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40	RWX	MBNCERQ_RD_NCE_ERR_OCCURRED__AFTER_UE_RETRY: If set, this error occurred after a retry for a memory read UE
41:63	RO	constant=0b00000000000000000000000

Register Name	***MBS Memory RCE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBRCERQ
Address	0000000002011661 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBRCERQ_RD_RCE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBRCERQ_RD_RCE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBRCERQ_RD_RCE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBRCERQ_RD_RCE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBRCERQ_RD_RCE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40	RWX	MBRCERQ_RD_RCE_ERR_OCCURRED_AFTER_UE_RETRY: If set, this error occurred after a retry for a memory read UE
41:63	RO	constant=0b00000000000000000000000

Register Name	***MBS Memory MPE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBMPERQ
Address	0000000002011662 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBMPERQ_RD_MPE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBMPERQ_RD_MPE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.

Bits	SCOM	Field Mnemonic: Description
7:10	RWX	MBMPERQ_RD_MPE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBMPERQ_RD_MPE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBMPERQ_RD_MPE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40	RWX	MBMPERQ_RD_MPE_ERR_OCCURRED_AFTER_UE_RETRY: If set, this error occurred after a retry for a memory read UE
41:63	RO	constant=0b00000000000000000000000

Register Name	***MBS Memory UE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBUERQ
Address	0000000002011663 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBUERQ_RD_UE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBUERQ_RD_UE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBUERQ_RD_UE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBUERQ_RD_UE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBUERQ_RD_UE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40:41	RWX	MBUERQ_RESERVED_40_41: RESERVED
42:63	RO	constant=0b00000000000000000000

Register Name	***Port A Error Counter 1***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCB_ERRCNTA1Q
Address	0000000002011664 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR0: Nibble 0 Error Counter
7:13	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR1: Nibble 1 Error Counter
14:20	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR2: Nibble 2 Error Counter
21:27	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR3: Nibble 3 Error Counter

Bits	SCOM	Field Mnemonic: Description
28:34	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR4: Nibble 4 Error Counter
35:41	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR5: Nibble 5 Error Counter
42:48	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR6: Nibble 6 Error Counter
49:55	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR7: Nibble 7 Error Counter
56:62	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR8: Nibble 8 Error Counter
63	RWX	MCB_ERRCNTA1Q_RESERVED_63: RESERVED

Register Name	***Port A Error Counter 2***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCB_ERRCNTA2Q
Address	0000000002011665 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR9: Nibble 9 Error Counter
7:13	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR10: Nibble 10 Error Counter
14:20	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR11: Nibble 11 Error Counter
21:27	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR12: Nibble 12 Error Counter
28:34	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR13: Nibble 13 Error Counter
35:41	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR14: Nibble 14 Error Counter
42:48	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR15: Nibble 15 Error Counter
49:55	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR16: Nibble 16 Error Counter
56:62	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR17: Nibble 17 Error Counter
63	RWX	MCB_ERRCNTA2Q_ERR_CNTR_OVERFLOW: Error Counter Overflow

Register Name	***Port A Error Counter 3***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCB_ERRCNTA3Q
Address	0000000002011666 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTA3Q_NIBBLE_ERR_PORTA_CNTR18: Nibble 18 Error Counter
7:13	RWX	MCB_ERRCNTA3Q_NIBBLE_ERR_PORTA_CNTR19: Nibble 19 Error Counter
14:63	RWX	MCB_ERRCNTA3Q_RESERVED_14_63: RESERVED

Register Name	*Port B Error Counter 1*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCB_ERRCNTB1Q
Address	0000000002011667 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR0: Nibble 0 Error Counter
7:13	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR1: Nibble 1 Error Counter
14:20	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR2: Nibble 2 Error Counter
21:27	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR3: Nibble 3 Error Counter
28:34	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR4: Nibble 4 Error Counter
35:41	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR5: Nibble 5 Error Counter
42:48	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR6: Nibble 6 Error Counter
49:55	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR7: Nibble 7 Error Counter
56:62	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR8: Nibble 8 Error Counter
63	RWX	MCB_ERRCNTB1Q_RESERVED_63: RESERVED

Register Name	*Port B Error Counter 2*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCB_ERRCNTB2Q
Address	0000000002011668 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR9: Nibble 9 Error Counter
7:13	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR10: Nibble 10 Error Counter
14:20	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR11: Nibble 11 Error Counter
21:27	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR12: Nibble 12 Error Counter
28:34	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR13: Nibble 13 Error Counter
35:41	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR14: Nibble 14 Error Counter
42:48	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR15: Nibble 15 Error Counter
49:55	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR16: Nibble 16 Error Counter
56:62	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR17: Nibble 17 Error Counter
63	RWX	MCB_ERRCNTB2Q_ERR_CNTR_OVERFLOW: Error Counter Overflow

Register Name	*Port B Error Counter 3*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCB_ERRCNTB3Q
Address	0000000002011669 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTB3Q_NIBBLE_ERR_PORTB_CNTR18: Nibble 18 Error Counter
7:13	RWX	MCB_ERRCNTB3Q_NIBBLE_ERR_PORTB_CNTR19: Nibble 19 Error Counter
14:63	RWX	MCB_ERRCNTB3Q_RESERVED_14_63: RESERVED

Register Name	***Port A Error Map Register 1***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBEMA1Q
Address	000000000201166A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMA1Q_ERROR_MAP_PORTA_RNK0: Rank 0 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMA1Q_ERROR_MAP_PORTA_RNK1: Rank 1 Error Map
40:59	RWX	MCBEMA1Q_ERROR_MAP_PORTA_RNK2: Rank 2 Error Map
60:63	RWX	MCBEMA1Q_RESERVED_60_63: RESERVED

Register Name	***Port A Error Map Register 2***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBEMA2Q
Address	000000000201166B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMA2Q_ERROR_MAP_PORTA_RNK3: Rank 3 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMA2Q_ERROR_MAP_PORTA_RNK4: Rank 4 Error Map
40:59	RWX	MCBEMA2Q_ERROR_MAP_PORTA_RNK5: Rank 5 Error Map
60:63	RWX	MCBEMA2Q_RESERVED_60_63: RESERVED

Register Name	*Port A Error Map Register 3*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBEMA3Q
Address	000000000201166C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMA3Q_ERROR_MAP_PORTA_RNK6: Rank 6 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMA3Q_ERROR_MAP_PORTA_RNK7: Rank 7 Error Map
40:63	RWX	MCBEMA3Q_RESERVED_40_63: RESERVED

Register Name	*Port B Error Map Register 1*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBEMB1Q
Address	000000000201166D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMB1Q_ERROR_MAP_PORTB_RNK0: Rank 0 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMB1Q_ERROR_MAP_PORTB_RNK1: Rank 1 Error Map
40:59	RWX	MCBEMB1Q_ERROR_MAP_PORTB_RNK2: Rank 2 Error Map
60:63	RWX	MCBEMB1Q_RESERVED_60_63: RESERVED

Register Name	*Port B Error Map Register 2*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBEMB2Q
Address	000000000201166E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMB2Q_ERROR_MAP_PORTB_RNK3: Rank 3 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMB2Q_ERROR_MAP_PORTB_RNK4: Rank 4 Error Map
40:59	RWX	MCBEMB2Q_ERROR_MAP_PORTB_RNK5: Rank 5 Error Map
60:63	RWX	MCBEMB2Q_RESERVED_60_63: RESERVED

Register Name	***Port B Error Map Register 3***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBEMB3Q
Address	000000000201166F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMB3Q_ERROR_MAP_PORTB_RNK6: Rank 6 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMB3Q_ERROR_MAP_PORTB_RNK7: Rank 7 Error Map
40:63	RWX	MCBEMB3Q_RESERVED_40_63: RESERVED

Register Name	***Port A Error Map And Status Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBSTATAQ
Address	0000000002011670 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MCBSTATAQ_PORTA_CE_ERR: CE Detected (ECC Mode only) 0 - No CE Detected 1 - CE Detected
1	ROX	MCBSTATAQ_PORTA_UE_ERR: UE Detected (ECC Mode only) 0 - No UE Detected 1 - UE Detected
2	ROX	MCBSTATAQ_PORTA_ERR_TRAP_OVERFLOW: Error Trap Overflow for both Port A and B 0 - 8 or less errors have been detected on both port A and B 1 - More than 8 errors have been detected on both port A and B
3:7	ROX	MCBSTATAQ_PORTA_CNTL_TRAP_SUBTST_NUM: Subtest Pointer

Bits	SCOM	Field Mnemonic: Description
8:10	ROX	MCBSTATAQ_PORTA_ERR_LOG_PTR: Error Log Pointer - In MCB mode the pointer points to the address where the next error will be stored. That is, the last error was written to (Error Log Pointer -1)
11:23	ROX	MCBSTATAQ_RESERVED_11_23: RESERVED
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***Port B Error Map And Status Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBSTATBQ
Address	0000000002011671 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MCBSTATBQ_PORTB_CE_ERR: CE Detected (ECC Mode only) 0 - No CE Detected 1 - CE Detected
1	ROX	MCBSTATBQ_PORTB_UE_ERR: UE Detected (ECC Mode only) 0 - No UE Detected 1 - UE Detected
2	ROX	MCBSTATBQ_PORTB_ERR_TRAP_OVERFLOW: Error Trap Overflow for both Port A and B 0 - 8 or less errors have been detected on both port A and B 1 - More than 8 errors have been detected on both port A and B
3:7	ROX	MCBSTATBQ_PORTB_CNTL_TRAP_SUBTST_NUM: Subtest Pointer
8:10	ROX	MCBSTATBQ_PORTB_ERR_LOG_PTR: Error Log Pointer - In MCB mode the pointer points to the address where the next error will be stored. That is, the last error was written to (Error Log Pointer -1)
11:23	ROX	MCBSTATBQ_RESERVED_11_23: RESERVED
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***Port A Compare Mask Register 1***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBCMA1Q
Address	0000000002011672 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBCMA1Q_COMPARE_MASK_A: Port A Compare Mask (0:63)

Register Name	***Port B Compare Mask Register 1***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBCMB1Q
Address	0000000002011673 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBCMB1Q_COMPARE_MASK_B: Port B Compare Mask (0:63)

Register Name	***Port A & B Compare Mask Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MCBCMABQ
Address	0000000002011674 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MCBCMABQ_COMPARE_MASK_A: Port A Compare Mask (64:79)
16:31	RW	MCBCMABQ_COMPARE_MASK_B: Port B Compare Mask (64:79)
32	RW	MCBCMABQ_CFG_STORE_FAIL: Cfg_store_fail 0 - store first 8 fails 1 - store last 8 fails
33	RW	MCBIST_ENABLE_CE_TRAP: Enable CE to be trapped in MCBIST ECC Mode 0 - disable trapping 1 - enable trapping
34	RW	MCBIST_ENABLE_MPE_TRAP: Enable MPE to be trapped in MCBIST ECC Mode 0 - disable trapping 1 - enable trapping
35	RW	MCBCMABQ_ENABLE_UE_TRAP: Enable UE to be trapped in MCBIST ECC Mode 0 - disable trapping 1 - enable trapping
36	RW	MCBIST_STOP_ON_NTH_FAIL: Stop on subtest when nth fail is detected. MCBCFGQ(62) turns on the stop on error. If that bit is not set, this register is a don;t care. Values: STOP_AT_THE_END_OF_A_SUSBTEST_WHEN_1_OR_MORE_FAILS_IS_DETECTED=>0b0 STOP_AT_THE_END_OF_A_SUSBTEST_WHEN_8_OR_MORE_FAILS_IS_DETECTED=>0b1
37	RW	MCBCMABQ_ARRAY_READ_ENABLE: Array SCOM Read Enable Values: DISABLE_SCOM_READS_TO_SRB_AND_PF_BUFFERS=>0b0 ENABLES_SCOM_READS_TO_SRB_AND_PF_BUFFERS=>0b1
38:63	RW	MCBCMABQ_RESERVED_38_63: RESERVED

Register Name	***MBS Random Data Seed 0 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS0Q
Address	0000000002011675 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 1 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS1Q
Address	0000000002011676 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 2 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS2Q
Address	0000000002011677 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 3 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS3Q
Address	0000000002011678 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 4 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS4Q
Address	0000000002011679 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 5 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS5Q
Address	000000000201167A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 6 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS6Q
Address	000000000201167B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 7 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS7Q
Address	000000000201167C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 8 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDS8Q
Address	000000000201167D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED0: DQ(8) Burst 1 Random Data Seed
8:15	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED1: DQ(8) Burst 2 Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED2: DQ(8) Burst 3 Random Data Seed
24:31	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED3: DQ(8) Burst 4 Random Data Seed
32:39	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED4: DQ(8) Burst 5 Random Data Seed
40:47	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED5: DQ(8) Burst 6 Random Data Seed
48:55	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED6: DQ(8) Burst 7 Random Data Seed
56:63	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED7: DQ(8) Burst 8 Random Data Seed

Register Name	***MBS Random Data Seed Spare Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBRDSSPQ
Address	000000000201167E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED0: DQ(9) Burst 1 Random Data Seed
8:15	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED1: DQ(9) Burst 2 Random Data Seed
16:23	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED2: DQ(9) Burst 3 Random Data Seed
24:31	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED3: DQ(9) Burst 4 Random Data Seed
32:39	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED4: DQ(9) Burst 5 Random Data Seed
40:47	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED5: DQ(9) Burst 6 Random Data Seed
48:55	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED6: DQ(9) Burst 7 Random Data Seed
56:63	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED7: DQ(9) Burst 8 Random Data Seed

Register Name	***MBS Data Rotate Seed Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBDRSRQ
Address	000000000201167F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBDRSRQ_CFG_DATA_ROT_SEED: Bits 0:63 of the Data Rotate Seed

Register Name	***Data Rotate Configuration Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBDRCRQ
Address	0000000002011680 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBS_MCBDRCRQ_CFG_DATA_ROT: Bits to shift: Values: ROTATE_1_BIT=>0b0001 ROTATE_2_BITS=>0b0010 ROTATE_3_BITS=>0b0011 ROTATE_4_BITS=>0b0100 ROTATE_5_BITS=>0b0101 ROTATE_6_BITS=>0b0110 ROTATE_7_BITS=>0b0111 ROTATE_8_BITS=>0b1000 ROTATE_9_BITS=>0b1001 ROTATE_10_BITS=>0b1010 ROTATE_11_BITS=>0b1011 ROTATE_12_BITS=>0b1100 ROTATE_13_BITS=>0b1101 ROTATE_14_BITS=>0b1110 ROTATE_15_BITS=>0b1111
4:19	RW	MBS_MCBDRCRQ_CFG_DATA_ROT_SEED: Bits 64:79 of the Data Rotate Seed
20	RW	MBS_MCBDRCRQ_CFG_INVERT_DATA: These bits control the final inversion of data over to the xpt. Bit 20 = Invert MA Data
21:63	RW	MBS_MCBDRCRQ_RESERVED_21_63: Not used

Register Name	***MBS Fixed Data Seed Burst 0 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD0Q
Address	0000000002011681 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD0Q_CFG_FIXED_SEED: Fixed Data Seed(0:63)

Register Name	***MBS Fixed Data Seed Burst 1 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD1Q
Address	0000000002011682 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD1Q_CFG_FIXED_SEED: Fixed Data Seed(72:135)

Register Name	***MBS Fixed Data Seed Burst 2 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD2Q
Address	0000000002011683 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD2Q_CFG_FIXED_SEED: Fixed Data Seed(144:207)

Register Name	***MBS Fixed Data Seed Burst 3 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD3Q
Address	0000000002011684 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD3Q_CFG_FIXED_SEED: Fixed Data Seed(216:279)

Register Name	***MBS Fixed Data Seed Burst 4 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD4Q
Address	0000000002011685 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD4Q_CFG_FIXED_SEED: Fixed Data Seed(288:351)

Register Name	***MBS Fixed Data Seed Burst 5 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD5Q
Address	0000000002011686 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD5Q_CFG_FIXED_SEED: Fixed Data Seed(360:423)

Register Name	***MBS Fixed Data Seed Burst 6 Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD6Q
Address	0000000002011687 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD6Q_CFG_FIXED_SEED: Fixed Data Seed(432:495)

Register Name	*MBS Fixed Data Seed Burst 7 Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFD7Q
Address	0000000002011688 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD7Q_CFG_FIXED_SEED: Fixed Data Seed(504:567)

Register Name	*MBS Fixed Data Seed Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFDQ
Address	0000000002011689 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBFDQ_CFG_FIXED_SEED1: DQ(8) Burst 1 Fixed Data Seed(64:71)
8:15	RW	MBS_MCBFDQ_CFG_FIXED_SEED2: DQ(8) Burst 2 Fixed Data Seed(136:143)
16:23	RW	MBS_MCBFDQ_CFG_FIXED_SEED3: DQ(8) Burst 3 Fixed Data Seed(208:215)
24:31	RW	MBS_MCBFDQ_CFG_FIXED_SEED4: DQ(8) Burst 4 Fixed Data Seed(280:287)
32:39	RW	MBS_MCBFDQ_CFG_FIXED_SEED5: DQ(8) Burst 5 Fixed Data Seed(352:359)
40:47	RW	MBS_MCBFDQ_CFG_FIXED_SEED6: DQ(8) Burst 6 Fixed Data Seed(424:431)
48:55	RW	MBS_MCBFDQ_CFG_FIXED_SEED7: DQ(8) Burst 7 Fixed Data Seed(496:503)
56:63	RW	MBS_MCBFDQ_CFG_FIXED_SEED8: DQ(8) Burst 8 Fixed Data Seed(568:575)

Register Name	*MBS Fixed Data Seed Spare Register*
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBS_MCBFDSPQ
Address	000000002201168A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED1: DQ(9) Burst 1 Fixed Data Seed(64:71)
8:15	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED2: DQ(9) Burst 2 Fixed Data Seed(136:143)
16:23	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED3: DQ(9) Burst 3 Fixed Data Seed(208:215)
24:31	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED4: DQ(9) Burst 4 Fixed Data Seed(280:287)
32:39	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED5: DQ(9) Burst 5 Fixed Data Seed(352:359)
40:47	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED6: DQ(9) Burst 6 Fixed Data Seed(424:431)
48:55	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED7: DQ(9) Burst 7 Fixed Data Seed(496:503)
56:63	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED8: DQ(9) Burst 8 Fixed Data Seed(568:575)

Register Name	***MBX Error Status Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBXERRSTATQ
Address	000000000201168F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBXERRSTATQ_WDONE_PAR_ERROR: Parity Error in the wdone IF linked to MBSFIR bit 1
1	ROX	MBXERRSTATQ_RDTAG_RDCHECK_ERROR: Parity Error in the Read Sequence IF linked to MBSFIR bit 1
2	ROX	MBXERRSTATQ_RDTAG_PAR_ERROR: Parity Error in the rdtag IF linked to MBSFIR bit 1
3	ROX	MBXERRSTATQ_RDTAG_PAR_RC_ERROR: Parity Error in the rdtag RowColumn IF linked to MBSFIR bit 1
4:63	ROX	MBXERRSTATQ_RESERVED_4_63: RESERVED

Register Name	***MBX Error Injection Register***
Mnemonic	MBU.MBS.MCBISTS01.SCOMFIR.MBXERRINJQ
Address	0000000002011690 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBXERRINJQ_RCMD_ERR_INJ_MODE: Parity Error inject mode into the RCMD array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
1	RW	MBXERRINJQ_RCMD_ERR_INJ: Parity Error inject into the RCMD array
2	RW	MBXERRINJQ_WRD_CE_ERR_INJ_MODE: CE Error inject mode into the WRD array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	MBXERRINJQ_WRD_CE_ERR_INJ: CE Error inject into the WRD array
4	RW	MBXERRINJQ_WRD_UE_ERR_INJ_MODE: UE Error inject mode into the WRD array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
5	RW	MBXERRINJQ_WRD_UE_ERR_INJ: UE Error inject into the WRD array
6	RW	MBXERRINJQ_MAINT_CE_ERR_INJ_MODE: CE Error inject mode into the Maint array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
7	RW	MBXERRINJQ_MAINT_CE_ERR_INJ: CE Error inject into the Maint array
8	RW	MBXERRINJQ_MAINT_UE_ERR_INJ_MODE: UE Error inject mode into the Maint array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
9	RW	MBXERRINJQ_MAINT_UE_ERR_INJ: UE Error inject into the Maint array

Bits	SCOM	Field Mnemonic: Description
10	RW	MBXERRINJQ_SCOM_PE_ERR_INJ_MODE: SCOM Parity Error inject mode Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
11	RW	MBXERRINJQ_SCOM_PE_ERR_INJ: SCOM Parity Error inject
12:63	RW	MBXERRINJQ_RESERVED_12_63: RESERVED

Register Name	***MBS01 PFB Buffer 0 Data 0***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA0
Address	0000000002011691 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA0_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 1***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA1
Address	0000000002011692 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA1_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 2***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA2
Address	0000000002011693 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA2_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 3***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA3
Address	0000000002011694 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA3_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 4***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA4
Address	0000000002011695 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA4_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 5***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA5
Address	0000000002011696 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA5_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 6***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA6
Address	0000000002011697 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA6_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS01 PFB Buffer 0 Data 7***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF0_DATA7
Address	0000000002011698 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF0_DATA7_MBS01_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	*MBS01 PFB Buffer 1 Data 0*
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA0
Address	0000000002011699 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA0_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	*MBS01 PFB Buffer 1 Data 1*
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA1
Address	000000000201169A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA1_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	*MBS01 PFB Buffer 1 Data 2*
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA2
Address	000000000201169B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA2_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	*MBS01 PFB Buffer 1 Data 3*
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA3
Address	000000000201169C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA3_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS01 PFB Buffer 1 Data 4***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA4
Address	000000000201169D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA4_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS01 PFB Buffer 1 Data 5***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA5
Address	000000000201169E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA5_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS01 PFB Buffer 1 Data 6***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA6
Address	000000000201169F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA6_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS01 PFB Buffer 1 Data 7***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF1_DATA7
Address	00000000020116A0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF1_DATA7_MBS01_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS01 PFB Buffer 2 Data 0***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA0
Address	00000000020116A1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA0_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 1***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA1
Address	00000000020116A2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA1_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 2***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA2
Address	00000000020116A3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA2_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 3***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA3
Address	00000000020116A4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA3_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 4***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA4
Address	00000000020116A5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA4_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 5***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA5
Address	00000000020116A6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA5_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 6***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA6
Address	00000000020116A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA6_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 2 Data 7***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF2_DATA7
Address	00000000020116A8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF2_DATA7_MBS01_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS01 PFB Buffer 3 Data 0***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA0
Address	00000000020116A9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA0_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 1***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA1
Address	00000000020116AA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA1_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 2***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA2
Address	00000000020116AB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA2_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 3***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA3
Address	00000000020116AC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA3_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 4***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA4
Address	00000000020116AD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA4_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 5***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA5
Address	00000000020116AE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA5_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 6***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA6
Address	00000000020116AF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA6_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 PFB Buffer 3 Data 7***
Mnemonic	MBU.MBS.PFB.MBS01_PFB_BUFF3_DATA7
Address	00000000020116B0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_PFB_BUFF3_DATA7_MBS01_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS01 SRB Buffer 0 Data 0***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA0
Address	00000000020116B1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA0_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 1***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA1
Address	00000000020116B2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA1_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 2***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA2
Address	00000000020116B3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA2_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 3***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA3
Address	00000000020116B4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA3_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 4***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA4
Address	00000000020116B5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA4_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 5***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA5
Address	00000000020116B6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA5_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 6***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA6
Address	00000000020116B7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA6_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 0 Data 7***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF0_DATA7
Address	00000000020116B8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF0_DATA7_MBS01_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS01 SRB Buffer 1 Data 0***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA0
Address	00000000020116B9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA0_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 1***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA1
Address	00000000020116BA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA1_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 2***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA2
Address	00000000020116BB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA2_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 3***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA3
Address	00000000020116BC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA3_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 4***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA4
Address	00000000020116BD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA4_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 5***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA5
Address	00000000020116BE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA5_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 6***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA6
Address	00000000020116BF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA6_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 1 Data 7***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF1_DATA7
Address	00000000020116C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF1_DATA7_MBS01_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS01 SRB Buffer 2 Data 0***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA0
Address	00000000020116C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA0_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 1***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA1
Address	00000000020116C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA1_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 2***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA2
Address	00000000020116C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA2_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 3***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA3
Address	00000000020116C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA3_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 4***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA4
Address	00000000020116C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA4_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 5***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA5
Address	00000000020116C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA5_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 6***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA6
Address	00000000020116C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA6_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 2 Data 7***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF2_DATA7
Address	00000000020116C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF2_DATA7_MBS01_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS01 SRB Buffer 3 Data 0***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA0
Address	00000000020116C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA0_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 1***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA1
Address	00000000020116CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA1_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 2***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA2
Address	00000000020116CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA2_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 3***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA3
Address	00000000020116CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA3_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 4***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA4
Address	00000000020116CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA4_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 5***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA5
Address	00000000020116CE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA5_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 6***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA6
Address	00000000020116CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA6_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS01 SRB Buffer 3 Data 7***
Mnemonic	MBU.MBS.SRB.MBS01_SRB_BUFF3_DATA7
Address	00000000020116D0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS01_SRB_BUFF3_DATA7_MBS01_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	*MBS MCBIST Fault Isolation Register (MBSFIR)*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSFIRQ
Address	0000000002011700 (SCOM) 0000000002011701 (SCOM1) 0000000002011702 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBSFIRQ_SCOM_PAR_ERRORS: SCOM Parity Errors
1	RWX	WOX_AND	WOX_OR	MBSFIRQ_MBX_PAR_ERRORS: MBX parity Errors
2:14	RWX	WOX_AND	WOX_OR	MBSFIRQ_RESERVED_2_14: RESERVED
15	RWX	WOX_AND	WOX_OR	MBSFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
16	RWX	WOX_AND	WOX_OR	MBSFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBS MCBIST Fault Isolation Mask Register (MBSFIRMASK)*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSFIRMASK
Address	0000000002011703 (SCOM) 0000000002011704 (SCOM1) 0000000002011705 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBSFIRMASK_SCOM_PAR_ERRORS: Masks FIR(0)
1	RW	WO_AND	WO_OR	MBSFIRMASK_MBX_PAR_ERRORS: Masks FIR(1)
2:14	RW	WO_AND	WO_OR	MBSFIRMASK_RESERVED_2_14: Reserved
15	RW	WO_AND	WO_OR	MBSFIRMASK_INTERNAL_SCOM_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	MBSFIRMASK_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(16)
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBS MCBIST Fault Isolation Action0 Register (MBSFIRACT0)*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSFIRACT0
Address	0000000002011706 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSFIRACT0_SCOM_PAR_ERRORS: Action 0 FIR(0)
1	RW	MBSFIRACT0_MBX_PAR_ERRORS: Action 0 FIR(1)
2:14	RW	MBSFIRACT0_RESERVED_2_14: RESERVED
15	RW	MBSFIRACT0_INTERNAL_SCOM_ERROR: Action 0 FIR(15)

Bits	SCOM	Field Mnemonic: Description
16	RW	MBSFIRACT0_INTERNAL_SCOM_ERROR_CLONE: Action 0 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation Action1 Register (MBSFIRACT1)***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSFIRACT1
Address	0000000002011707 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSFIRACT1_SCOM_PAR_ERRORS: Action 1 FIR(0)
1	RW	MBSFIRACT1_MBX_PAR_ERRORS: Action 1 FIR(1)
2:14	RW	MBSFIRACT1_RESERVED_2_14: RESERVED
15	RW	MBSFIRACT1_INTERNAL_SCOM_ERROR: Action 1 FIR(15)
16	RW	MBSFIRACT1_INTERNAL_SCOM_ERROR_CLONE: Action 1 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBS MCBIST Fault Isolation WOF Register (MBSFIRWOF)***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSFIRWOF
Address	0000000002011708 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBSFIRWOF_SCOM_PAR_ERRORS: Who's On First (WOF0) Register
1	ROX	MBSFIRWOF_MBX_PAR_ERRORS: Who's On First (WOF1) Register
2:14	ROX	MBSFIRWOF_RESERVED_2_14: RESERVED
15	ROX	MBSFIRWOF_INTERNAL_SCOM_ERROR: Who's On First (WOF15) Register
16	ROX	MBSFIRWOF_INTERNAL_SCOM_ERROR_CLONE: Who's On First (WOF16) Register
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***Maintenance Buffer 0 Data 0***
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA0
Address	000000000201170A (SCOM_DUALPORT_WRITE) 0000000003010E55 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA0_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA1
Address	000000000201170B (SCOM_DUALPORT_WRITE) 0000000003010E56 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA1_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA2
Address	000000000201170C (SCOM_DUALPORT_WRITE) 0000000003010E57 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA2_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA3
Address	000000000201170D (SCOM_DUALPORT_WRITE) 0000000003010E58 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA3_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA4
Address	000000000201170E (SCOM_DUALPORT_WRITE) 0000000003010E59 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA4_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA5
Address	000000000201170F (SCOM_DUALPORT_WRITE) 0000000003010E5A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA5_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA6
Address	0000000002011710 (SCOM_DUALPORT_WRITE) 0000000003010E5B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA6_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA7
Address	0000000002011711 (SCOM_DUALPORT_WRITE) 0000000003010E5C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF0_DATA7_MAINT_BUFF0_DATA: Maintenance Buffer0 Data

Register Name	*Maintenance Buffer 0 Data ECC 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC0
Address	0000000002011712 (SCOM_DUALPORT_WRITE) 0000000003010E5D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC1
Address	0000000002011713 (SCOM_DUALPORT_WRITE) 0000000003010E5E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC2
Address	0000000002011714 (SCOM_DUALPORT_WRITE) 0000000003010E5F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC2_ECC: ECC bits for error inject for ECC mode

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC3
Address	0000000002011715 (SCOM_DUALPORT_WRITE) 0000000003010E60 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC4
Address	0000000002011716 (SCOM_DUALPORT_WRITE) 0000000003010E61 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC5
Address	0000000002011717 (SCOM_DUALPORT_WRITE) 0000000003010E62 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC5_ECC: ECC bits for error inject for ECC mode

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC6
Address	0000000002011718 (SCOM_DUALPORT_WRITE) 0000000003010E63 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 0 Data ECC 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF0_DATA_ECC7
Address	0000000002011719 (SCOM_DUALPORT_WRITE) 0000000003010E64 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF0_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF0_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA0
Address	000000002201171A (SCOM_DUALPORT_WRITE) 0000000003010E65 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA0_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA1
Address	000000000201171B (SCOM_DUALPORT_WRITE) 0000000003010E66 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA1_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA2
Address	000000000201171C (SCOM_DUALPORT_WRITE) 0000000003010E67 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA2_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA3
Address	000000000201171D (SCOM_DUALPORT_WRITE) 0000000003010E68 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA3_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA4
Address	000000000201171E (SCOM_DUALPORT_WRITE) 0000000003010E69 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA4_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA5
Address	0000000002011721F (SCOM_DUALPORT_WRITE) 0000000003010E6A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA5_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA6
Address	0000000002011720 (SCOM_DUALPORT_WRITE) 0000000003010E6B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA6_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA7
Address	0000000002011721 (SCOM_DUALPORT_WRITE) 0000000003010E6C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF1_DATA7_MAINT_BUFF1_DATA: Maintenance Buffer1 Data

Register Name	*Maintenance Buffer 1 Data ECC 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC0
Address	0000000002011722 (SCOM_DUALPORT_WRITE) 0000000003010E6D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC1
Address	0000000002011723 (SCOM_DUALPORT_WRITE) 0000000003010E6E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC2
Address	0000000002011724 (SCOM_DUALPORT_WRITE) 0000000003010E6F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC3
Address	0000000002011725 (SCOM_DUALPORT_WRITE) 0000000003010E70 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC4
Address	0000000002011726 (SCOM_DUALPORT_WRITE) 0000000003010E71 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC5
Address	0000000002011727 (SCOM_DUALPORT_WRITE) 0000000003010E72 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC6
Address	0000000002011728 (SCOM_DUALPORT_WRITE) 0000000003010E73 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 1 Data ECC 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF1_DATA_ECC7
Address	0000000002011729 (SCOM_DUALPORT_WRITE) 0000000003010E74 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF1_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF1_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA0
Address	000000002201172A (SCOM_DUALPORT_WRITE) 0000000003010E75 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA0_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA1
Address	000000000201172B (SCOM_DUALPORT_WRITE) 0000000003010E76 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA1_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA2
Address	000000000201172C (SCOM_DUALPORT_WRITE) 0000000003010E77 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA2_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA3
Address	000000000201172D (SCOM_DUALPORT_WRITE) 0000000003010E78 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA3_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA4
Address	000000000201172E (SCOM_DUALPORT_WRITE) 0000000003010E79 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA4_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA5
Address	000000000201172F (SCOM_DUALPORT_WRITE) 0000000003010E7A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA5_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA6
Address	0000000002011730 (SCOM_DUALPORT_WRITE) 0000000003010E7B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA6_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA7
Address	0000000002011731 (SCOM_DUALPORT_WRITE) 0000000003010E7C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF2_DATA7_MAINT_BUFF2_DATA: Maintenance Buffer2 Data

Register Name	*Maintenance Buffer 2 Data ECC 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC0
Address	0000000002011732 (SCOM_DUALPORT_WRITE) 0000000003010E7D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC1
Address	0000000002011733 (SCOM_DUALPORT_WRITE) 0000000003010E7E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC2
Address	0000000002011734 (SCOM_DUALPORT_WRITE) 0000000003010E7F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC3
Address	0000000002011735 (SCOM_DUALPORT_WRITE) 0000000003010E80 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC4
Address	0000000002011736 (SCOM_DUALPORT_WRITE) 0000000003010E81 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC5
Address	0000000002011737 (SCOM_DUALPORT_WRITE) 0000000003010E82 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC6
Address	0000000002011738 (SCOM_DUALPORT_WRITE) 0000000003010E83 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 2 Data ECC 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF2_DATA_ECC7
Address	0000000002011739 (SCOM_DUALPORT_WRITE) 0000000003010E84 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF2_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF2_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA0
Address	000000002201173A (SCOM_DUALPORT_WRITE) 0000000003010E85 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA0_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA1
Address	000000000201173B (SCOM_DUALPORT_WRITE) 0000000003010E86 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA1_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA2
Address	000000000201173C (SCOM_DUALPORT_WRITE) 0000000003010E87 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA2_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA3
Address	000000000201173D (SCOM_DUALPORT_WRITE) 0000000003010E88 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA3_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA4
Address	000000000201173E (SCOM_DUALPORT_WRITE) 0000000003010E89 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA4_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA5
Address	0000000002011737F (SCOM_DUALPORT_WRITE) 0000000003010E8A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA5_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA6
Address	0000000002011740 (SCOM_DUALPORT_WRITE) 0000000003010E8B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA6_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA7
Address	0000000002011741 (SCOM_DUALPORT_WRITE) 0000000003010E8C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0:63	WO	RO	MAINT_BUFF3_DATA7_MAINT_BUFF3_DATA: Maintenance Buffer3 Data

Register Name	*Maintenance Buffer 3 Data ECC 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC0
Address	0000000002011742 (SCOM_DUALPORT_WRITE) 0000000003010E8D (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC0_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC0_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 1*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC1
Address	0000000002011743 (SCOM_DUALPORT_WRITE) 0000000003010E8E (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC1_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC1_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 2*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC2
Address	0000000002011744 (SCOM_DUALPORT_WRITE) 0000000003010E8F (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC2_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC2_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC3
Address	0000000002011745 (SCOM_DUALPORT_WRITE) 0000000003010E90 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC3_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC3_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC4
Address	0000000002011746 (SCOM_DUALPORT_WRITE) 0000000003010E91 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC4_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC4_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 5*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC5
Address	0000000002011747 (SCOM_DUALPORT_WRITE) 0000000003010E92 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC5_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC5_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b000000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 6*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC6
Address	0000000002011748 (SCOM_DUALPORT_WRITE) 0000000003010E93 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC6_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC6_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance Buffer 3 Data ECC 7*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF3_DATA_ECC7
Address	0000000002011749 (SCOM_DUALPORT_WRITE) 0000000003010E94 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF3_DATA_ECC7_SPARE: Spare
1:8	WO	RO	MAINT_BUFF3_DATA_ECC7_ECC: ECC bits for error inject for ECC mode
9:63	N/A	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Maintenance 65th Byte And 64B ECC Register 0*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC0
Address	000000002201174A (SCOM_DUALPORT_WRITE) 0000000003010E95 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_SPARE_ECC_BITS: Spare ECC bits used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC0_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 1***
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC1
Address	000000000201174B (SCOM_DUALPORT_WRITE) 0000000003010E96 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC1_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 2***
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC2
Address	000000000201174C (SCOM_DUALPORT_WRITE) 0000000003010E97 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC2_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	*Maintenance 65th Byte And 64B ECC Register 3*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC3
Address	000000000201174D (SCOM_DUALPORT_WRITE) 0000000003010E98 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC3_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	*Maintenance 65th Byte And 64B ECC Register 4*
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC4
Address	000000000201174E (SCOM_DUALPORT_WRITE) 0000000003010E99 (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC4_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 5***
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC5
Address	0000000002011740F (SCOM_DUALPORT_WRITE) 0000000003010E9A (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC5_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 6***
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC6
Address	0000000002011750 (SCOM_DUALPORT_WRITE) 0000000003010E9B (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC6_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***Maintenance 65th Byte And 64B ECC Register 7***
Mnemonic	MBU.MBX.MAINT1.MAINT_BUFF_65TH_BYTE_64B_ECC7
Address	0000000002011751 (SCOM_DUALPORT_WRITE) 0000000003010E9C (SCOM_DUALPORT_READ)
Attributes	
Description	

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
0	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_CHECKBIT0_1: Check Bits n=0 Check Bit 0 for 1st 64Bytes of Cache Line n=1 Check Bit 1 for 1st 64Bytes of Cache Line n=2 Check Bit 0 for 2nd 64Bytes of Cache Line n=3 Check Bit 1 for 2nd 64Bytes of Cache Line n=4:7 Unused
1	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_TAG0_2: Tag Bit n=0 Tag 0 for 1st 64Bytes of Cache Line n=1 Tag 2 for 1st 64Bytes of Cache Line n=2 Tag 0 for 2nd 64Bytes of Cache Line n=3 Tag 2 for 2nd 64Bytes of Cache Line n=4:7 Unused

Bits	SCOM_DUALPORT_WRITE	SCOM_DUALPORT_READ	Field Mnemonic: Description
2	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_TAG1_3: Tag Bit n=0 Tag 1 for 1st 64Bytes of Cache Line n=1 Tag 3 for 1st 64Bytes of Cache Line n=2 Tag 1 for 2nd 64Bytes of Cache Line n=3 Tag 3 for 2nd 64Bytes of Cache Line n=4:7 Unused
3	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_MDI: MDI Bit n=0 MDI for 1st 64Bytes of Cache Line n=1 MDI for 1st 64Bytes of Cache Line n=2 MDI for 2nd 64Bytes of Cache Line n=3 MDI for 2nd 64Bytes of Cache Line n=4:7 Unused
4:15	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_ECC_C6_C5_C4: ECC check byte C6_C5_C4 n=0 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 1st 64Bytes of Cache Line n=1 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 1st 64Byte of Cache Line n=2 C6(0:1), C5(0:1), C4(0:1) C6(2:3), C5(2:3) C4(2:3) for 2nd 64Bytes of Cache Line n=3 C6(4:5), C5(4:5), C4(4:5), C6(6:7), C5(6:7), C5(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
16:31	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_ECC_C3_C2_C1_C0: ECC check byte C3_C2_C1_C0 n=0 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 1st 64Bytes of Cache Line n=1 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 1st 64Byte of Cache Line n=2 C3(0:1), C2(0:1), C1(0:1), C0(0:1), C3(2:3), C2(2:3), C1(2:3), C0(2:3) for 2nd 64Bytes of Cache Line n=3 C3(4:5), C2(4:5), C1(4:5), C0(4:5), C3(6:7), C2(6:7), C1(6:7), C0(6:7) for 2nd 64Byte of Cache Line n=4:7 Unused
32:47	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_SPARE_ECC_BITS: Spare Ecc bits Used for future expansion
48:55	WO	RO	MAINT_BUFF_65TH_BYTE_64B_ECC7_FABRIC_ECC: ECC bits for error inject for Fabric ECC
56:63	N/A	RO	constant=0b00000000

Register Name	***MBS Memory Scrub/Read Error Count Register 0***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSEC0Q
Address	0000000002011753 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RWX	MBSEC0Q_SOFT_CE_COUNT: Soft CE Count This is a 12-bit count of soft CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
12:23	RWX	MBSEC0Q_INTERMITTENT_CE_COUNT: Intermittent CE Count This is a 12-bit count of intermittent CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
24:35	RWX	MBSEC0Q_HARD_CE_COUNT: Hard CE Count This is a 12-bit count of hard CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
36:47	RWX	MBSEC0Q_SCE_COUNT: Symbol CE Count This is a 12-bit count of symbol CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
48:59	RWX	MBSEC0Q_MCE_COUNT: Mark CE Count This is a 12-bit count of mark CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
60:63	RO	constant=0b0000

Register Name	***MBS Memory Scrub/Read Error Count Register 1***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSEC1Q
Address	0000000002011754 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RWX	MBSEC1Q_RCE_COUNT: Retry CE Count This is a 12-bit count of retry CE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
12:23	RWX	MBSEC1Q_MPE_COUNT: Mark Place Error Count This is a 12-bit count of mark place error events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
24:35	RWX	MBSEC1Q_UE_COUNT: UE Count This is a 12-bit count of UE events. It contains an 11-bit count value and an overflow bit (MSB). Once the overflow bit is set, it will remain set until the counter is cleared.
36:63	RO	constant=0b00000000000000000000000000

Register Name	***MBS Memory Scrub/Read Error Threshold Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSTRQ
Address	0000000002011755 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBSTRQ_SOFT_CE_COUNT_THRESHOLD_ATTN_STOP: Select Soft CE Count Threshold sets ETE Special Attention stops maint op. When set, ETE special attention is set when Soft_CE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stop s immediately or at the end of the current rank
1	RWX	MBSTRQ_INTERMITTENT_CE_COUNT_THRESHOLD_ATTN_STOP: Select Intermittent CE Count Threshold sets ETE Special Attention stops maint op. When set, ETE special attention is set when Intermittent_CE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stops immediately or at the end of the current rank
2	RWX	MBSTRQ_HARD_CE_COUNT_THRESHOLD_ATTN_STOP: Select Hard CE Count Threshold sets ETE Special Attention stops maint op. When set, ETE special attention is set when Hard_CE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stops immediately or at the end of the current rank
3	RWX	MBSTRQ_RCE_COUNT_THRESHOLD_ATTN_STOP: Select RCE Count Threshold sets ETE Special Attention stops maint op. When set, ETE special attention is set when RCE_Count = Error_Count_Threshold (immediate or end-of-rank). The maint operation also stops immediately or at the end of the current rank
4:15	RWX	MBSTRQ_SOFT_CE_COUNT_THRESHOLD: Soft CE Count Threshold. Compare against the Soft CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
16:27	RWX	MBSTRQ_INTERMITTENT_CE_COUNT_THRESHOLD: Intermittent CE Count Threshold. Compare against the Intermittent CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
28:39	RWX	MBSTRQ_HARD_CE_COUNT_THRESHOLD: Hard CE Count Threshold. Compare against the Hard CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
40:51	RWX	MBSTRQ_RETRY_CE_COUNT_THRESHOLD: Retry CE Count Threshold. Compare against the Retry CE Count Value, causes ETE Attention to be set and maint op to stop, if enabled and stop condition is set
52	RWX	MBSTRQ_RESET_KEEPER: Reset keeper for MBS clock domain

Bits	SCOM	Field Mnemonic: Description
53	RWX	MBSTRQ_RESET_ALL_ERROR_COUNT_REGISTERS: Reset all error count and symbol error count registers Set to clear registers. Hardware will reset this bit to zero after registers are cleared.
54	RWX	MBSTRQ_DISABLE_RESET_ERROR_REG_RANK_END: Disable reset of error count and symbol error count registers at end of rank When set, the se registers will not be reset at the end of a rank. When this bit is reset to zero, the error registers will be reset when the end of a rank is reached and the MBMACA address has incremented to the next valid rank during execution of a multi-address command. Note: The only way to clear the count and syndrome registers is by setting bit 11 above or incrementing the MBMACA address past the end of a rank during a multi-address command. Starting and stopping scrubs will NOT reset these registers.
55	RWX	MBSTRQ_SOFT_CE_INCR_SYMBOL_COUNT: soft ce increment symbol counters When set, a soft CE detected by a readscrub op will increment one of the 72 8-bit a symbol error counters
56	RWX	MBSTRQ_INTERMIT_INCR_SYMBOL_COUNT: intermittent ce increment symbol counters When set, an intermittent CE detected by a readscrub op will increment one of the 72 8-bit symbol error counters
57	RWX	MBSTRQ_HARD_CE_INCR_SYMBOL_COUNT: Hard ce increment symbol counters When set, a hard CE detected by a readscrub op will increment one of the 72 8-bit a symbol error counters
58	RWX	MBSTRQ_MCE_INCR_SYMBOL_COUNT: MCE increment symbol count (but would need to split out failed symbol info from chip mark....TBD, extra credit)
59	RWX	MBSTRQ_UE_TRAP: Trap data only with UEs enabled When set, only read data with UEs will be saved in the Maint buffers. When not set, all data from a read will be saved into the Maint buffers regardless if it had an error or not.
60:61	RWX	MBSTRQ_RESERVED_60_61: Reserved
62	RWX	MBSTRQ_INTERMITTENT_NCE_INJECT: Intermittent NCE Inject not implemented This logic has been removed and replaced with the error injector in the ECC macro.
63	RWX	MBSTRQ_RESERVED_63: Reserved

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 0***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC0Q
Address	0000000002011756 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC0Q_SYMBOL_0_ERROR_COUNT: Symbol 0 error count
8:15	RWX	MBSSYMEC0Q_SYMBOL_1_ERROR_COUNT: Symbol 1 error count
16:23	RWX	MBSSYMEC0Q_SYMBOL_2_ERROR_COUNT: Symbol 2 error count
24:31	RWX	MBSSYMEC0Q_SYMBOL_3_ERROR_COUNT: Symbol 3 error count
32:39	RWX	MBSSYMEC0Q_SYMBOL_4_ERROR_COUNT: Symbol 4 error count
40:47	RWX	MBSSYMEC0Q_SYMBOL_5_ERROR_COUNT: Symbol 5 error count
48:55	RWX	MBSSYMEC0Q_SYMBOL_6_ERROR_COUNT: Symbol 6 error count
56:63	RWX	MBSSYMEC0Q_SYMBOL_7_ERROR_COUNT: Symbol 7 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 1*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC1Q
Address	0000000002011757 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC1Q_SYMBOL_8_ERROR_COUNT: Symbol 8 error count
8:15	RWX	MBSSYMEC1Q_SYMBOL_9_ERROR_COUNT: Symbol 9 error count
16:23	RWX	MBSSYMEC1Q_SYMBOL_10_ERROR_COUNT: Symbol 10 error count
24:31	RWX	MBSSYMEC1Q_SYMBOL_11_ERROR_COUNT: Symbol 11 error count
32:39	RWX	MBSSYMEC1Q_SYMBOL_12_ERROR_COUNT: Symbol 12 error count
40:47	RWX	MBSSYMEC1Q_SYMBOL_13_ERROR_COUNT: Symbol 13 error count
48:55	RWX	MBSSYMEC1Q_SYMBOL_14_ERROR_COUNT: Symbol 14 error count
56:63	RWX	MBSSYMEC1Q_SYMBOL_15_ERROR_COUNT: Symbol 15 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 2*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC2Q
Address	0000000002011758 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC2Q_SYMBOL_16_ERROR_COUNT: Symbol 16 error count
8:15	RWX	MBSSYMEC2Q_SYMBOL_17_ERROR_COUNT: Symbol 17 error count
16:23	RWX	MBSSYMEC2Q_SYMBOL_18_ERROR_COUNT: Symbol 18 error count
24:31	RWX	MBSSYMEC2Q_SYMBOL_19_ERROR_COUNT: Symbol 19 error count
32:39	RWX	MBSSYMEC2Q_SYMBOL_20_ERROR_COUNT: Symbol 20 error count
40:47	RWX	MBSSYMEC2Q_SYMBOL_21_ERROR_COUNT: Symbol 21 error count
48:55	RWX	MBSSYMEC2Q_SYMBOL_22_ERROR_COUNT: Symbol 22 error count
56:63	RWX	MBSSYMEC2Q_SYMBOL_23_ERROR_COUNT: Symbol 23 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 3*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC3Q
Address	0000000002011759 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC3Q_SYMBOL_24_ERROR_COUNT: Symbol 24 error count
8:15	RWX	MBSSYMEC3Q_SYMBOL_25_ERROR_COUNT: Symbol 25 error count

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	MBSSYMEC3Q_SYMBOL_26_ERROR_COUNT: Symbol 26 error count
24:31	RWX	MBSSYMEC3Q_SYMBOL_27_ERROR_COUNT: Symbol 27 error count
32:39	RWX	MBSSYMEC3Q_SYMBOL_28_ERROR_COUNT: Symbol 28 error count
40:47	RWX	MBSSYMEC3Q_SYMBOL_29_ERROR_COUNT: Symbol 29 error count
48:55	RWX	MBSSYMEC3Q_SYMBOL_30_ERROR_COUNT: Symbol 30 error count
56:63	RWX	MBSSYMEC3Q_SYMBOL_31_ERROR_COUNT: Symbol 31 error count

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 4***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC4Q
Address	000000000201175A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC4Q_SYMBOL_32_ERROR_COUNT: Symbol 32 error count
8:15	RWX	MBSSYMEC4Q_SYMBOL_33_ERROR_COUNT: Symbol 33 error count
16:23	RWX	MBSSYMEC4Q_SYMBOL_34_ERROR_COUNT: Symbol 34 error count
24:31	RWX	MBSSYMEC4Q_SYMBOL_35_ERROR_COUNT: Symbol 35 error count
32:39	RWX	MBSSYMEC4Q_SYMBOL_36_ERROR_COUNT: Symbol 36 error count
40:47	RWX	MBSSYMEC4Q_SYMBOL_37_ERROR_COUNT: Symbol 37 error count
48:55	RWX	MBSSYMEC4Q_SYMBOL_38ERROR_COUNT: Symbol 38error count
56:63	RWX	MBSSYMEC4Q_SYMBOL_39_ERROR_COUNT: Symbol 39 error count

Register Name	***MBS Memory Scrub/Read Symbol Error Count Registers 5***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC5Q
Address	000000000201175B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC5Q_SYMBOL_40_ERROR_COUNT: Symbol 40 error count
8:15	RWX	MBSSYMEC5Q_SYMBOL_41_ERROR_COUNT: Symbol 41 error count
16:23	RWX	MBSSYMEC5Q_SYMBOL_42_ERROR_COUNT: Symbol 42 error count
24:31	RWX	MBSSYMEC5Q_SYMBOL_43_ERROR_COUNT: Symbol 43 error count
32:39	RWX	MBSSYMEC5Q_SYMBOL_44_ERROR_COUNT: Symbol 44 error count
40:47	RWX	MBSSYMEC5Q_SYMBOL_45_ERROR_COUNT: Symbol 45 error count
48:55	RWX	MBSSYMEC5Q_SYMBOL_46_ERROR_COUNT: Symbol 46 error count
56:63	RWX	MBSSYMEC5Q_SYMBOL_47_ERROR_COUNT: Symbol 47 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 6*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC6Q
Address	000000000201175C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC6Q_SYMBOL_48_ERROR_COUNT: Symbol 48 error count
8:15	RWX	MBSSYMEC6Q_SYMBOL_49_ERROR_COUNT: Symbol 49 error count
16:23	RWX	MBSSYMEC6Q_SYMBOL_50_ERROR_COUNT: Symbol 50 error count
24:31	RWX	MBSSYMEC6Q_SYMBOL_51_ERROR_COUNT: Symbol 51 error count
32:39	RWX	MBSSYMEC6Q_SYMBOL_52_ERROR_COUNT: Symbol 52 error count
40:47	RWX	MBSSYMEC6Q_SYMBOL_53_ERROR_COUNT: Symbol 53 error count
48:55	RWX	MBSSYMEC6Q_SYMBOL_54_ERROR_COUNT: Symbol 54 error count
56:63	RWX	MBSSYMEC6Q_SYMBOL_55_ERROR_COUNT: Symbol 55 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 7*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC7Q
Address	000000000201175D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC7Q_SYMBOL_56_ERROR_COUNT: Symbol 56 error count
8:15	RWX	MBSSYMEC7Q_SYMBOL_57_ERROR_COUNT: Symbol 57 error count
16:23	RWX	MBSSYMEC7Q_SYMBOL_58_ERROR_COUNT: Symbol 58 error count
24:31	RWX	MBSSYMEC7Q_SYMBOL_59_ERROR_COUNT: Symbol 59 error count
32:39	RWX	MBSSYMEC7Q_SYMBOL_60_ERROR_COUNT: Symbol 60 error count
40:47	RWX	MBSSYMEC7Q_SYMBOL_61_ERROR_COUNT: Symbol 61 error count
48:55	RWX	MBSSYMEC7Q_SYMBOL_62_ERROR_COUNT: Symbol 62 error count
56:63	RWX	MBSSYMEC7Q_SYMBOL_63_ERROR_COUNT: Symbol 63 error count

Register Name	*MBS Memory Scrub/Read Symbol Error Count Registers 8*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSSYMEC8Q
Address	000000000201175E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	MBSSYMEC8Q_SYMBOL_64_ERROR_COUNT: Symbol 64 error count
8:15	RWX	MBSSYMEC8Q_SYMBOL_65_ERROR_COUNT: Symbol 65 error count

Bits	SCOM	Field Mnemonic: Description
16:23	RWX	MBSSYMEC8Q_SYMBOL_66_ERROR_COUNT: Symbol 66 error count
24:31	RWX	MBSSYMEC8Q_SYMBOL_67_ERROR_COUNT: Symbol 67 error count
32:39	RWX	MBSSYMEC8Q_SYMBOL_68_ERROR_COUNT: Symbol 68 error count
40:47	RWX	MBSSYMEC8Q_SYMBOL_69_ERROR_COUNT: Symbol 69 error count
48:55	RWX	MBSSYMEC8Q_SYMBOL_70_ERROR_COUNT: Symbol 70 error count
56:63	RWX	MBSSYMEC8Q_SYMBOL_71_ERROR_COUNT: Symbol 71 error count

Register Name	***MBS Memory Error Vector Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBSEVRQ
Address	000000000201175F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RWX	MBSEVRQ_ERR_VECTOR0: Error Vector 0 This is the 56-bit error vector associated with the last memory error detected. 0:7 - E1 8:15 - E2 16:23 - E3 24:31 - E4 32:39 - E 40:47 - R 48:55 - Error Mask E1 is the error magnitude for the symbol pointed to by the mark x1 E2 is the error magnitude for the symbol pointed to by the mark x2 E3 is the error magnitude for the symbol pointed to by the mark x3 E4 is the error magnitude for the symbol pointed to by the mark x4 E is the error magnitude for a NEW error (associated with NCE) R is the error location, coded as a Galois Field index, for the new error (associated with NCE) Error Mask is the 8bit xor mask that indicates which bits in the corrected symbol were flipped in order to the correct the SCE
56:63	RO	constant=0b00000000

Register Name	***MBS Memory NCE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBNCERQ
Address	0000000002011760 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBNCERQ_RD_NCE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBNCERQ_RD_NCE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBNCERQ_RD_NCE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBNCERQ_RD_NCE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBNCERQ_RD_NCE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40	RWX	MBNCERQ_RD_NCE_ERR_OCCURRED__AFTER_UE_RETRY: If set, this error occurred after a retry for a memory read UE
41:63	RO	constant=0b00000000000000000000000

Register Name	***MBS Memory RCE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBRCERQ
Address	0000000002011761 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBRCERQ_RD_RCE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBRCERQ_RD_RCE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBRCERQ_RD_RCE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBRCERQ_RD_RCE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBRCERQ_RD_RCE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40	RWX	MBRCERQ_RD_RCE_ERR_OCCURRED_AFTER_UE_RETRY: If set, this error occurred after a retry for a memory read UE
41:63	RO	constant=0b00000000000000000000000

Register Name	***MBS Memory MPE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBMPERQ
Address	0000000002011762 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBMPERQ_RD_MPE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBMPERQ_RD_MPE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBMPERQ_RD_MPE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBMPERQ_RD_MPE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBMPERQ_RD_MPE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40	RWX	MBMPERQ_RD_MPE_ERR_OCCURRED_AFTER_UE_RETRY: If set, this error occurred after a retry for a memory read UE
41:63	RO	constant=0b00000000000000000000000

Register Name	***MBS Memory UE Error Address Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBUERQ
Address	0000000002011763 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBUERQ_RD_UE_MASTER_RANK: Master Rank Master rank address for memory operations. For memory buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBUERQ_RD_UE_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBUERQ_RD_UE_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBUERQ_RD_UE_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBUERQ_RD_UE_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40:41	RWX	MBUERQ_RESERVED_40_41: RESERVED
42:63	RO	constant=0b00000000000000000000

Register Name	***Port A Error Counter 1***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCB_ERRCNTA1Q
Address	0000000002011764 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR0: Nibble 0 Error Counter
7:13	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR1: Nibble 1 Error Counter
14:20	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR2: Nibble 2 Error Counter
21:27	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR3: Nibble 3 Error Counter
28:34	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR4: Nibble 4 Error Counter
35:41	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR5: Nibble 5 Error Counter
42:48	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR6: Nibble 6 Error Counter
49:55	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR7: Nibble 7 Error Counter
56:62	RWX	MCB_ERRCNTA1Q_NIBBLE_ERR_PORTA_CNTR8: Nibble 8 Error Counter
63	RWX	MCB_ERRCNTA1Q_RESERVED_63: RESERVED

Register Name	*Port A Error Counter 2*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCB_ERRCNTA2Q
Address	0000000002011765 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR9: Nibble 9 Error Counter
7:13	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR10: Nibble 10 Error Counter
14:20	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR11: Nibble 11 Error Counter
21:27	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR12: Nibble 12 Error Counter
28:34	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR13: Nibble 13 Error Counter
35:41	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR14: Nibble 14 Error Counter
42:48	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR15: Nibble 15 Error Counter
49:55	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR16: Nibble 16 Error Counter
56:62	RWX	MCB_ERRCNTA2Q_NIBBLE_ERR_PORTA_CNTR17: Nibble 17 Error Counter
63	RWX	MCB_ERRCNTA2Q_ERR_CNTR_OVERFLOW: Error Counter Overflow

Register Name	*Port A Error Counter 3*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCB_ERRCNTA3Q
Address	0000000002011766 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTA3Q_NIBBLE_ERR_PORTA_CNTR18: Nibble 18 Error Counter
7:13	RWX	MCB_ERRCNTA3Q_NIBBLE_ERR_PORTA_CNTR19: Nibble 19 Error Counter
14:63	RWX	MCB_ERRCNTA3Q_RESERVED_14_63: RESERVED

Register Name	*Port B Error Counter 1*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCB_ERRCNTB1Q
Address	0000000002011767 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR0: Nibble 0 Error Counter
7:13	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR1: Nibble 1 Error Counter
14:20	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR2: Nibble 2 Error Counter
21:27	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR3: Nibble 3 Error Counter
28:34	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR4: Nibble 4 Error Counter

Bits	SCOM	Field Mnemonic: Description
35:41	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR5: Nibble 5 Error Counter
42:48	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR6: Nibble 6 Error Counter
49:55	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR7: Nibble 7 Error Counter
56:62	RWX	MCB_ERRCNTB1Q_NIBBLE_ERR_PORTB_CNTR8: Nibble 8 Error Counter
63	RWX	MCB_ERRCNTB1Q_RESERVED_63: RESERVED

Register Name	*Port B Error Counter 2*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCB_ERRCNTB2Q
Address	0000000002011768 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR9: Nibble 9 Error Counter
7:13	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR10: Nibble 10 Error Counter
14:20	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR11: Nibble 11 Error Counter
21:27	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR12: Nibble 12 Error Counter
28:34	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR13: Nibble 13 Error Counter
35:41	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR14: Nibble 14 Error Counter
42:48	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR15: Nibble 15 Error Counter
49:55	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR16: Nibble 16 Error Counter
56:62	RWX	MCB_ERRCNTB2Q_NIBBLE_ERR_PORTB_CNTR17: Nibble 17 Error Counter
63	RWX	MCB_ERRCNTB2Q_ERR_CNTR_OVERFLOW: Error Counter Overflow

Register Name	*Port B Error Counter 3*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCB_ERRCNTB3Q
Address	0000000002011769 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RWX	MCB_ERRCNTB3Q_NIBBLE_ERR_PORTB_CNTR18: Nibble 18 Error Counter
7:13	RWX	MCB_ERRCNTB3Q_NIBBLE_ERR_PORTB_CNTR19: Nibble 19 Error Counter
14:63	RWX	MCB_ERRCNTB3Q_RESERVED_14_63: RESERVED

Register Name	*Port A Error Map Register 1*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBEMA1Q
Address	000000000201176A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMA1Q_ERROR_MAP_PORTA_RNK0: Rank 0 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMA1Q_ERROR_MAP_PORTA_RNK1: Rank 1 Error Map
40:59	RWX	MCBEMA1Q_ERROR_MAP_PORTA_RNK2: Rank 2 Error Map
60:63	RWX	MCBEMA1Q_RESERVED_60_63: RESERVED

Register Name	***Port A Error Map Register 2***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBEMA2Q
Address	000000000201176B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMA2Q_ERROR_MAP_PORTA_RNK3: Rank 3 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMA2Q_ERROR_MAP_PORTA_RNK4: Rank 4 Error Map
40:59	RWX	MCBEMA2Q_ERROR_MAP_PORTA_RNK5: Rank 5 Error Map
60:63	RWX	MCBEMA2Q_RESERVED_60_63: RESERVED

Register Name	***Port A Error Map Register 3***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBEMA3Q
Address	000000000201176C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMA3Q_ERROR_MAP_PORTA_RNK6: Rank 6 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMA3Q_ERROR_MAP_PORTA_RNK7: Rank 7 Error Map
40:63	RWX	MCBEMA3Q_RESERVED_40_63: RESERVED

Register Name	***Port B Error Map Register 1***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBEMB1Q
Address	000000000201176D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMB1Q_ERROR_MAP_PORTB_RNK0: Rank 0 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMB1Q_ERROR_MAP_PORTB_RNK1: Rank 1 Error Map
40:59	RWX	MCBEMB1Q_ERROR_MAP_PORTB_RNK2: Rank 2 Error Map
60:63	RWX	MCBEMB1Q_RESERVED_60_63: RESERVED

Register Name	***Port B Error Map Register 2***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBEMB2Q
Address	000000000201176E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMB2Q_ERROR_MAP_PORTB_RNK3: Rank 3 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMB2Q_ERROR_MAP_PORTB_RNK4: Rank 4 Error Map
40:59	RWX	MCBEMB2Q_ERROR_MAP_PORTB_RNK5: Rank 5 Error Map
60:63	RWX	MCBEMB2Q_RESERVED_60_63: RESERVED

Register Name	***Port B Error Map Register 3***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBEMB3Q
Address	000000000201176F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	RWX	MCBEMB3Q_ERROR_MAP_PORTB_RNK6: Rank 6 Error Map In x4 Mode: In x8 Mode: Bit 0 - DRAM 0 fail Bit 0 - DRAM 0 Nibble 0 fail Bit 1 - DRAM 1 fail Bit 1 - DRAM 0 Nibble 1 fail Bit 2 - DRAM 2 fail Bit 2 - DRAM 1 Nibble 0 fail Bit 3 - DRAM 3 fail Bit 3 - DRAM 1 Nibble 1 fail Bit 4 - DRAM 4 fail Bit 4 - DRAM 2 Nibble 0 fail Bit 5 - DRAM 5 fail Bit 5 - DRAM 2 Nibble 1 fail Bit 6 - DRAM 6 fail Bit 6 - DRAM 3 Nibble 0 fail Bit 7 - DRAM 7 fail Bit 7 - DRAM 3 Nibble 1 fail Bit 8 - DRAM 8 fail Bit 8 - DRAM 4 Nibble 0 fail Bit 9 - DRAM 9 fail Bit 9 - DRAM 4 Nibble 1 fail Bit 10 - DRAM 10 fail Bit 10 - DRAM 5 Nibble 0 fail Bit 11 - DRAM 11 fail Bit 11 - DRAM 5 Nibble 1 fail Bit 12 - DRAM 12 fail Bit 12 - DRAM 6 Nibble 0 fail Bit 13 - DRAM 13 fail Bit 13 - DRAM 6 Nibble 1 fail Bit 14 - DRAM 14 fail Bit 14 - DRAM 7 Nibble 0 fail Bit 15 - DRAM 15 fail Bit 15 - DRAM 7 Nibble 1 fail Bit 16 - DRAM 16 fail Bit 16 - DRAM 8 Nibble 0 fail Bit 17 - DRAM 17 fail Bit 17 - DRAM 8 Nibble 1 fail Bit 18 - DRAM 18 fail Bit 18 - DRAM 9 Nibble 0 fail Bit 19 - DRAM 19 fail Bit 19 - DRAM 9 Nibble 1 fail
20:39	RWX	MCBEMB3Q_ERROR_MAP_PORTB_RNK7: Rank 7 Error Map
40:63	RWX	MCBEMB3Q_RESERVED_40_63: RESERVED

Register Name	***Port A Error Map And Status Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBSTATAQ
Address	0000000002011770 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MCBSTATAQ_PORTA_CE_ERR: CE Detected (ECC Mode only) 0 - No CE Detected 1 - CE Detected
1	ROX	MCBSTATAQ_PORTA_UE_ERR: UE Detected (ECC Mode only) 0 - No UE Detected 1 - UE Detected
2	ROX	MCBSTATAQ_PORTA_ERR_TRAP_OVERFLOW: Error Trap Overflow for both Port A and B 0 - 8 or less errors have been detected on both port A and B 1 - More than 8 errors have been detected on both port A and B
3:7	ROX	MCBSTATAQ_PORTA_CNTL_TRAP_SUBTST_NUM: Subtest Pointer

Bits	SCOM	Field Mnemonic: Description
8:10	ROX	MCBSTATAQ_PORTA_ERR_LOG_PTR: Error Log Pointer - In MCB mode the pointer points to the address where the next error will be stored. That is, the last error was written to (Error Log Pointer -1)
11:23	ROX	MCBSTATAQ_RESERVED_11_23: RESERVED
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***Port B Error Map And Status Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBSTATBQ
Address	0000000002011771 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MCBSTATBQ_PORTB_CE_ERR: CE Detected (ECC Mode only) 0 - No CE Detected 1 - CE Detected
1	ROX	MCBSTATBQ_PORTB_UE_ERR: UE Detected (ECC Mode only) 0 - No UE Detected 1 - UE Detected
2	ROX	MCBSTATBQ_PORTB_ERR_TRAP_OVERFLOW: Error Trap Overflow for both Port A and B 0 - 8 or less errors have been detected on both port A and B 1 - More than 8 errors have been detected on both port A and B
3:7	ROX	MCBSTATBQ_PORTB_CNTL_TRAP_SUBTST_NUM: Subtest Pointer
8:10	ROX	MCBSTATBQ_PORTB_ERR_LOG_PTR: Error Log Pointer - In MCB mode the pointer points to the address where the next error will be stored. That is, the last error was written to (Error Log Pointer -1)
11:23	ROX	MCBSTATBQ_RESERVED_11_23: RESERVED
24:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***Port A Compare Mask Register 1***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBCMA1Q
Address	0000000002011772 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBCMA1Q_COMPARE_MASK_A: Port A Compare Mask (0:63)

Register Name	***Port B Compare Mask Register 1***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBCMB1Q
Address	0000000002011773 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBCMB1Q_COMPARE_MASK_B: Port B Compare Mask (0:63)

Register Name	***Port A & B Compare Mask Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MCBCMABQ
Address	0000000002011774 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MCBCMABQ_COMPARE_MASK_A: Port A Compare Mask (64:79)
16:31	RW	MCBCMABQ_COMPARE_MASK_B: Port B Compare Mask (64:79)
32	RW	MCBCMABQ_CFG_STORE_FAIL: Cfg_store_fail 0 - store first 8 fails 1 - store last 8 fails
33	RW	MCBIST_ENABLE_CE_TRAP: Enable CE to be trapped in MCBIST ECC Mode 0 - disable trapping 1 - enable trapping
34	RW	MCBIST_ENABLE_MPE_TRAP: Enable MPE to be trapped in MCBIST ECC Mode 0 - disable trapping 1 - enable trapping
35	RW	MCBCMABQ_ENABLE_UE_TRAP: Enable UE to be trapped in MCBIST ECC Mode 0 - disable trapping 1 - enable trapping
36	RW	MCBIST_STOP_ON_NTH_FAIL: Stop on subtest when nth fail is detected. MCBCFGQ(62) turns on the stop on error. If that bit is not set, this register is a don;t care. Values: STOP_AT_THE_END_OF_A_SUSBTEST_WHEN_1_OR_MORE_FAILS_IS_DETECTED=>0b0 STOP_AT_THE_END_OF_A_SUSBTEST_WHEN_8_OR_MORE_FAILS_IS_DETECTED=>0b1
37	RW	MCBCMABQ_ARRAY_READ_ENABLE: Array SCOM Read Enable Values: DISABLE_SCOM_READS_TO_SRB_AND_PF_BUFFERS=>0b0 ENABLES_SCOM_READS_TO_SRB_AND_PF_BUFFERS=>0b1
38:63	RW	MCBCMABQ_RESERVED_38_63: RESERVED

Register Name	***MBS Random Data Seed 0 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS0Q
Address	0000000002011775 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS0Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 1 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS1Q
Address	0000000002011776 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS1Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 2 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS2Q
Address	0000000002011777 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS2Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 3 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS3Q
Address	0000000002011778 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS3Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 4 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS4Q
Address	0000000002011779 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS4Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***MBS Random Data Seed 5 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS5Q
Address	000000000201177A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS5Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 6 Register*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS6Q
Address	000000000201177B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS6Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 7 Register*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS7Q
Address	000000000201177C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MBS_MCBRDS7Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*MBS Random Data Seed 8 Register*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDS8Q
Address	000000000201177D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED0: DQ(8) Burst 1 Random Data Seed
8:15	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED1: DQ(8) Burst 2 Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED2: DQ(8) Burst 3 Random Data Seed
24:31	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED3: DQ(8) Burst 4 Random Data Seed
32:39	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED4: DQ(8) Burst 5 Random Data Seed
40:47	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED5: DQ(8) Burst 6 Random Data Seed
48:55	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED6: DQ(8) Burst 7 Random Data Seed
56:63	RW	MBS_MCBRDS8Q_DGEN_RNDD_SEED7: DQ(8) Burst 8 Random Data Seed

Register Name	***MBS Random Data Seed Spare Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBRDSSPQ
Address	000000000201177E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED0: DQ(9) Burst 1 Random Data Seed
8:15	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED1: DQ(9) Burst 2 Random Data Seed
16:23	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED2: DQ(9) Burst 3 Random Data Seed
24:31	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED3: DQ(9) Burst 4 Random Data Seed
32:39	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED4: DQ(9) Burst 5 Random Data Seed
40:47	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED5: DQ(9) Burst 6 Random Data Seed
48:55	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED6: DQ(9) Burst 7 Random Data Seed
56:63	RW	MBS_MCBRDSSPQ_DGEN_RNDD_SEED7: DQ(9) Burst 8 Random Data Seed

Register Name	***MBS Data Rotate Seed Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBDRSRQ
Address	000000000201177F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBDRSRQ_CFG_DATA_ROT_SEED: Bits 0:63 of the Data Rotate Seed

Register Name	***Data Rotate Configuration Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBDRCRQ
Address	0000000002011780 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBS_MCBDRCRQ_CFG_DATA_ROT: Bits to shift: Values: ROTATE_1_BIT=>0b0001 ROTATE_2_BITS=>0b0010 ROTATE_3_BITS=>0b0011 ROTATE_4_BITS=>0b0100 ROTATE_5_BITS=>0b0101 ROTATE_6_BITS=>0b0110 ROTATE_7_BITS=>0b0111 ROTATE_8_BITS=>0b1000 ROTATE_9_BITS=>0b1001 ROTATE_10_BITS=>0b1010 ROTATE_11_BITS=>0b1011 ROTATE_12_BITS=>0b1100 ROTATE_13_BITS=>0b1101 ROTATE_14_BITS=>0b1110 ROTATE_15_BITS=>0b1111
4:19	RW	MBS_MCBDRCRQ_CFG_DATA_ROT_SEED: Bits 64:79 of the Data Rotate Seed
20	RW	MBS_MCBDRCRQ_CFG_INVERT_DATA: These bits control the final inversion of data over to the xpt. Bit 20 = Invert MA Data
21:63	RW	MBS_MCBDRCRQ_RESERVED_21_63: Not used

Register Name	***MBS Fixed Data Seed Burst 0 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD0Q
Address	0000000002011781 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD0Q_CFG_FIXED_SEED: Fixed Data Seed(0:63)

Register Name	***MBS Fixed Data Seed Burst 1 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD1Q
Address	0000000002011782 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD1Q_CFG_FIXED_SEED: Fixed Data Seed(72:135)

Register Name	***MBS Fixed Data Seed Burst 2 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD2Q
Address	0000000002011783 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD2Q_CFG_FIXED_SEED: Fixed Data Seed(144:207)

Register Name	***MBS Fixed Data Seed Burst 3 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD3Q
Address	0000000002011784 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD3Q_CFG_FIXED_SEED: Fixed Data Seed(216:279)

Register Name	***MBS Fixed Data Seed Burst 4 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD4Q
Address	0000000002011785 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD4Q_CFG_FIXED_SEED: Fixed Data Seed(288:351)

Register Name	***MBS Fixed Data Seed Burst 5 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD5Q
Address	0000000002011786 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD5Q_CFG_FIXED_SEED: Fixed Data Seed(360:423)

Register Name	***MBS Fixed Data Seed Burst 6 Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD6Q
Address	0000000002011787 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD6Q_CFG_FIXED_SEED: Fixed Data Seed(432:495)

Register Name	*MBS Fixed Data Seed Burst 7 Register*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFD7Q
Address	0000000002011788 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MBS_MCBFD7Q_CFG_FIXED_SEED: Fixed Data Seed(504:567)

Register Name	*MBS Fixed Data Seed Register*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFDQ
Address	0000000002011789 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBFDQ_CFG_FIXED_SEED1: DQ(8) Burst 1 Fixed Data Seed(64:71)
8:15	RW	MBS_MCBFDQ_CFG_FIXED_SEED2: DQ(8) Burst 2 Fixed Data Seed(136:143)
16:23	RW	MBS_MCBFDQ_CFG_FIXED_SEED3: DQ(8) Burst 3 Fixed Data Seed(208:215)
24:31	RW	MBS_MCBFDQ_CFG_FIXED_SEED4: DQ(8) Burst 4 Fixed Data Seed(280:287)
32:39	RW	MBS_MCBFDQ_CFG_FIXED_SEED5: DQ(8) Burst 5 Fixed Data Seed(352:359)
40:47	RW	MBS_MCBFDQ_CFG_FIXED_SEED6: DQ(8) Burst 6 Fixed Data Seed(424:431)
48:55	RW	MBS_MCBFDQ_CFG_FIXED_SEED7: DQ(8) Burst 7 Fixed Data Seed(496:503)
56:63	RW	MBS_MCBFDQ_CFG_FIXED_SEED8: DQ(8) Burst 8 Fixed Data Seed(568:575)

Register Name	*MBS Fixed Data Seed Spare Register*
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBS_MCBFDSPQ
Address	000000000201178A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED1: DQ(9) Burst 1 Fixed Data Seed(64:71)
8:15	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED2: DQ(9) Burst 2 Fixed Data Seed(136:143)
16:23	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED3: DQ(9) Burst 3 Fixed Data Seed(208:215)
24:31	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED4: DQ(9) Burst 4 Fixed Data Seed(280:287)
32:39	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED5: DQ(9) Burst 5 Fixed Data Seed(352:359)
40:47	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED6: DQ(9) Burst 6 Fixed Data Seed(424:431)
48:55	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED7: DQ(9) Burst 7 Fixed Data Seed(496:503)
56:63	RW	MBS_MCBFDSPQ_CFG_FIXED_SEED8: DQ(9) Burst 8 Fixed Data Seed(568:575)

Register Name	***MBX Error Status Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBXERRSTATQ
Address	000000000201178F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBXERRSTATQ_WDONE_PAR_ERROR: Parity Error in the wdone IF linked to MBSFIR bit 1
1	ROX	MBXERRSTATQ_RDTAG_RDCHECK_ERROR: Parity Error in the Read Sequence IF linked to MBSFIR bit 1
2	ROX	MBXERRSTATQ_RDTAG_PAR_ERROR: Parity Error in the rdtag IF linked to MBSFIR bit 1
3	ROX	MBXERRSTATQ_RDTAG_PAR_RC_ERROR: Parity Error in the rdtag RowColumn IF linked to MBSFIR bit 1
4:63	ROX	MBXERRSTATQ_RESERVED_4_63: RESERVED

Register Name	***MBX Error Injection Register***
Mnemonic	MBU.MBS.MCBISTS23.SCOMFIR.MBXERRINJQ
Address	0000000002011790 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBXERRINJQ_RCMD_ERR_INJ_MODE: Parity Error inject mode into the RCMD array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
1	RW	MBXERRINJQ_RCMD_ERR_INJ: Parity Error inject into the RCMD array
2	RW	MBXERRINJQ_WRD_CE_ERR_INJ_MODE: CE Error inject mode into the WRD array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	MBXERRINJQ_WRD_CE_ERR_INJ: CE Error inject into the WRD array
4	RW	MBXERRINJQ_WRD_UE_ERR_INJ_MODE: UE Error inject mode into the WRD array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
5	RW	MBXERRINJQ_WRD_UE_ERR_INJ: UE Error inject into the WRD array
6	RW	MBXERRINJQ_MAINT_CE_ERR_INJ_MODE: CE Error inject mode into the Maint array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
7	RW	MBXERRINJQ_MAINT_CE_ERR_INJ: CE Error inject into the Maint array
8	RW	MBXERRINJQ_MAINT_UE_ERR_INJ_MODE: UE Error inject mode into the Maint array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
9	RW	MBXERRINJQ_MAINT_UE_ERR_INJ: UE Error inject into the Maint array

Bits	SCOM	Field Mnemonic: Description
10	RW	MBXERRINJQ_SCOM_PE_ERR_INJ_MODE: SCOM Parity Error inject mode Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
11	RW	MBXERRINJQ_SCOM_PE_ERR_INJ: SCOM Parity Error inject
12:63	RW	MBXERRINJQ_RESERVED_12_63: RESERVED

Register Name	***MBS23 PFB Buffer 0 Data 0***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA0
Address	0000000002011791 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA0_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 1***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA1
Address	0000000002011792 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA1_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 2***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA2
Address	0000000002011793 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA2_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 3***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA3
Address	0000000002011794 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA3_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 4***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA4
Address	0000000002011795 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA4_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 5***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA5
Address	0000000002011796 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA5_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 6***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA6
Address	0000000002011797 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA6_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 0 Data 7***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF0_DATA7
Address	0000000002011798 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF0_DATA7_MBS23_PFB_BUFF0_DATA: PFB Buffer0 Data

Register Name	***MBS23 PFB Buffer 1 Data 0***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA0
Address	0000000002011799 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA0_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 1***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA1
Address	000000000201179A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA1_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 2***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA2
Address	000000000201179B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA2_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 3***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA3
Address	000000000201179C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA3_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 4***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA4
Address	000000000201179D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA4_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 5***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA5
Address	000000000201179E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA5_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 6***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA6
Address	000000000201179F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA6_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 1 Data 7***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF1_DATA7
Address	000000000020117A0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF1_DATA7_MBS23_PFB_BUFF1_DATA: PFB Buffer1 Data

Register Name	***MBS23 PFB Buffer 2 Data 0***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA0
Address	00000000020117A1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA0_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 1***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA1
Address	00000000020117A2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA1_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 2***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA2
Address	00000000020117A3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA2_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 3***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA3
Address	00000000020117A4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA3_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 4***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA4
Address	00000000020117A5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA4_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 5***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA5
Address	00000000020117A6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA5_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 6***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA6
Address	00000000020117A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA6_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 2 Data 7***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF2_DATA7
Address	00000000020117A8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF2_DATA7_MBS23_PFB_BUFF2_DATA: PFB Buffer2 Data

Register Name	***MBS23 PFB Buffer 3 Data 0***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA0
Address	00000000020117A9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA0_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 1***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA1
Address	00000000020117AA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA1_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 2***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA2
Address	00000000020117AB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA2_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 3***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA3
Address	00000000020117AC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA3_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 4***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA4
Address	00000000020117AD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA4_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 5***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA5
Address	00000000020117AE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA5_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 6***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA6
Address	00000000020117AF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA6_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 PFB Buffer 3 Data 7***
Mnemonic	MBU.MBS.PFB.MBS23_PFB_BUFF3_DATA7
Address	00000000020117B0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_PFB_BUFF3_DATA7_MBS23_PFB_BUFF3_DATA: PFB Buffer3 Data

Register Name	***MBS23 SRB Buffer 0 Data 0***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA0
Address	00000000020117B1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA0_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 1***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA1
Address	00000000020117B2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA1_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 2***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA2
Address	00000000020117B3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA2_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 3***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA3
Address	00000000020117B4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA3_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 4***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA4
Address	00000000020117B5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA4_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 5***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA5
Address	00000000020117B6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA5_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 6***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA6
Address	00000000020117B7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA6_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 0 Data 7***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF0_DATA7
Address	00000000020117B8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF0_DATA7_MBS23_SRB_BUFF0_DATA: SRB Buffer0 Data

Register Name	***MBS23 SRB Buffer 1 Data 0***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA0
Address	00000000020117B9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA0_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 1***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA1
Address	00000000020117BA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA1_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 2***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA2
Address	00000000020117BB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA2_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 3***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA3
Address	00000000020117BC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA3_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 4***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA4
Address	00000000020117BD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA4_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 5***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA5
Address	00000000020117BE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA5_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 6***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA6
Address	00000000020117BF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA6_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 1 Data 7***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF1_DATA7
Address	00000000020117C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF1_DATA7_MBS23_SRB_BUFF1_DATA: SRB Buffer1 Data

Register Name	***MBS23 SRB Buffer 2 Data 0***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA0
Address	00000000020117C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA0_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 1***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA1
Address	00000000020117C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA1_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 2***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA2
Address	00000000020117C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA2_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 3***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA3
Address	00000000020117C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA3_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 4***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA4
Address	00000000020117C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA4_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 5***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA5
Address	00000000020117C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA5_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 6***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA6
Address	00000000020117C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA6_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 2 Data 7***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF2_DATA7
Address	00000000020117C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF2_DATA7_MBS23_SRB_BUFF2_DATA: SRB Buffer2 Data

Register Name	***MBS23 SRB Buffer 3 Data 0***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA0
Address	00000000020117C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA0_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 1***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA1
Address	00000000020117CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA1_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 2***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA2
Address	00000000020117CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA2_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 3***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA3
Address	00000000020117CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA3_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 4***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA4
Address	00000000020117CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA4_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 5***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA5
Address	00000000020117CE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA5_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 6***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA6
Address	00000000020117CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA6_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	***MBS23 SRB Buffer 3 Data 7***
Mnemonic	MBU.MBS.SRB.MBS23_SRB_BUFF3_DATA7
Address	00000000020117D0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RO	MBS23_SRB_BUFF3_DATA7_MBS23_SRB_BUFF3_DATA: SRB Buffer3 Data

Register Name	*Trace Array High Data Register*
Mnemonic	TCN.TRA.MBS1TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000002011880 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	*Trace Array Low Data Register*
Mnemonic	TCN.TRA.MBS1TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000002011881 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	*Trace Array High Data Register*
Mnemonic	TCN.TRA.MBS2TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	00000000020118C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	*Trace Array Low Data Register*
Mnemonic	TCN.TRA.MBS2TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	00000000020118C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95

Bits	SCOM	Field Mnemonic: Description
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	***Configuration Of CC Counters***
Mnemonic	TCN.SYNC_CONFIG
Address	0000000002030000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ISLE_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from chiplet
1	RW	PCB_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from pcb
2	RW	CLKSTP_SYNC_EN: stop clocks aligned to sync pulse
3	RW	EDRAM_XSTOP_MASK_B: mask for clockstop of eDRAM clock on any xstop
4	RW	PLL_XSTOP_MASK_B: mask for clockstop of pll clock on any xstop
5	RW	LOCAL_XSTOP_MASK_B: mask for clockstop of all island clocks on local xstop from chiplet
6	RW	DISABLE_PCB_ITR: disable interrupt generation within CC
7	RW	USE_SYNC_FOR_SCAN: if set, use opcg initial alignment for scan requests
8	RW	KEEP_EDRAM_ON_XSTOP: keep eDRAM enabled when a checkstop occurs
9	RW	TRIGGER_OPCG_ON_XSTOP: trigger opcg on xstop instead of performing clockstop
10	RW	SEL_EXT_OPCG_TRIGGER: select external OPCG trigger (set OPCG in slave mode)
11	RW	LISTEN_TO_SYNC_PULSE: enable phase counter synchronization by sync_pulse signal
12	RW	SYNC_CLK_START_ENABLE: enable clk start driven by tc_sync_clk_stop (falling edge)
13	RW	SYNC_CLK_STOP_ENABLE: enable clk stop driven by tc_sync_clk_stop (rising_edge)
14	RWX_WOR	CHIP_PROTECTION_ENABLE: memory buffer only - can only be set, but not cleared via PCB. When this bit is SET, no clock starts are possible
15	RW	SPARE15: spare
16	RW	SPARE16: spare
17	RW	SPARE17: spare
18	RW	SPARE18: spare
19	RW	SPARE19: spare
20	RW	SPARE20: spare

Register Name	*Counter Offset*
Mnemonic	TCN.PHASE_SHADOW
Address	0000000002030001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RWX	PHASE_COUNT_SHADOW_Q: offset for sync counter
6	RO	constant=0b0

Register Name	*OPCG Control Register 0*
Mnemonic	TCN.OPCG_REG0
Address	0000000002030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), runn-mode: loopcnt(4:6)
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count (l = 1-2^28 (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	*OPCG Control Register 1*
Mnemonic	TCN.OPCG_REG1
Address	0000000002030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1
4:43	RW	FUNC_CAPT_INSTR_F: BIST mode: functional capture Instr 0-7 f domain (sl, nsl, ary, sg, fce)

Bits	PCB	Field Mnemonic: Description
44:63	RW	FUNC_CAPT_INSTR_FBY2: BIST mode: functional capture Instr 0-3 f/2 domain (sl, nsl, ary, sg, fce)

Register Name	*OPCG Control Register 2*
Mnemonic	TCN.OPCG_REG2
Address	0000000002030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	SCAN_CLK_USE_EVEN: BIST mode: Generate scan clock in f odd cycle. runn-mode: run one additional clock in f domain
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill and SNOP runn-mode: OPCG engine controls start_abist (overrides GP0 setting)
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	*Opcg Start Register*
Mnemonic	TCN.OPCG_REG3
Address	0000000002030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence)
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse)
2	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse)
3:4	RW	ALIGN_SOURCE_SELECT: 0: use inopa setting from opcg_reg0, 1: use rising edge of sync pulse, 2: use input from unit (for AVP)
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: set to 0 for prpg always on, else seed

Bits	PCB	Field Mnemonic: Description
20	RW	EXTEND_INOPW_ENOPW: extend I/ENOPW: add 256 cycles if i/enop>0, else 257+max i/enop
21	RW	EXTEND_SNOPW: add 256 cycles if snop>0, else 257+max snop
22	RW	FORCE_SG_HIGH_DURING_SNOP: force sg high during snop
23:31	RW	CHKSW: reserved for debug switches (keep 0 unless chksw required)
32:43	RW	PRPG_A_VAL: a value for PRPG aperture
44:55	RW	PRPG_B_VAL: b value for PRPG aperture
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end)
57:63	RW	SPARE3: spares

Register Name	***Start/stop Of Clocks***
Mnemonic	TCN.CLK_REGION
Address	0000000002030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	constant=0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)
5	RWX	CLOCK_REGION_FASTUNIT0: for clock region mbi
6	RWX	CLOCK_REGION_FASTUNIT1: for clock region dmi
7	RWX	CLOCK_REGION_UNIT2: for clock region msc
8	RWX	CLOCK_REGION_UNIT3: for clock region mbs
9	RWX	CLOCK_REGION_UNIT4: for clock region unit4 region is UNUSED
10	RWX	CLOCK_REGION_UNIT5: for clock region refr
11	RWX	CLOCK_REGION_PLL: for clock region pll region is UNUSED
12:19	RO	constant=0b00000000
20	RWX	SEL_THOLD_SL: select sl tholds
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name	***Scan Region And Type***
Mnemonic	TCN.SCANSELQ
Address	0000000002030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b000
3	RW_WCLRPART	SCANSEL_CLK_VITL: scan clock region vitl (Vital = Clock)

Bits	PCB	Field Mnemonic: Description
4	RWX	SCANSEL_CLK_PERV: scan clock region perv (Pervasive)
5	RWX	SCANSEL_CLK_FASTUNIT0: scan clock region mbi
6	RWX	SCANSEL_CLK_FASTUNIT1: scan clock region dmi
7	RWX	SCANSEL_CLK_UNIT2: scan clock region msc
8	RWX	SCANSEL_CLK_UNIT3: scan clock region mbs
9	RWX	SCANSEL_CLK_UNIT4: scan clock region unit4 region is UNUSED
10	RWX	SCANSEL_CLK_UNIT5: scan clock region refr
11	RWX	SCANSEL_CLK_PLL: scan clock region pll region is UNUSED
12:19	RO	constant=0b00000000
20	RW	SCANSEL_FUNC: scan chain func (functional)
21	RW	SCANSEL_CFG: scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: scan chain ccfg / gptr (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: scan chain regf (register files)
24	RW	SCANSEL_LBIST: scan chain lbst (LBIST)
25	RW	SCANSEL_ABIST: scan chain abst (ABIST)
26	RW	SCANSEL_REPR: scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: scan chain time (Array Timing)
28	RW	SCANSEL_BNDY_FARY: scan chain bndy (Boundary IOs)
29	RW	SCANSEL_FARR: scan chain farr (fast array unload)
30	RW	SCANSEL_CMSK: scan chain cmsk (lbist channel mask)

Register Name	***Clocks Running***
Mnemonic	TCN.CLOCK_STAT
Address	0000000002030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: status of perv func_sl_thold 0=run, 1=stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: status of perv func_nsl_thold 0=run, 1=stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: status of perv ary_nsl_thold 0=run, 1=stop
3	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_SL: status of mbi_odd func_sl_thold 0=run, 1=stop
4	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_SL: status of mbi_even func_sl_thold 0=run, 1=stop
5	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_NSL: status of mbi_odd func_nsl_thold 0=run, 1=stop
6	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_NSL: status of mbi_even func_nsl_thold 0=run, 1=stop
7	ROX	CLOCK_STATUS_FASTUNIT0_ODD_ARY_NSL: status of mbi_odd ary_nsl_thold 0=run, 1=stop
8	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_ARY_NSL: status of mbi_even ary_nsl_thold 0=run, 1=stop
9	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_SL: status of dmi_odd func_sl_thold 0=run, 1=stop
10	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_SL: status of dmi_even func_sl_thold 0=run, 1=stop
11	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_NSL: status of dmi_odd func_nsl_thold 0=run, 1=stop
12	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_NSL: status of dmi_even func_nsl_thold 0=run, 1=stop

Bits	PCB	Field Mnemonic: Description
13	ROX	CLOCK_STATUS_FASTUNIT1_ODD_ARY_NSL: status of dmi_odd ary_nsl_thold 0=run, 1=stop
14	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_ARY_NSL: status of dmi_even ary_nsl_thold 0=run, 1=stop
15	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of msc func_sl_thold 0=run, 1=stop
16	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of msc func_nsl_thold 0=run, 1=stop
17	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of msc ary_nsl_thold 0=run, 1=stop
18	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of mbs func_sl_thold 0=run, 1=stop
19	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of mbs func_nsl_thold 0=run, 1=stop
20	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of mbs ary_nsl_thold 0=run, 1=stop
21	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of unit4 func_sl_thold 0=run, 1=stop region is UNUSED
22	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of unit4 func_nsl_thold 0=run, 1=stop region is UNUSED
23	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of unit4 ary_nsl_thold 0=run, 1=stop region is UNUSED
24	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of refr func_sl_thold 0=run, 1=stop
25	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of refr func_nsl_thold 0=run, 1=stop
26	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of refr ary_nsl_thold 0=run, 1=stop
27	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of pll func_sl_thold 0=run, 1=stop region is UNUSED
28	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of pll func_nsl_thold 0=run, 1=stop region is UNUSED
29	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of pll ary_nsl_thold 0=run, 1=stop region is UNUSED
30:63	RO	constant=0b11111111111111111111111111111111

Register Name	***Error Status Of CC***
Mnemonic	TCN.ERROR_STATUS
Address	0000000002030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: scan collision - high when scan protection error occurred
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error - during test its ok, but in system its a error
13	RWX	PHASE_CNT_CORRUPTED: phase hold counter corruption detected

Bits	PCB	Field Mnemonic: Description
14:15	RWX	CC_PAR_ERR: parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: parity error in GP0 register
17	RWX	SECURITY_VIOLATION: security_violation - when Chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name	***CC Protect Mode Register***
Mnemonic	TCN.CC_PROTECT_MODE_REG
Address	00000000020303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TCN.CC_ATOMIC_LOCK_REG
Address	00000000020303FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	CC_ATOMIC_ID: Atomic ID

Register Name	***Global Checkstop FIR***
Mnemonic	TCN.XFIR
Address	0000000002040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: xstop from other chips
3	RWX	XFIR_IN3: xstop from pervasive unit
4	RWX	XFIR_IN4: unused
5	RWX	XFIR_IN5: xstop from dmi
6	RWX	XFIR_IN6: xstop from mbi
7	RWX	XFIR_IN7: xstop from mbs0
8	RWX	XFIR_IN8: xstop from mbs1

Bits	PCB	Field Mnemonic: Description
9	RWX	XFIR_IN9: xstop from mbs2
10	RWX	XFIR_IN10: xstop from mbs3
11	RWX	XFIR_IN11: xstop from mbs4
12	RWX	XFIR_IN12: xstop from fbistn
13	RWX	XFIR_IN13: xstop from scac
14	RWX	XFIR_IN14: xstop from mbs secure fir
15:25	RWX	XFIR_IN15: unused
26	RWX	XFIR_IN26: xstop on debug trigger

Register Name	***Global Recoverable FIR***
Mnemonic	TCN.RFIR
Address	0000000002040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: unused
1	ROX	LFIR_RECOV_ERR: error from local LFIR
2:23	ROX	RFIR_IN: recoverable errors: same mapping as XFIR(4:25)

Register Name	***FIR Mask***
Mnemonic	TCN.FIR_MASK
Address	0000000002040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit
1	RW	FIR_MASK_IN1: mask for xfir PCB status bit
2	RW	FIR_MASK_IN2: mask for xfir IO status bit
3	RW	FIR_MASK_IN3: mask for LFIR status bit
4:26	RW	FIR_MASK_IN4: masks for XFIR and RFIR

Register Name	***Special Attention***
Mnemonic	TCN.EPS.FIR.SPATTN
Address	0000000002040004 (PCB) 0000000002040005 (PCB1) 0000000002040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: MEM Chiplet Only: Special Attention from MBA01
1	ROX	NCX	NCX	SPATTN_IN1: MEM Chiplet Only: Special Attention from MBA23
2:9	ROX	NCX	NCX	SPATTN_IN2: unused special attentions

Register Name	***Special Attention Mask***
Mnemonic	TCN.EPS.FIR.SPA_MASK
Address	0000000002040007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask

Register Name	***Mode Register***
Mnemonic	TCN.EPS.FIR.MODE_REG
Address	0000000002040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: unused

Register Name	***Local FIR***
Mnemonic	TCN.LOCAL_FIR
Address	000000000204000A (PCB) 000000000204000B (PCB1) 000000000204000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (Critical Trip error)
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (Fatal Trip error)
10	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Thermal (Voltage trip error)
11	RWX	WOX_AND	WOX_OR	FIR_IN11: local errors from Trace Array (error)
12	RWX	WOX_AND	WOX_OR	FIR_IN12: local errors from Trace Array (error)
13:39	RWX	WOX_AND	WOX_OR	FIR_IN13: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	***Local FIR Mask***
Mnemonic	TCN.EPS.FIR.LOCAL_FIR_MASK
Address	000000000204000D (PCB) 000000000204000E (PCB1) 000000000204000F (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

Register Name	***Local FIR Action0***
Mnemonic	TCN.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000002040010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name	***Local FIR Action1***
Mnemonic	TCN.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000002040011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name	***DTS Thermal Sensor Results***
Mnemonic	TCN.EPS.THERM.DTS_RESULT0
Address	0000000002050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***DTS Trace Results***
Mnemonic	TCN.EPS.THERM.DTS_TRC_RESULT
Address	0000000002050003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant=0b000
48:63	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with ID 0.

Register Name	***DTS0-1 Bit 0 - 15: Temperature Result DTS0, Bit 16 - 31: Temperature Result DTS1(available Only In NEST Chiplet),***
Mnemonic	TCN.EPS.THERM.ENC_CPM_RESULT0
Address	0000000002050008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.
32:55	RO	constant=0b000000000000000000000000

Register Name	***Voltage Sensor Results***
Mnemonic	TCN.EPS.THERM.VOLT_READ0
Address	000000000205000B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	Reserved field. (Access type is volt_data0)
16:31	ROX	Reserved field. (Access type is volt_data1)
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***CPM & DTS Enables And Controls***
Mnemonic	TCN.EPS.THERM.THERM_MODE_REG
Address	000000000205000F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: critical path result bubble correction active
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables 1xx: trip0 - warning x1x: trip1 - critical xx1: trip2 - fatal
5	RW	THERM_DTS_SAMPLE_ENA: 0: no dts sampling, 1: dts sampling is enabled and below counter compare match can occur.

Bits	PCB	Field Mnemonic: Description
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is feed into an 18 Bit counter, with the therm_sample_pulse_cnt it is possible to select a highorder bit of the counter to enable a resolutions of sampling dtss between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a dts sample 0000: 16 ms 0001: 8 ms 0010: 4 ms 0011: 2 ms 0100: 1 ms 0101: 0.5 ms 0110: 250 us 0111: 125 us 1000: 62 .5us 1001: 31.3 us 1010: 15.6 us 1011: 7.8 us 1100: 3.9 us 1101: 2 us 1110: 1 us 1111: 0.5 us
10:11	RW	THERM_THRES_MODE_ENA: forces max or min mode in threshold unit: 00: is off 11: is illegal 10: max mode 01: min mode
12	RW	DTS_TRIGGER_MODE: unused
13	RW	DTS_TRIGGER_SEL: unused
14:15	RW	THERM_MODE_UNUSED: unused
16:19	RW	THERM_DTS_READ_SEL: selects which dts result will be provided with pcb read addr_v(4): 000: DTS 0 001: DTS 1 010: DTS 2 011: DTS 3 100: DTS 4 111: Worst Case Sensor
20:21	RW	THERM_DTS_ENABLE: dts enables: 1xxxx: DTS 0 available x1xx: DTS 1 available
22:34	RO	constant=0b0000000000000
35:36	RW	THERM_CPM_ENABLE: cpm enables

Register Name	***Skitter Control Register***
Mnemonic	TCN.EPS.THERM.SKITTER_MODE_REG
Address	0000000002050010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: forces skitter to hold current sample
1	RW	DISABLE_SKITTER_STICKINESS: if '0' accumulation mode, '1' samples new value each cycle and resets sticky value
2:3	RW	SKITTER_MODE_UNUSED1: unused
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0 bit1: _on_trigger1

Bits	PCB	Field Mnemonic: Description
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0 bit1: reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: selects guts to measure: 00: guts1 01: guts2 10: guts3 11: guts4
10:43	RO	constant=0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: forces skitter to hold current sample on dbg trigger, this has highest priority
45	ROX	SKITTER_DATA_V_LT: if '1' the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 pcb reads

Register Name	*Error Injection Control Register*
Mnemonic	TCN.EPS.THERM.INJECT_REG
Address	0000000002050011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection 01: warning trip level injection 10: critical trip level injection 11: fatal trip level injection
2:3	RW	THERM_INJECT_MODE: 00: no injection 01: injection on the next dts sample 10: solid injection for the next dts samples till bit setting changes 11: not used

Register Name	*Control / Force Reset Register*
Mnemonic	TCN.EPS.THERM.CONTROL_REG
Address	0000000002050012 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	WO_1P	Reserved field. (Access type is reset_trip_history)
1	WO_1P	Reserved field. (Access type is reset_sample_pulse_cnt)
2	WO_1P	Reserved field. (Access type is f_reset_cpm_rd)
3	WO_1P	Reserved field. (Access type is f_reset_cpm_wr)
4	WO_1P	Reserved field. (Access type is reset_sample_dts)
5	WO_1P	Reserved field. (Access type is force_sample_dts)
6	WO_1P	Reserved field. (Access type is force_sample_dts_interruptible)
7	WO_1P	Reserved field. (Access type is force_reset_thres_l1results)
8	WO_1P	Reserved field. (Access type is force_reset_thres_l2results)

Bits	PCB	Field Mnemonic: Description
9	WO_1P	Reserved field. (Access type is force_reset_thres_l3results)
10	WO_1P	Reserved field. (Access type is force_measure_volt_interruptible)
11	WO_1P	Reserved field. (Access type is force_reset_measure_volt)
12	WO_1P	Reserved field. (Access type is force_shift_sensor)

Register Name	***Thermal Error Status Register***
Mnemonic	TCN.EPS.THERM.ERR_STATUS_REG
Address	0000000002050013 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is serial_shiftcnt_modereg_parity_err_hold)
1	ROX	Reserved field. (Access type is therm_modereg_parity_err_hold)
2	ROX	Reserved field. (Access type is skitter_modereg_parity_err_hold)
3	ROX	Reserved field. (Access type is skitter_forcereg_parity_err_hold)
4	ROX	Reserved field. (Access type is scan_init_version_reg_parity_err_hold)
5	ROX	Reserved field. (Access type is volt_modereg_parity_err_hold)
6	ROX	Reserved field. (Access type is skitter_clksrcreg_parity_err_hold)
7	ROX	Reserved field. (Access type is count_state_err_hold)
8	ROX	Reserved field. (Access type is run_state_err_hold)
9	ROX	Reserved field. (Access type is thres_therm_state_err_hold)
10	ROX	Reserved field. (Access type is thres_therm_overflow_err_hold)
11	ROX	Reserved field. (Access type is shifter_parity_err_hold)
12	ROX	Reserved field. (Access type is shifter_valid_err_hold)
13	ROX	Reserved field. (Access type is timeout_err_hold)
14	ROX	Reserved field. (Access type is f_skitter_err_hold)
15	ROX	Reserved field. (Access type is pcb_err_hold_out)
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: serial shift count parity error mask
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: therm mode reg parity error mask
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: skitter mode register parity error mask
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: skitter force register parity error mask
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: scan init version register parity error mask
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: volt mode reg parity error mask
22	RO	constant=0b0
23	ROX	COUNT_STATE_ERR_MASK: count state machine error mask
24	ROX	RUN_STATE_ERR_MASK: run state machine error mask
25	ROX	THRES_STATE_ERR_MASK: thres state machine error mask
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask

Bits	PCB	Field Mnemonic: Description
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask
30	ROX	F_SKITTER_READ_ERR_MASK: force skitter read one hot error mask
31	ROX	PCB_ERR_MASK: pervasive control bus error mask
32:39	RO	constant=0b00000000
40:43	ROX	Reserved field. (Access type is count_state_lt)
44:46	ROX	Reserved field. (Access type is run_state_lt)
47	ROX	Reserved field. (Access type is shift_dts_lt)
48	ROX	Reserved field. (Access type is shift_volt_lt)
49:50	ROX	Reserved field. (Access type is read_state_lt)
51:54	ROX	Reserved field. (Access type is write_state_lt)
55	ROX	Reserved field. (Access type is sample_dts_lt)
56	ROX	Reserved field. (Access type is measure_volt_lt)
57	ROX	Reserved field. (Access type is read_cpm_lt)
58	ROX	Reserved field. (Access type is write_cpm_lt)
59	ROX	Reserved field. (Access type is unused)
60:63	RO	constant=0b0000

Register Name	***Skitter Force Read Register***
Mnemonic	TCN.EPS.THERM.SKITTER_FORCE_REG
Address	0000000002050014 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter

Register Name	***Voltage Sensor Enables And Controls***
Mnemonic	TCN.EPS.THERM.VOLT_MODE_REG
Address	0000000002050015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	VOLT_MEASURE_ENA: enables the measurement of voltage sensor
1	RW	VOLT_TRIP_ENA: enables the trip of voltage sensor
2:3	RW	VOLT_ENABLE: Voltage sensor enables 1xxxx:voltage sensor0 available

Register Name	***Skitter Clock Src Control Register***
Mnemonic	TCN.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000002050016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: selects clock to measure: 000: local mesh clock 001: external pin skitter_c1_1_in 010: local d1clk only if d_mode = 1 011: external pin skitter_c1_2_in 100: local lclk only if d_mode = 1 101: external pin skitter_c1_3_in 110: unused 111: external pin skitter_c1_4_in
3:35	RO	constant=0b00000000000000000000000000000000

Register Name	***Skitter Data Register Read Bit0:63***
Mnemonic	TCN.EPS.THERM.SKITTER_DATA0
Address	0000000002050019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Skitter Data Register Read Bit32:95***
Mnemonic	TCN.EPS.THERM.SKITTER_DATA1
Address	000000000205001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Skitter Data Register Read Bit64:127***
Mnemonic	TCN.EPS.THERM.SKITTER_DATA2
Address	000000000205001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	*Timestamp Counter Read*
Mnemonic	TCN.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000205001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.

Register Name	*Contains The Slave's Primary Address*
Mnemonic	TPTOP.NET.PCBSLNEST.PRIMARY_ADDRESS_REG
Address	00000000020F0000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field. (Access type is primary_address)

Register Name	*Multicast Group 1*
Mnemonic	TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_1
Address	00000000020F0001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	*Multicast Group 2*
Mnemonic	TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_2
Address	00000000020F0002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name	***Multicast Group 3***
Mnemonic	TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_3
Address	00000000020F0003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	***Multicast Group 4***
Mnemonic	TPTOP.NET.PCBSLNEST.MULTICAST_GROUP_4
Address	00000000020F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	***Timeout Select Register***
Mnemonic	TPTOP.NET.PCBSLNEST.TIMEOUT_REG
Address	00000000020F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field. (Access type is int_timeout)

Register Name	***Assist Interrupt Register***
Mnemonic	TPTOP.NET.PCBSLNEST.ASSIST_INTERRUPT_REG
Address	00000000020F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is attn)
1	ROX	Reserved field. (Access type is recov)
2	ROX	Reserved field. (Access type is xstop)

Register Name	*GP3 Register (NA In PERV CPLT)*
Mnemonic	TPTOP.NET.PCBSLNEST.GP3_REG
Address	00000000020F0012 (PCB) 00000000020F0013 (PCB1) 00000000020F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2:4	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
5	RWX	RWX_WAND	RWX_WOR	NCLK_NODIV: Force cache_nclk to equal nclk (for test only).
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FENCE2_EN: Fencing signal for chiplet.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
22	RWX	RWX_WAND	RWX_WOR	RESCLK_FLUSH: Flush for resonant clocking.
23	RWX	RWX_WAND	RWX_WOR	RESCLK_OVERRIDE_VALUE: Override value for resonant clocking.
24	RWX	RWX_WAND	RWX_WOR	DPHY_PLL: dphy pll
25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	FSYNC_ENABLE: Set the 'Frame Synchronous (Geared) Clocking Mode'.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
30	RWX	RWX_WAND	RWX_WOR	CHIPET_RI: Chiplet RI
31	RWX	RWX_WAND	RWX_WOR	CHIPET_DI1: Chiplet DI1

Register Name	*Skew Adjust Data*
Mnemonic	TPTOP.NET.PCBSLNEST.CLK_ADJ_REG
Address	00000000020F0015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	*Clk Ajust Config*
Mnemonic	TPTOP.NET.PCBSLNEST.CLK_ADJ_SET
Address	00000000020F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	*Vital Scan Out*
Mnemonic	TPTOP.NET.PCBSLNEST.VITAL_SCAN_OUT
Address	00000000020F0017 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	*Chiplet Heartbeat Register*
Mnemonic	TPTOP.NET.PCBSLNEST.HEARTBEAT_REG
Address	00000000020F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

Register Name	*Lock Indications From PLLs*
Mnemonic	TPTOP.NET.PCBSLNEST.PLL_LOCK_REG
Address	00000000020F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock)

Register Name	*Attn Interrupt*
Mnemonic	TPTOP.NET.PCBSLNEST.ATTN_INTERRUPT_REG
Address	00000000020F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is attn)

Register Name	*Recov Interrupt*
Mnemonic	TPTOP.NET.PCBSLNEST.RECOV_INTERRUPT_REG
Address	00000000020F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is recov)

Register Name	*Xstop Interrupt*
Mnemonic	TPTOP.NET.PCBSLNEST.XSTOP_INTERRUPT_REG
Address	00000000020F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is xstop)

Register Name	*Slave Config Register*
Mnemonic	TPTOP.NET.PCBSLNEST.SLAVE_CONFIG_REG
Address	00000000020F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting

Bits	PCB	Field Mnemonic: Description
13:15	RW	

Register Name	*Error Capture Register*
Mnemonic	TPTOP.NET.PCBSLNEST.ERROR_REG
Address	00000000020F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad

Bits	PCB	Field Mnemonic: Description
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name	***Hang Pulse Generation Register 0***
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_0_REG
Address	00000000020F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 1***
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_1_REG
Address	00000000020F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 2***
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_2_REG
Address	00000000020F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 3*
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_3_REG
Address	00000000020F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 4*
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_4_REG
Address	00000000020F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 5*
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_5_REG
Address	00000000020F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 6*
Mnemonic	TPTOP.NET.PCBSLNEST.HANG_PULSE_6_REG
Address	00000000020F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Divider For Hang Counter Clock***
Mnemonic	TPTOP.NET.PCBSLNEST.PRE_COUNTER_REG
Address	00000000020F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

Register Name	***Protect Mode Register***
Mnemonic	TPTOP.NET.PCBSLNEST.PROTECT_MODE_REG
Address	00000000020F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TPTOP.NET.PCBSLNEST.ATOMIC_LOCK_REG
Address	00000000020F03FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

4. PCB Slave 2: DMI Indirect Registers

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_ERROR_INJECT_PB	0x800F98000201043F	1444
DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_MASK_PB	0x800F90000201043F	1444
DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_PB	0x800F88000201043F	1443
DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_RESET_PB	0x800F80000201043F	1443
DMI.BUSCTL.BUS_CTL_REGS.TX_ANALOG_IREF_PB	0x800F34000201043F	1442
DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_NVAL_PB	0x800F0C000201043F	1439
DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_PB	0x800F04000201043F	1439
DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_PVAL_PB	0x800F14000201043F	1439
DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_P_4X_PB	0x800F1C000201043F	1440
DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_SWO1_PB	0x800F24000201043F	1440
DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_SWO2_PB	0x800F2C000201043F	1442
DMI.BUSCTL.BUS_CTL_REGS.TX_INIT_VERSION_PB	0x800F44000201043F	1443
DMI.BUSCTL.BUS_CTL_REGS.TX_MINIKERF_PB	0x800F3C000201043F	1442
DMI.BUSCTL.BUS_CTL_REGS.TX_SCRATCH_REG_PB	0x800F4C000201043F	1443
DMI.RX.RXCLKCTL.CUPLL_CTL	0x0000008000000010	836
DMI.RX.RXCLKCTL.CUPLL_CTL_SETUP	0x0000008000000013	837
DMI.RX.RXCTL.RX_CTL2_REGS.RX_STOP_ADDR_LSB_PG	0x800838000201043F	1171
DMI.RX.RXCTL.RX_CTL2_REGS.RX_STOP_CNTL_STAT_PG	0x800810000201043F	1170
DMI.RX.RXCTL.RX_CTL2_REGS.RX_STOP_MASK_LSB_PG	0x800840000201043F	1171
DMI.RX.RXCTL.RX_CTL2_REGS.RX_WT_CONFIG_PG	0x800A20000201043F	1196
DMI.RX.RXCTL.RX_CTL_REGS.RX_AMAX_PG	0x800A68000201043F	1200
DMI.RX.RXCTL.RX_CTL_REGS.RX_AMIN_PG	0x800A60000201043F	1200
DMI.RX.RXCTL.RX_CTL_REGS.RX_AMP_OFFSET_PG	0x800A78000201043F	1201
DMI.RX.RXCTL.RX_CTL_REGS.RX_AMP_VAL_PG	0x800A70000201043F	1200
DMI.RX.RXCTL.RX_CTL_REGS.RX_AN_PG	0x800A58000201043F	1199
DMI.RX.RXCTL.RX_CTL_REGS.RX_AP_PG	0x800A50000201043F	1199
DMI.RX.RXCTL.RX_CTL_REGS.RX_BAD_LANE_ENC_GCRMSG_PG	0x800988000201043F	1188
DMI.RX.RXCTL.RX_CTL_REGS.RX_BER_CHK_PG	0x800AF0000201043F	1206
DMI.RX.RXCTL.RX_CTL_REGS.RX_BER_CNTL_PP	0x800B50000201043F	1229
DMI.RX.RXCTL.RX_CTL_REGS.RX_BER_MODE_PP	0x800B58000201043F	1231
DMI.RX.RXCTL.RX_CTL_REGS.RX_BIST_GCRMSG_PP	0x800BB8000201043F	1373
DMI.RX.RXCTL.RX_CTL_REGS.RX_CLK_MODE_PG	0x800800000201043F	1168
DMI.RX.RXCTL.RX_CTL_REGS.RX_CNTL_FAST_PP	0x800B10000201043F	1219
DMI.RX.RXCTL.RX_CTL_REGS.RX_DESKEW_GCRMSGS_PG	0x800968000201043F	1187
DMI.RX.RXCTL.RX_CTL_REGS.RX_DESKEW_MODE_PG	0x800978000201043F	1188
DMI.RX.RXCTL.RX_CTL_REGS.RX_DESKEW_STATUS_PG	0x800980000201043F	1188
DMI.RX.RXCTL.RX_CTL_REGS.RX_DFE_CONFIG_PP	0x800B78000201043F	1309
DMI.RX.RXCTL.RX_CTL_REGS.RX_DFE_TIMERS_PP	0x800B80000201043F	1312
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_CONFIG_PG	0x800A18000201043F	1195
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_GCRMSG_PG	0x800A28000201043F	1196
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_PG	0x800A08000201043F	1194
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_TIMEOUTS_PP	0x800B40000201043F	1223
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_DEBUG2_PG	0x800870000201043F	1173
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_DEBUG_PG	0x800AD8000201043F	1204
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_ERR_TALLYING1_PG	0x8009D8000201043F	1191

Mnemonic	Address	Page
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_ERR_TALLYING2_PG	0x800AE0000201043F	1205
DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_GCRMSG_PG	0x8009D0000201043F	1191
DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_CONVERGENCE_PG	0x800A80000201043F	1201
DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_FINAL_L2U_GCRMSGS_PG	0x8009E0000201043F	1192
DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_STEP_CNTL_PG	0x800A38000201043F	1198
DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_STEP_STAT_PG	0x800A40000201043F	1199
DMI.RX.RXCTL.RX_CTL_REGS.RX_ERR_TALLYING_GCRMSG_PG	0x800AA0000201043F	1202
DMI.RX.RXCTL.RX_CTL_REGS.RX_FENCE_PG	0x8009A8000201043F	1189
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIFO_MODE_PG	0x8008A0000201043F	1178
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR1_ERROR_INJECT_PG	0x8008F0000201043F	1180
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR1_MASK_PG	0x8008E0000201043F	1180
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR1_PG	0x8008D0000201043F	1179
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR2_ERROR_INJECT_PG	0x8008F8000201043F	1181
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR2_MASK_PG	0x8008E8000201043F	1180
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR2_PG	0x8008D8000201043F	1179
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR_TRAINING_MASK_PG	0x800908000201043F	1182
DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR_TRAINING_PG	0x800900000201043F	1181
DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_DEST_ADDR_PG	0x8009F8000201043F	1194
DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_DEST_IDS_PG	0x8009E8000201043F	1193
DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_SRC_IDS_PG	0x8009F0000201043F	1193
DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_WRITE_DATA_PG	0x800A00000201043F	1194
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DMI.RX.RXCTL.RX_CTL_REGS.RX_ID3_PG	0x800860000201043F	1172
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DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_BAD_VEC_16_31_PG	0x800920000201043F	1185
DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_DISABLED_VEC_0_15_PG	0x800928000201043F	1185
DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_DISABLED_VEC_16_31_PG	0x800930000201043F	1185
DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_SWAPPED_VEC_0_15_PG	0x800938000201043F	1186
DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_SWAPPED_VEC_16_31_PG	0x800940000201043F	1186
DMI.RX.RXCTL.RX_CTL_REGS.RX_MINIKERF_PG	0x800868000201043F	1173
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DMI.RX.RXCTL.RX_CTL_REGS.RX_MODE1_PP	0x800B08000201043F	1207
DMI.RX.RXCTL.RX_CTL_REGS.RX_MODE2_PP	0x800BB0000201043F	1365
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DMI.RX.RXCTL.RX_CTL_REGS.RX_TIMEOUT_SEL2_PG	0x8009B8000201043F	1190
DMI.RX.RXCTL.RX_CTL_REGS.RX_TIMEOUT_SEL_PG	0x800898000201043F	1176
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DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PRBS_MODE_PL	0x8000B0100201043F	958
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DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SLS_PL	0x8000E8100201043F	987
DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL	0x800010100201043F	866
DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_TRACE_PL	0x800158100201043F	1016
DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_WT_STATUS_PL	0x8000F0100201043F	998
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DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL	0x800404100201043F	1041
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434100201043F	1089
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414100201043F	1058
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C110201043F	1070
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C110201043F	1166
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C110201043F	1119
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464110201043F	1146
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C110201043F	1139
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_PL	0x800454110201043F	1132
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C110201043F	1157
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_PL	0x800404110201043F	1042

Mnemonic	Address	Page
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434110201043F	1090
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414110201043F	1058
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C120201043F	1071
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C120201043F	1167
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C120201043F	1120
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464120201043F	1146
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C120201043F	1139
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_PL	0x800454120201043F	1132
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C120201043F	1158
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_PL	0x800404120201043F	1044
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434120201043F	1091
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414120201043F	1059
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP	0x800E9C000201043F	1406
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP	0x800EA4000201043F	1413
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP	0x800EBC000201043F	1426
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP	0x800EB4000201043F	1423
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP	0x800EC4000201043F	Error: Reference source not found
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP	0x800EAC000201043F	1420
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP	0x800E8C000201043F	1396
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP	0x800ECC000201043F	1432
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP	0x800E94000201043F	1400
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP	0x800ED4000201043F	1434
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP	0x800EDC000201043F	1436
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP	0x800EE4000201043F	1438
DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP	0x800E84000201043F	1389
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C130201043F	1071
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C130201043F	1167
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C130201043F	1121
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464130201043F	1146
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C130201043F	1139
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL	0x800454130201043F	1132
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C130201043F	1158
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL	0x800404130201043F	1045
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434130201043F	1092

Mnemonic	Address	Page
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414130201043F	1059
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C140201043F	1072
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C140201043F	1167
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C140201043F	1122
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464140201043F	1146
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C140201043F	1140
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL	0x800454140201043F	1133
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C140201043F	1159
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL	0x800404140201043F	1046
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434140201043F	1093
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414140201043F	1060
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C150201043F	1072
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C150201043F	1168
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C150201043F	1124
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464150201043F	1147
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C150201043F	1140
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL	0x800454150201043F	1133
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C150201043F	1160
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL	0x800404150201043F	1047
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434150201043F	1094
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414150201043F	1060
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C160201043F	1073
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C160201043F	1168
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C160201043F	1125
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464160201043F	1147
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C160201043F	1140
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_PL	0x800454160201043F	1133
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C160201043F	1160
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_PL	0x800404160201043F	1048
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434160201043F	1095
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414160201043F	1061

Mnemonic	Address	Page
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_BIST_STAT_PL	0x80042C170201043F	1073
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL	0x80047C170201043F	1168
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL	0x80043C170201043F	1126
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL	0x800464170201043F	1147
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_MASK_PL	0x80045C170201043F	1140
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_PL	0x800454170201043F	1134
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_FAST_PL	0x80046C170201043F	1161
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_PL	0x800404170201043F	1049
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_PRBS_MODE_PL	0x800434170201043F	1096
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_SPARE_MODE_PL	0x800414170201043F	1061
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP	0x800E9C000201043F	1407
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP	0x800EA4000201043F	1414
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP	0x800EBC000201043F	1427
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP	0x800EB4000201043F	1424
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP	0x800EC4000201043F	Error: Reference source not found
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP	0x800EAC000201043F	1421
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP	0x800E8C000201043F	1397
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP	0x800ECC000201043F	1432
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP	0x800E94000201043F	1401
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP	0x800ED4000201043F	1434
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP	0x800EDC000201043F	1436
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP	0x800EE4000201043F	1438
DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP	0x800E84000201043F	1389

The memory buffer registers are listed in the following tables.

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***PLL Control Register***
Mnemonic	DMI.RX.RXCLKCTL.CUPLL_CTL
Address	0000008000000010 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:10	RW	ANALOGTUNE: analogtune
11:14	RW	ATSTSEL: atstsel
15:16	RW	BANDSEL: bandsel
17:25	RW	DIVSELFB: divselfb
26:28	RW	BGOFFSET: bgoffset
29	RW	SPARE: spare
30	RW	CAPSEL: capsel
31:33	RW	CPISEL: cpisel
34:36	RW	ITUNE: itune
37:38	RW	PCLKSEL: pclksel
39:40	RW	PHASEFB: phasefb
41	RW	RDIV: rdiv
42	RW	REFCLKSEL: refclksel
43	RW	RESSEL: ressel
44	RW	VREGENABLE_N: vregenable_n
45	RW	VREGBYPASS: vregbypass

Bits	PLLREG	Field Mnemonic: Description
46	RW	PLLLOCK: plllock

Register Name	*PLL Control Register NSL*
Mnemonic	DMI.RX.RXCLKCTL.CUPLL_CTL_SETUP
Address	0000008000000013 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:10	RO	SHADOW_ANALOGTUNE: analogtune
11:14	RO	SHADOW_ATSTSEL: atstsel
15:16	RO	SHADOW_BANDSEL: bandsel
17:25	RO	SHADOW_DIVSELFB: divselfb
26:28	RO	SHADOW_BGOFFSET: bgoffset
29	RO	SHADOW_SPARE: spare
30	RO	SHADOW_CAPSEL: capsel
31:33	RO	SHADOW_CPISEL: cpisel
34:36	RO	SHADOW_ITUNE: itune
37:38	RO	SHADOW_PCLKSEL: pclksel
39:40	RO	SHADOW_PHASEFB: phasefb
41	RO	SHADOW_RDIV: rdiv
42	RO	SHADOW_REFCLKSEL: refclksel
43	RO	SHADOW_RESSEL: ressel
44	RO	SHADOW_VREGENABLE_N: vregenable_n
45	RO	SHADOW_VREGBYPASS: vregbypass

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_MODE_PL
Address	8000000A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_MODE_PL
Address	8000000B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_MODE_PL
Address	8000000C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_MODE_PL
Address	8000000D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_MODE_PL
Address	8000000E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_MODE_PL
Address	8000000F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*RX Lane Mode Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***RX Lane Mode Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_MODE_PL
Address	800000110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_LANE_PDWN: Used to receive inhibit and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (rx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers rx_lane_disabled_vec_0_15 and rx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and power down a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Receive Inhibited and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49:53	RO	constant=0b00000 Values: ENABLED=>0b0 DISABLED=>0b1
54	RWX	RX_LANE_SCRAMBLE_DISABLE: Used to disable the RX descrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800080080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800080090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_CNTL_PL
Address	8000080A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_CNTL_PL
Address	8000080B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_CNTL_PL
Address	8000080C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_CNTL_PL
Address	8000080D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_CNTL_PL
Address	8000080E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_CNTL_PL
Address	8000080F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Control And Status Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_CNTL_PL
Address	800008110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BLOCK_LOCK_LANE: Enables rotation and checking for block lock. 0b0 = Disable checking (forces block_locked_b to 1) 0b1 = Enable checking and run block lock. Values: DISABLED=>0b0 ENABLED=>0b1
49	RWX	RX_CHECK_SKEW_LANE: Per-Lane Initialization controls. Checks skew request.
50	RWX	RX_PDWN_LITE: GCR Message: When set, partially powers down unused spare lanes when not being recalibrated.
51	RWX	RX_OFFCAL_MODE: When set, put this lanes front end into offset cancellation mode. Only needed as an override since running offset cancellation does this automatically.. JFG
52:63	RO	constant=0b000000000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8000100A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8000100B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8000100C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8000100D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8000100E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	8000100F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX Per-lane Spare Mode Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SPARE_MODE_PL
Address	800010110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	RX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	RX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	RX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	RX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	RX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	RX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	RX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*RX BIST Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	8000280A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	8000280B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	8000280C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	8000280D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	8000280E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	8000280F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX BIST Status Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_BIST_STAT_PL
Address	800028110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_BIST_ERR: Indicates that RXBIST did not find two data eyes of sufficient width.. JGR 0b0 = No Error 0b1 = An Error has occured during RXBIST Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is rx_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***RX Even Sample Latch Offset Control Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.

Bits	SCOM	Field Mnemonic: Description
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	8000400A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	8000400B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	8000400C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	8000400D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	8000400E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	8000400F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Even Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_EVEN_PL
Address	800040110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_EVEN_SAMP1: This is the vertical offset of the even sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_EVEN_SAMP0: This is the vertical offset of the even sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	8000480A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	8000480B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	8000480C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	8000480D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	8000480E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	8000480F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Odd Sample Latch Offset Control Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_OFFSET_ODD_PL
Address	800048110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_OFFSET_ODD_SAMP1: This is the vertical offset of the odd sampling latch.
56	RO	constant=0b0
57:63	RWX	RX_OFFSET_ODD_SAMP0: This is the vertical offset of the odd sampling latch.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	8000500A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	8000500B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	8000500C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	8000500D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	8000500E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	8000500F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_VAL_PL
Address	800050110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK: This is the vertical offset of the pre-amp.
52:55	RWX	RX_AMP_GAIN: This is the gain setting of the pre-amp.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET: This is the peaking setting of the pre-amp.

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	***RX Preamp Value Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	***RX Preamp Value Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	***RX Preamp Value Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	8000580A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	8000580B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	8000580C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	8000580D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Preamp Value Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	8000580E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	***RX Preamp Value Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	8000580F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	***RX Preamp Value Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	***RX Preamp Value Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMP_CNTL_PL
Address	800058110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_AMP_ADJ_DONE: VGA adjust is complete for this lane.
49	ROX	Reserved field. (Access type is rx_amp_adj_all_done_b_ro_signal)
50:63	RO	constant=0b00000000000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	***RX Phase Rotator Mode Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	***RX Phase Rotator Mode Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	***RX Phase Rotator Mode Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	8000680A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	8000680B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	8000680C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	8000680D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	***RX Phase Rotator Mode Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	8000680E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	***RX Phase Rotator Mode Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	8000680F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	***RX Phase Rotator Mode Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Mode Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_MODE_PL
Address	800068110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_PHASEROT_OFFSET: RX Phase Rotator fixed offset from learned value.
56:63	RO	constant=0b00000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	***RX Phase Rotator Control Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	***RX Phase Rotator Control Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	***RX Phase Rotator Control Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	8000700A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	***RX Phase Rotator Control Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	8000700B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	8000700C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	8000700D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	8000700E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	***RX Phase Rotator Control Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	8000700F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	***RX Phase Rotator Control Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX Phase Rotator Control Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PROT_CNTL_PL
Address	800070110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48	RWX	RX_BUMP_LEFT_HALF_UI: Per-Lane Bump left 1/2 UI control (Self-Clearing).
49	RWX	RX_BUMP_RIGHT_HALF_UI: Per-Lane Bump right 1/2 UI control (Self-Clearing).
50	RWX	RX_BUMP_ONE_UI: Per-Lane Bump 1 UI control (Self-Clearing).
51	RWX	RX_BUMP_TWO_UI: Per-Lane Bump 2 UI control (Self-Clearing).
52	NCX	Reserved field. (Access type is rx_ext_sr_wo_pulse_slow_signal)
53	NCX	Reserved field. (Access type is rx_ext_sl_wo_pulse_slow_signal)
54:63	RO	constant=0b0000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	8000780A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	8000780B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	8000780C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	8000780D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	8000780E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	8000780F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX FIFO Status Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIFO_STAT_PL
Address	800078110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_FIFO_L2U_DLY: RX FIFO load-to-unload delay, initailed during FIFO init and modified thereafter by the deskew machine. For setting X, the latency is 4*X to 4*X+4 UI. Default is 20-24 UI.
52	NCX	Reserved field. (Access type is rx_fifo_init_wo_pulse_slow_signal)
53:63	RO	constant=0b00000000000

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AP_PL
Address	800080000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AP_PL
Address	800080010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AP_PL
Address	800080020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AP_PL
Address	800080030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AP_PL
Address	800080040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AP_PL
Address	800080050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AP_PL
Address	800080060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AP_PL
Address	800080070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AP_PL
Address	800080080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AP_PL
Address	800080090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AP_PL
Address	8000800A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AP_PL
Address	8000800B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AP_PL
Address	8000800C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AP_PL
Address	8000800D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AP_PL
Address	8000800E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AP_PL
Address	8000800F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	*RX Ap Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AP_PL
Address	800080100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX Ap Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AP_PL
Address	800080110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_SAMP: Average value of a 1 in the even sampler.
56:63	RWX	RX_AP_ODD_SAMP: Average value of a 1 in the odd sampler.

Register Name	***RX An Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AN_PL
Address	800088000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	***RX An Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AN_PL
Address	800088010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AN_PL
Address	800088020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AN_PL
Address	800088030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AN_PL
Address	800088040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AN_PL
Address	800088050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	***RX An Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AN_PL
Address	800088060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	***RX An Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AN_PL
Address	800088070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	***RX An Even/Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AN_PL
Address	800088080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AN_PL
Address	800088090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AN_PL
Address	8000880A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AN_PL
Address	8000880B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AN_PL
Address	8000880C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AN_PL
Address	8000880D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AN_PL
Address	8000880E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AN_PL
Address	8000880F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AN_PL
Address	800088100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX An Even/Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AN_PL
Address	800088110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AN_EVEN_SAMP: Average value of a 0 in the even sampler.
56:63	RWX	RX_AN_ODD_SAMP: Average value of a 0 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMIN_PL
Address	8000900A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMIN_PL
Address	8000900B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMIN_PL
Address	8000900C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMIN_PL
Address	8000900D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_AMIN_PL
Address	8000900E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	*RX Amin Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_AMIN_PL
Address	8000900F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX Amin Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_AMIN_PL
Address	800090110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN: Lowest value of a 1 in the even sampler.
56:63	RWX	RX_AMIN_ODD: Lowest value of a 1 in the odd sampler.

Register Name	***RX H1 Even Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	***RX H1 Even Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	***RX H1 Even Sampler Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	***RX H1 Even Sampler Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	8000980A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	8000980B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	8000980C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	8000980D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	8000980E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	8000980F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Even Sampler Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_EVEN_PL
Address	800098110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_EVEN_SAMP1: DFE H1 value for Even sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_EVEN_SAMP0: DFE H1 value for Even sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	***RX H1 Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	***RX H1 Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	***RX H1 Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A00A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A00B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A00C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A00D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A00E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A00F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	*RX H1 Odd Sampler Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	***RX H1 Odd Sampler Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_H1_ODD_PL
Address	8000A0110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	RX_H1_ODD_SAMP1: DFE H1 value for Odd sampler 1.
56	RO	constant=0b0
57:63	RWX	RX_H1_ODD_SAMP0: DFE H1 value for Odd sampler 0.

Register Name	***RX Per-Lane PRBS Mode Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Bits	SCOM	Field Mnemonic: Description
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B00A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B00B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B00C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B00D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B00E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B00F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX Per-Lane PRBS Mode Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_PRBS_MODE_PL
Address	8000B0110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_PRBS_TAP_ID: Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with tx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C80A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C80B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C80C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C80D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	***RX FIFO Deskew Status/error Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C80E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	***RX FIFO Deskew Status/error Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C80F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	***RX FIFO Deskew Status/error Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX FIFO Deskew Status/error Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DESKEW_STAT_PL
Address	8000C8110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BLOCK_LOCK: Deskew Step block lock not established--lane marked bad.
49	RWX	RX_BAD_SKEW: Deskew Step skew value not detected--lane marked bad.
50	RWX	RX_BAD_DESKEW: Deskew Step deskew value.
51:63	RO	constant=0b0000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.

Bits	SCOM	Field Mnemonic: Description
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	***RX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	***RX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D00A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	***RX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D00B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D00C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D00D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D00E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D00F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	***RX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	***RX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_PL
Address	8000D0110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
50:63	RO	constant=0b00000000000000

Register Name	***RX Per-Lane FIR Error Source-Isolation Mask Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D80A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D80B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D80C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D80D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D80E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D80F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_MASK_PL
Address	8000D8110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pl errors.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E00A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E00B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E00C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E00D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E00E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E00F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_FIR_ERROR_INJECT_PL
Address	8000E0110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_PL_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-lane RX Registers.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E80A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E80B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E80C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E80D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX SLS Settings Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E80E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	***RX SLS Settings Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E80F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	***RX SLS Settings Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	***RX SLS Settings Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SLS_PL
Address	8000E8110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_LANE_SEL: Selects which lane to receive SLS Commands and Recalibration Data on.
49	RWX	RX_9TH_PATTERN_EN: Sets RX Descrabmler to use calibration or 9th Scramble Pattern.
50:63	RO	constant=0b00000000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	***RX Wiretest Status Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) +1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F00A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F00B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F00C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F00D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F00E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F00F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.

Bits	SCOM	Field Mnemonic: Description
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Wiretest Status Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_WT_STATUS_PL
Address	8000F0110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_LANE_DISABLED: Wiretest has disabled this lane.
49	RWX	RX_WT_LANE_INVERTED: Wiretest lane inverted (or _n and _p swapped) 0--not inverted if rx_wt_lane_bad_code = 000 1--inverted if rx_wt_lane_bad_code = 000. See rx_wt_lane_bad_code descriptions for meaning if rx_wt_lane_bad_code not = 000.
50:52	RWX	RX_WT_LANE_BAD_CODE: Wiretest Lane Bad code Concatenate rx_wt_lane_inverted with rx_wt_lane_bad_code to get a full status: 0000--GOOD LANE--not inverted (EDI and EI-4) 0001--BAD LANE--N leg stuck at 1--not inverted (EDI-only) 0010--BAD LANE--N leg stuck at 0--not inverted (EDI-only) 0011--BAD LANE--P leg stuck at 1--not inverted (EDI-only) 0100--BAD LANE--P leg stuck at 0--not inverted (EDI-only) 0101--BAD LANE--N/(P) leg floating if (NOT) inverted (EDI-only) 0110--BAD LANE--P/(N) leg floating if (NOT) inverted (EDI-only) 0111--BAD LANE--P and N legs stuck at same value, 0 or 1 (EDI only) 1000--GOOD LANE--inverted (EDI and EI-4) 1001--BAD LANE--N leg stuck at 1--inverted (EDI only) 1010--BAD LANE--N leg stuck at 0--inverted (EDI only) 1011--BAD LANE--P leg stuck at 1--inverted (EDI only) 1100--BAD LANE--P leg stuck at 0--inverted (EDI only) 1101--BAD LANE--P leg stuck at 0--N leg stuck at 1 (EDI and EI-4) 1110--BAD LANE--P leg stuck at 1--N leg stuck at 0 (EDI and EI-4) 1111--BAD LANE--Unknown reason--inversion undetermined (EDI and EI-4).
53:63	RO	constant=0b00000000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.

Bits	SCOM	Field Mnemonic: Description
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Servo Operation Command And Control***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Servo Operation Command And Control***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Servo Operation Command And Control***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Servo Operation Command And Control***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Servo Operation Command And Control***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	8001200A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	8001200B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	8001200C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	8001200D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	8001200E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	8001200F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	*RX Servo Operation Command And Control*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.

Bits	SCOM	Field Mnemonic: Description
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Servo Operation Command And Control***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_SERVO_CNTL_PL
Address	800120110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_SERVO_OP_DONE: Servo Op completed.
49	ROX	Reserved field. (Access type is rx_servo_op_all_done_b_ro_signal)
50:54	RWX	RX_SERVO_OP: Servo Op completed.
55	RWX	RX_SCOPE_EN: Set this bit to enable per lane scope mode.
56:63	RO	constant=0b00000000

Register Name	***RX Dfe Clock Adjust Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	***RX Dfe Clock Adjust Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.

Bits	SCOM	Field Mnemonic: Description
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	8001500A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	8001500B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	8001500C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	8001500D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	8001500E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	*RX Dfe Clock Adjust Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	8001500F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	***RX Dfe Clock Adjust Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	***RX Dfe Clock Adjust Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_DFE_CLKADJ_PL
Address	800150110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_DFE_CLKADJ: Tweak value for the clock offset when doing DFE calibration.
52:63	RO	constant=0b000000000000

Register Name	***RX Trace Per Lane Settings***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_TRACE_PL
Address	8001580A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_TRACE_PL
Address	8001580B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_TRACE_PL
Address	8001580C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_TRACE_PL
Address	8001580D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_TRACE_PL
Address	8001580E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_TRACE_PL
Address	8001580F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Per Lane Settings*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_TRACE_PL
Address	800158110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_LN_TRC_EN: Enable tracing of this lane..
49:63	RO	constant=0b000000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	***RX Eye Optimization Error Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	***RX Eye Optimization Error Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.

Bits	SCOM	Field Mnemonic: Description
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	8001680A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	8001680B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	8001680C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	8001680D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.SLICE#2.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	8001680E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.SLICE#3.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	8001680F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#0.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.

Bits	SCOM	Field Mnemonic: Description
52:63	RO	constant=0b000000000000

Register Name	*RX Eye Optimization Error Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.SLICE#1.RD.RX_BIT_REGS.RX_EYE_OPT_STAT_PL
Address	800168110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_EYE_OPT_BER: Eye opt Step failed BER test--lane marked bad.
49	RWX	RX_BAD_EYE_OPT_WIDTH: Eye opt Step failed width test--lane marked bad.
50	RWX	RX_BAD_EYE_OPT_HEIGHT: Eye opt Step failed height test--lane marked bad.
51	RWX	RX_BAD_EYE_OPT_DDC: Eye opt Step failed dynamic data centering--lane marked bad.
52:63	RO	constant=0b000000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11

Bits	SCOM	Field Mnemonic: Description
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL
Address	8004040A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL
Address	8004040B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL
Address	8004040C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_PL
Address	8004040D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11

Bits	SCOM	Field Mnemonic: Description
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL
Address	8004040E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL
Address	8004040F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11

Bits	SCOM	Field Mnemonic: Description
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1

Bits	SCOM	Field Mnemonic: Description
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	*TX Lane Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Lane Mode Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_PL
Address	800404170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_LANE_PDWN: Used to drive inhibit (tristate) and fully power down a lane independent of the logical lane disable. This control is independent from the per-group logical lane disable settings (tx_lane_disable_vec*) in order to allow for flexibility. Note that this control routes through the boundary scan logic, which has dominance. Also note that per-group registers tx_lane_disabled_vec_0_15 and tx_lane_disabled_vec_16_31 are used to logically disable a lane with respect to the training, recalibration, and repair machines so both this per-lane and the per-group registers need to be set in order to logically disable and powerdown a lane. Note that this per-lane register is adjusted for lane swizzling automatically in HW but it is NOT adjusted automatically in HW when in the MSB-LSB swap mode so the eRepair procedure needs to take care to power down the correct lane when in this mode. 0b0 = Lane Powered Up (default) 0b1 = Lane Drive Inhibited (Tristated) and Powered Down. The lane_disable_vec_* per-group registers configure the state machine but do not automatically power down or tristate the lanes. DEBUG NOTE: You have to account for swizzle when correlating the per-pack latch to the per-group latch setting. Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	TX_LANE_INVERT: Used to invert the polarity of a lane. 0b0 = Normal Lane Polarity (default) 0b1 = Lane Inverted. Values: NORMAL=>0b0 INVERTED=>0b1
50:51	RWX	TX_LANE_QUIESCE_P: Used to force the output of the positive differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_LANE_QUIESCE_N: Used to force the output of the negative differential leg of a lane to a particular value. 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output. Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_LANE_SCRAMBLE_DISABLE: Used to disable the TX scrambler on a specific lane or all lanes by using a per-lane/per-group global write.
55:63	RO	constant=0b000000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	8004140A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	8004140B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	8004140C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	8004140D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	8004140E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	8004140F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	***TX Per-Lane Spare Mode Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.

Bits	SCOM	Field Mnemonic: Description
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX Per-Lane Spare Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_SPARE_MODE_PL
Address	800414170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_SPARE_MODE_0: Per-lane spare mode latch.
49	RWX	TX_PL_SPARE_MODE_1: Per-lane spare mode latch.
50	RWX	TX_PL_SPARE_MODE_2: Per-lane spare mode latch.
51	RWX	TX_PL_SPARE_MODE_3: Per-lane spare mode latch.
52	RWX	TX_PL_SPARE_MODE_4: Per-lane spare mode latch.
53	RWX	TX_PL_SPARE_MODE_5: Per-lane spare mode latch.
54	RWX	TX_PL_SPARE_MODE_6: Per-lane spare mode latch.
55	RWX	TX_PL_SPARE_MODE_7: Per-lane spare mode latch.
56:63	RO	constant=0b00000000

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C0A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C0B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C0C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C0D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C0E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C0F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX BIST Status Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_BIST_STAT_PL
Address	80042C170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_LANE_BIST_ERR: Indicates TXBIST has found an error.. JGR 0b0 = No Error 0b1 = An error has been found during TXBIST. Values: NO_ERROR=>0b0 ERROR=>0b1
49	ROX	Reserved field. (Access type is tx_lane_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
50:63	RO	constant=0b00000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	8004340A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	8004340B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	8004340C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	8004340D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	8004340E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	8004340F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Per-Lane PRBS Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_PRBS_MODE_PL
Address	800434170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	TX_PRBS_TAP_ID: TX Per-Lane PRBS Tap Selector. Used to specify the tap-point for each lanes PRBS scramble pattern. This must be set consistent with rx_prbs_tap_id. 0b000 = PRBS tap point A 0b001 = PRBS tap point B 0b010 = PRBS tap point C 0b011 = PRBS tap point D 0b100 = PRBS tap point E 0b101 = PRBS tap point F 0b110 = PRBS tap point G 0b111 = PRBS tap point H Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111
51:63	RO	constant=0b0000000000000 Values: PATTERN_A=>0b000 PATTERN_B=>0b001 PATTERN_C=>0b010 PATTERN_D=>0b011 PATTERN_E=>0b100 PATTERN_F=>0b101 PATTERN_G=>0b110 PATTERN_H=>0b111

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C0A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C0B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C0C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C0D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C0E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C0F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	*TX Data Control Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Data Control Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_DATA_CNTL_GCRMSG_PL
Address	80043C170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	TX_DRV_DATA_PATTERN_GCRMSG: GCR Message: TX Per Data Lane Drive Patterns. 0b0000 = Drive All 0s Pattern 0b0001 = Drive Wiretest Pattern 0b0010 = Drive All 1s Pattern 0b0011 = Drive Deskew Pattern A 0b0100 = Drive Deskew Pattern B 0b0101 = PRBS Full Speed Scramble Pattern (see tx_prbs_tap_id) (0b0110 = PRBS Reduced Density Scramble Pattern (see tx_prbs_tap_id and tx_reduced_scramble_mode) 0b0111 = PRBS calibration or 9th pattern 0b1000 = EI-3 Busy IAP Pattern (EI4 only) 0b1001 = Unused 0b1010 = Drives TDR Pulse-Square waves 0b1011 = Drives 20-bit K28.5 pattern - padded to 32 bits 0b1100 = Unused 0b1101 = Unused 0b1110 = Unused 0b1111 = Unused Values: DRV_0S=>0b0000 DRV_WT=>0b0001 DRV_1S=>0b0010 DRV_DESKEW_A=>0b0011 DRV_DESKEW_B=>0b0100 DRV_FULL_PRBS=>0b0101 DRV_RED_PRBS=>0b0110 DRV_CAL_PRBS=>0b0111 DRV_EI3_IAP=>0b1000 UNUSED_E=>0b1001 TDR_SQUARE_WAVE=>0b1010 K28_5=>0b1011 UNUSED_A=>0b1100 UNUSED_B=>0b1101 UNUSED_C=>0b1110 UNUSED_D=>0b1111

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_DRV_FUNC_DATA_GCRMSG: GCR Message: Functional Data. 0b0 = Functional data gated 0b1 = Send functional data Values: FUNC_GATED=>0b0 SND_FUNC=>0b1
53	RWX	TX_SLS_LANE_SEL_GCRMSG: GCR Message: SLS Commands & Recalibration. 0b0 = SLS commands & Recalibration data gated 0b1 = Send SLS command or Recalibration Data Values: SLS_GATED=>0b0 SND_SLS=>0b1
54:63	RO	constant=0b0000000000 Values: SLS_GATED=>0b0 SND_SLS=>0b1

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL
Address	8004540A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL
Address	8004540B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL
Address	8004540C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_PL
Address	8004540D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL
Address	8004540E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL
Address	8004540F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_PL
Address	800454170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C0A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C0B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C0C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C0D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C0E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C0F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	***TX Per-Lane FIR Error Mask Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Mask Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_MASK_PL
Address	80045C170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for all per-lane register or per-lane state machine parity errors.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004640A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004640B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004640C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004640D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004640E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	8004640F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane FIR Error Injection Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_FIR_ERROR_INJECT_PL
Address	800464170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PL_FIR_ERR_INJ: IOTK ALIAS: for tx_fir_error_inject_pl register.
49:63	RO	constant=0b000000000000000

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***TX Per-Lane Fast-Clocked Mode Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C0A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C0B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C0C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C0D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C0E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C0F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)

Bits	SCOM	Field Mnemonic: Description
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***TX Per-Lane Fast-Clocked Mode Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Per-Lane Fast-Clocked Mode Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_MODE_FAST_PL
Address	80046C170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	NCX	Reserved field. (Access type is tx_err_inject_wo_pulse_fast_signal)
52	RWX	TX_ERR_INJ_A_ENABLE: Control to enable the random bit error injection pattern A for this lane.(default) 0b0 = Pattern A error injection is masked for this lane. 0b1 = Pattern A error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
53	RWX	TX_ERR_INJ_B_ENABLE: Control to enable the random bit error injection pattern B for this lane.(default) 0b0 = Pattern B error injection is masked for this lane. 0b1 = Pattern B error injection is enabled for this lane. Values: DISABLED=>0b0 ENABLED=>0b1
54:63	RO	constant=0b0000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C010201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C020201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C030201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C040201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C050201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C060201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C070201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C080201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C090201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C0A0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C0B0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C0C0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C0D0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C0E0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C0F0201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C100201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C110201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C120201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#0.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C130201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#1.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C140201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#2.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C150201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#3.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C160201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*TX Control Register Via GCR Messages*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.SLICE#4.TD.TX_BIT_REGS.TX_CNTL_GCRMSG_PL
Address	80047C170201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_PDWN_LITE_GCRMSG: GCR Message: When set, gates TX data path (post FIFO) to 0s on unused spare lanes when not being recalibrated..
49:63	RO	constant=0b000000000000000

Register Name	*RX Per-Group Clk Mode Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_CLK_MODE_PG
Address	800800000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_CLK_PDWN: Used to disable the rx clock and put it into a low power state. 0b0 = Clk Enabled (default) 0b1 = Clk Disabled Values: ENABLED=>0b0 DISABLED=>0b1
49	RWX	RX_CLK_INVERT: Used to invert the polarity of the clock. 0b0 = Normal Clk Polarity (default) 0b1 = Clk Inverted Values: NORMAL=>0b0 INVERTED=>0b1
50:63	RO	constant=0b00000000000000 Values: NORMAL=>0b0 INVERTED=>0b1

Register Name	***RX Per-Group Spare Mode Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SPARE_MODE_PG
Address	800808000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_SPARE_MODE_0: Per-group spare mode latch.
49	RWX	RX_PG_SPARE_MODE_1: Per-group spare mode latch.
50	RWX	RX_PG_SPARE_MODE_2: Per-group spare mode latch.
51	RWX	RX_PG_SPARE_MODE_3: Per-group spare mode latch.
52	RWX	RX_PG_SPARE_MODE_4: Per-group spare mode latch.
53:55	RWX	RX_SLS_EXTEND_SEL: How Long to extend sending of the TX SLS command (that is, delay the gcr_wrt_done to the sending SM).. (Times based on EDI slow clk of 833ps). 0b000 = 0.833ns 0b001 = 53.3ns 0b010 = 106.6ns 0b011 = 213.2ns 0b100 = 426.5ns 0b101 = 853.0ns 0b110 = 1.7us 0b111 = 3.4us Values: TAP1=>0b000 TAP2=>0b001 TAP3=>0b010 TAP4=>0b011 TAP5=>0b100 TAP6=>0b101 TAP7=>0b110 TAProcessor=>0b111

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000 Values: TAP1=>0b000 TAP2=>0b001 TAP3=>0b010 TAP4=>0b011 TAP5=>0b100 TAP6=>0b101 TAP7=>0b110 TAProcessor=>0b111

Register Name	*RX Trace/State Stop Control/status/ MSB Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL2_REGS.RX_STOP_CNTL_STAT_PG
Address	800810000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_STOP_STATE_ENABLE: Enable State machine stop of address.
49	ROX	Reserved field. (Access type is rx_state_stopped_ro_signal)
50	NCX	Reserved field. (Access type is rx_resume_from_stop_wo_pulse_slow_signal)
51:55	RO	constant=0b00000
56:59	RWX	RX_STOP_ADDR_MSB: Stop address Most-significant four bits 0 to 3.
60:63	RWX	RX_STOP_MASK_MSB: Stop mask Most-significant four bits 0 to 3.

Register Name	*RX Mode Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_MODE_PG
Address	800818000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_MASTER_MODE: Master Mode. Used to set a chip bus as the master side of the interface. The master side of the interface is where training is kicked off and coordinated in the logic.. 0b0 = Slave 0b1 = Master Values: SLAVE=>0b0 MASTER=>0b1

Bits	SCOM	Field Mnemonic: Description
49	RWX	RX_DISABLE_FENCE_RESET: Set to disable clearing of the RX and TX fence controls at the end of training. 0b0 = Clear the fence bit (default) 0b1 = Leave the fence in its current state Values: ENABLE=>0b0 DISABLE=>0b1
50	RWX	RX_PDWN_LITE_DISABLE: Disables the power down lite feature of unused spare lanes (generally should match tx_pdwn_lite_disable).
51	RWX	RX_USE_SLS_AS_SPR: Determines whether the RX SLS lane can be used as a spare lane on the bus to repair bad lanes (NOTE: if yes, recal is disabled once the SLS lane has been used as a spare lane.). (NOTE: applies to TX side as well).
52:63	RO	constant=0b000000000000

Register Name	***RX Trace/State Stop Address 4-19 Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL2_REGS.RX_STOP_ADDR_LSB_PG
Address	800838000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RWX	RX_STOP_ADDR_LSB: Stop address least-significant 16 bits 4 to 19.

Register Name	***RX Trace/State Stop Mask 4-19 Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL2_REGS.RX_STOP_MASK_LSB_PG
Address	800840000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RWX	RX_STOP_MASK_LSB: Stop mask least-significant 16 bits 4 to 19.

Register Name	***RX Reset Control Action Register (RCAR)***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RESET_ACT_PG
Address	800848000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	NCX	Reserved field. (Access type is rx_reset_cfg_ena_wo_pulse_slow_signal)

Bits	SCOM	Field Mnemonic: Description
49:61	RO	constant=0b0000000000000
62	RWX	RX_CLR_PAR_ERRS: Clear All RX Parity Error Latches. Toggle this field 0->1->0 to clear all RX parity error latches.
63	RWX	RX_FIR_RESET: FIR Reset. Toggle this field 0->1->0 to reset all RX FIR related latches, including the isolation and parity error latches.

Register Name	*RX Clock Group Identification 1 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_ID1_PG
Address	800850000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_BUS_ID: This field is used to programmably set the bus number that a clkgrp belongs to.. DMB
54	RO	constant=0b0
55:60	RWX	RX_GROUP_ID: This field is used to programmably set the clock group number within a bus.. DMB
61:63	RO	constant=0b000

Register Name	*RX Clock Group Identification 2 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_ID2_PG
Address	800858000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RWX	RX_LAST_GROUP_ID: This field is used to programmably set the last clock group number within a bus.. DMB
54:63	RO	constant=0b0000000000

Register Name	*RX Clock Group Identification 3 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_ID3_PG
Address	800860000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RWX	RX_START_LANE_ID: This field is used to programmably set the first lane position in the group but relative to the bus.. DMB
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RWX	RX_END_LANE_ID: This field is used to programmably set the last lane position in the group but relative to the bus.. DMB

Register Name	*RX Minikerf Control Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_MINIKERF_PG
Address	800868000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_MINIKERF: RX Minikerf control bits.. Bits (3:13) are only used when (0:2)=001. Bits (14:15) are spare. (0:2) is level 1 steering, . (0:2)=000 - reserved . (0:2)=001 - use bits (3:5) level 2 steering, (6:13) dac controls, (14:15) spare . (0:2)=010 - impedance control termref_mk_probe_ana(0:1) only for the memory buffer. All other buses use the tx_minikerf_pb. (0:2)=011 - rx cleanup pll atst on pad_io_p. Pad_io_n=0. (0:2)=100 - reserved . (0:2)=101 - reserved.(0:2)=110 - rx cleanup pll clk on c4 pads.(0:2)=111 - reserved. SMC

Register Name	*Dynamic Repair Testfloor/Debug Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_DEBUG2_PG
Address	800870000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BAD_BUS_LANE_ERR_CNTR_DIS_CLR: Disable clearing of the bad bus lane error counter (aka counter1) when the next CRC/ECC error comes in on a new lane.
49:55	ROX	Reserved field. (Access type is rx_bad_bus_lane_err_cntr_ro_signal)
56	RO	constant=0b0
57:63	ROX	Reserved field. (Access type is rx_last_bad_bus_lane_ro_signal)

Register Name	*RX Spare Lane Signaling Mode Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SLS_MODE_PG
Address	800878000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_DISABLE: Disables receiving & decoding of SLS commands.

Bits	SCOM	Field Mnemonic: Description
49	RWX	TX_SLS_DISABLE: If set, the SLS command being sent will always just be a NOP. To truly disable the full SLS logic path, also do some combination of the following (depending on what exactly you are trying to do): set the rx_sls_disable, manually override the tx_snd_sls_cmd_gcrmsg per pack registers (if you do not also disable the various sending SMs, though, this will eventually get overwritten), set tx_sls_lane_val_gcrmsg to 0 (if there is no valid TX SLS lane, no SLS command will get sent on it), and/or disable the recal, repair, recovery SMs (rx_dyn_recal_suspend, rx_dyn_rpr_disable, rx_sls_rcvy_disable) that initiate the sending of SLS commands.
50:51	RWX	RX_SLS_CNTR_TAP_PTS: How Long the SLS RX Command Needs to be Stable for.. Need to make sure this scales with tx_dyn_recal_interval_timeout & status_rpt_timeout. 0b00 = EDI - 16 c8 clks; EI4 - 32 c4 clks 0b01 = EDI - 32 c8 clks; EI4 - 64 c4 clks 0b10 = EDI - 64 c8 clks; EI4 - 128 c4 clks 0b11 = EDI - 128 c8 clks; EI4 - 256 c4 clks Values: TAP1=>0b00 TAP2=>0b01 TAP3=>0b10 TAP4=>0b11
52:53	RWX	RX_NONSLS_CNTR_TAP_PTS: How Long a Non-SLS RX Command Needs to be Stable for (to know we have switched from an SLS command to data).. Need to make sure this scales with tx_dyn_recal_interval_timeout & status_rpt_timeout. 0b00 = EDI - 32 c8 clks; EI4 - 64 c4 clks 0b01 = EDI - 64 c8 clks; EI4 - 128 c4 clks 0b10 = EDI - 128 c8 clks; EI4 - 256 c4 clks 0b11 = EDI - 256 c8 clks; EI4 - 512 c4 clks Values: TAP1=>0b00 TAP2=>0b01 TAP3=>0b10 TAP4=>0b11
54	RWX	RX_SLS_ERR_CHK_RUN: Run SLS error check counter.
55:63	RO	constant=0b000000000

Register Name	***RX Training State Start Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TRAINING_START_PG
Address	800880000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_START_WIRETEST: When this register is written to a 1 the training state machine will run the wiretest portion of the training states..
49	RWX	RX_START_DESKEW: When this register is written to a 1 the training state machine will run the deskew portion of the training states..
50	RWX	RX_START_EYE_OPT: When this register is written to a 1 the training state machine will run the data eye optimization portion of the training states..
51	RWX	RX_START_REPAIR: When this register is written to a 1 the training state machine will run the static lane repair portion of the training states..
52	RWX	RX_START_FUNC_MODE: When this register is written to a 1 the training state machine will run the transition to functional data portion of the training states..

Bits	SCOM	Field Mnemonic: Description
53	RWX	RX_START_BIST: Set bit to run BIST and perform the required TX FIFO init, RX CU PLL lock, RX FIFO init, and offset calibration in the BIST helper state machine. The RX BIST state machine is enabled through a GCR message to the rx_bist_en register field.JGR 0b0 = Idle 0b1 = Start RX BIST Values: IDLE=>0b0 EN_RX_BIST=>0b1
54	RWX	RX_START_OFFSET_CAL: Set bit to run offset cal and the required TX FIFO init, RX CU PLL lock, and RX FIFO init through the BIST helper state machine.JGR 0b0 = Idle 0b1 = Start Offset Cal Values: IDLE=>0b0 OCAL=>0b1
55	RWX	RX_START_WT_BYPASS: Set bit to run wiretest bypass and the required TX FIFO initialization through the BIST helper state machine.JGR 0b0 = Idle 0b1 = Start Wiretest Bypass Values: IDLE=>0b0 WTBYP=>0b1
56:63	RO	constant=0b00000000 Values: IDLE=>0b0 WTBYP=>0b1

Register Name	***RX Training State Status Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TRAINING_STATUS_PG
Address	800888000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WIRETEST_DONE: When this bit is read as a 1, the wiretest training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state..
49	RWX	RX_DESKEW_DONE: When this bit is read as a 1, the deskew training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state..
50	RWX	RX_EYE_OPT_DONE: When this bit is read as a 1, the eye optimization training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state..
51	RWX	RX_REPAIR_DONE: When this bit is read as a 1, the static lane repair training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state..
52	RWX	RX_FUNC_MODE_DONE: When this bit is read as a 1, the transition to functional data training state has completed. Check the corresponding rx_ts_*_failed register field for the pass/fail status of this training state..
53	RWX	RX_BIST_STARTED: When this bit is read as a 1, the RX BIST helper initializations have completed and a GCR enable message has been sent to RX BIST.JGR
54	RWX	RX_OFFSET_CAL_DONE: When this bit is read as a 1, offset cal has completed.JGR
55	RWX	RX_WT_BYPASS_DONE: When this bit is read as a 1, wiretest bypass has completed.JGR

Bits	SCOM	Field Mnemonic: Description
56	RWX	RX_WIRETEST_FAILED: When this bit is read as a 1, the wiretest training state encountered an error..
57	RWX	RX_DESKEW_FAILED: When this bit is read as a 1, the deskew training state encountered an error..
58	RWX	RX_EYE_OPT_FAILED: When this bit is read as a 1, the eye optimization training state encountered an error..
59	RWX	RX_REPAIR_FAILED: When this bit is read as a 1, the static lane repair training state encountered an error..
60	RWX	RX_FUNC_MODE_FAILED: When this bit is read as a 1, the transition to functional data training state encountered an error..
61	RWX	RX_START_BIST_FAILED: When this bit is read as a 1, the RX CU PLL failed to lock and BIST was not started. (This bit is set along with rx_wt_bypass_failed and rx_offset_cal_failed). JGR
62	RWX	RX_OFFSET_CAL_FAILED: When this bit is read as a 1, the RX CU PLL failed to lock and offset cal was not performed. (This bit is set along with rx_wt_bypass_failed and rx_start_bist_failed). JGR
63	RWX	RX_WT_BYPASS_FAILED: When this bit is read as a 1, the RX CU PLL failed to lock. Wiretest bypass did not complete. (This bit is set along with rx_offset_cal_failed and rx_start_bist_failed). JGR

Register Name	***RX Recal Status Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RECAL_STATUS_PG
Address	800890000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	RX_RECAL_STATUS: NO LONGER USED--REMOVE for DD2 design.

Register Name	***RX Timeout Select Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TIMEOUT_SEL_PG
Address	800898000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_SLS_TIMEOUT_SEL: Selects Spare Lane Signalling Timeout value (how long to wait for a SLS handshake command). Note: value needs to be larger than tx_dyn_recal_interval_timeout_sel when doing Recal Aborts. 0b000 = 6.8us very small value for sim only 0b001 = 54.6us 0b010 = 109.2us 0b011 = 218.4us 0b100 = 436.7us 0b101 = 873.5us 0b110 = 28.0ms 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:53	RWX	RX_DS_BL_TIMEOUT_SEL: Selects Deskew Block Lock Timeout value. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
54:56	RWX	RX_CL_TIMEOUT_SEL: Selects Clock Lock Timeout value. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_WT_TIMEOUT_SEL: Selects Wiretest Timeout value. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
60:62	RWX	RX_DS_TIMEOUT_SEL: Selects Deskew Timeout value. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
63	RO	constant=0b0 Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Register Name	*RX FIFO Mode Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIFO_MODE_PG
Address	8008A0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_FIFO_INITIAL_L2U_DLY: RX FIFO Initial Load to Unload Delay. For setting X, the latency is 4*X to 4*X+4 UI. Default is 16-20 UI.
52:55	RWX	RX_FIFO_FINAL_L2U_DLY: RX FIFO Final Load to Unload Delay. For setting X, the latency is 4*X to 4*X+4 UI. Default is 8-12 UI.
56:59	RWX	RX_FIFO_MAX_DESKEW: NO LONGER USED--REMOVE for DD2 design.
60:61	RWX	RX_FIFO_FINAL_L2U_MIN_ERR_THRESH: RX FIFO error threshold used to qualify the minimum load to unload delay as bad, which is used as the point of reference for adjusting to the final load to unload delay. Note that the errors are accumulated across the entire clock group for a length of time selected by rx_eo_final_l2u_timeout_sel. 0b00 = 8 errors 0b01 = 16 errors 0b10 = 128 errors 0b11 = 255 errors Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
62:63	RO	constant=0b00 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***RX Per-Group FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR1_PG
Address	8008D0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:61	RWX	RX_PG_FIR1_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-group logic.
62	RO	constant=0b0
63	RWX	RX_PL_FIR_ERR: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.

Register Name	***RX Per-Group FIR Error Source-Isolation Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR2_PG
Address	8008D8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RWX	RX_PG_FIR2_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-group logic.
55:63	RO	constant=0b000000000

Register Name	*RX Per-Group FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR1_MASK_PG
Address	8008E0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:61	RWX	RX_PG_FIR1_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir1_pg errors.
62	RO	constant=0b0
63	RWX	RX_PL_FIR_ERR_MASK: IOTK ALIAS: FIR mask for per-lane register parity errors.

Register Name	*RX Per-Group FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR2_MASK_PG
Address	8008E8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RWX	RX_PG_FIR2_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir2_pg errors.
55:63	RO	constant=0b000000000

Register Name	*RX Per-Group FIR Error Injection Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR1_ERROR_INJECT_PG
Address	8008F0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:61	RWX	RX_PG_FIR1_ERR_INJ: IOTK ALIAS: RX Per-Group Parity Error Injection. Allows injection of non-destructive parity errors in either register or statemachine latch banks. The register or state value is not affected.
62:63	RO	constant=0b00

Register Name	*RX Per-Group FIR Error Injection Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR2_ERROR_INJECT_PG
Address	8008F8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_PG_FIR2_ERR_INJ: IOTK ALIAS: RX Per-Group Parity Error Injection. Allows injection of non-destructive parity errors in either register or statemachine latch banks. The register or state value is not affected.
55:63	RO	constant=0b000000000

Register Name	*RX Per-Group Training FIR Error Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR_TRAINING_PG
Address	800900000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_PG_FIR_TRAINING_ERROR: This field is now defunct and is permanently masked in the rx_fir_training_mask_pg FIR isolation register.
49	RWX	RX_PG_FIR_STATIC_SPARE_DEPLOYED: A spare lane has been deployed during training to heal a lane that was detected as bad. rx_Static_Spare_Deployed (SSD) will be set after the repair training step if during training either wiretest, deskew, eyeopt or repair has detected one or more bad lanes have been detected. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lane(s) were healed and the rx_bad_lane.
50	RWX	RX_PG_FIR_STATIC_MAX_SPARES_EXCEEDED: A lane has been detected as bad during training but there are no spare lanes available to heal it. THIS FIR WILL NOT BE SET UNTIL THE REPAIR TRAINING STEP HAS BEEN RUN. THIS IS A CATASTROPHIC FAILURE FOR THE BUS WHEN IN MISSION MODE BUT ALL TRAINING STEPS WILL STILL BE RUN ON WHATEVER GOOD LANES THERE ARE. rx_static_max_spares_exceeded will be set if wiretest, deskew, eyeopt or repair find the excessive number of bad lanes.
51	RWX	RX_PG_FIR_DYNAMIC_REPAIR_ERROR: A Dynamic Repair error has occurred. The Recal Error FFDC registers should be read to help isolate to a particular piece of logic.
52	RWX	RX_PG_FIR_DYNAMIC_SPARE_DEPLOYED: A spare lane has been deployed by ECC/CRC logic to heal a lane that was detected as bad. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lane(s) were healed.
53	RWX	RX_PG_FIR_DYNAMIC_MAX_SPARES_EXCEEDED: A lane has been detected as bad by ECC/CRC logic but there are no spare lanes to heal it. THIS IS A CATASTROPHIC FAILURE FOR THE BUS.
54	RWX	RX_PG_FIR_RECAL_ERROR: A Recalibration Error has occurred. The Recal Error FFDC registers should be read to help isolate to a particular piece of logic.
55	RWX	RX_PG_FIR_RECAL_SPARE_DEPLOYED: A spare lane has been deployed during Recal to heal a lane that was detected as bad. The rx_bad_lane_enc_gcrmsg_pg register can be read to isolate which lane(s) were healed.
56	RWX	RX_PG_FIR_RECAL_MAX_SPARES_EXCEEDED: A lane has been detected as bad during Recal but there are no spare lanes to heal it. THIS IS A CATASTROPHIC FAILURE FOR THE BUS.
57	RWX	RX_PG_FIR_TOO_MANY_BUS_ERRORS: More than one lane has been detected as having too many errors during functional operation. THIS IS A CATASTROPHIC FAILURE FOR THE BUS.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*RX Per-Group Training FIR Error Mask Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FIR_TRAINING_MASK_PG
Address	800908000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_PG_FIR_TRAINING_ERROR_MASK: FIR mask for rx_pg_fir_training_error.
49	RWX	RX_PG_FIR_STATIC_SPARE_DEPLOYED_MASK: FIR mask for rx_pg_fir_static_spare_deployed.
50	RWX	RX_PG_FIR_STATIC_MAX_SPARES_EXCEEDED_MASK: FIR mask for rx_pg_fir_static_max_spares_exceeded.
51	RWX	RX_PG_FIR_DYNAMIC_REPAIR_ERROR_MASK: FIR mask for rx_pg_fir_dynamic_repair_error.
52	RWX	RX_PG_FIR_DYNAMIC_SPARE_DEPLOYED_MASK: FIR mask for rx_pg_fir_dynamic_spare_deployed.
53	RWX	RX_PG_FIR_DYNAMIC_MAX_SPARES_EXCEEDED_MASK: FIR mask for rx_pg_fir_dynamic_max_spares_exceeded.
54	RWX	RX_PG_FIR_RECAL_ERROR_MASK: FIR mask for rx_pg_fir_recal_error.
55	RWX	RX_PG_FIR_RECAL_SPARE_DEPLOYED_MASK: FIR mask for rx_pg_fir_recal_spare_deployed.
56	RWX	RX_PG_FIR_RECAL_MAX_SPARES_EXCEEDED_MASK: FIR mask for rx_pg_fir_recal_max_spares_exceeded.
57	RWX	RX_PG_FIR_TOO_MANY_BUS_ERRORS_MASK: FIR mask for rx_pg_fir_too_many_bus_errors.
58:63	RO	constant=0b000000

Register Name	*RX Timeout Select Register 1*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TIMEOUT_SEL1_PG
Address	800910000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_EO_OFFSET_TIMEOUT_SEL: Selects Latch offset timeout. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:53	RWX	RX_EO_AMP_TIMEOUT_SEL: Selects Amplitude measurement watchdog timeout. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
54:56	RWX	RX_EO_CTLE_TIMEOUT_SEL: Selects CTLE ajdust watchdog timeout. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
57:59	RWX	RX_EO_H1AP_TIMEOUT_SEL: Selects H1Ap ajdust watchdog timeout. 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
60:62	RWX	RX_EO_DDC_TIMEOUT_SEL: Selects DDC watchdog timeout (EDI ONLY). 0b000 = 64k UI or 6.8us 0b001 = 128k UI or 13.6us 0b010 = 256k UI or 27.3us 0b011 = 1M UI or 109.2us 0b100 = 2M UI or 218.5us 0b101 = 4M UI or 436.9us 0b110 = 8M UI or 873.8us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
63	RWX	RX_EO_FINAL_L2U_TIMEOUT_SEL: Selects Final Load to Unload Delay qualification time per step. 0b0 = 4k UI or 0.425us 0b1 = 64k UI or 6.8us Values: TAP0=>0b0 TAP1=>0b1

Register Name	***RX Bad Lanes 0 To 15 Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_BAD_VEC_0_15_PG
Address	800918000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RWX	RX_LANE_BAD_VEC_0_15: Lanes found bad by HW (status) or method to force lane bad from software (control).to be clear, the bad_lane vector is only updated during training. It will not reflect bad lanes found post training during dynamic repair or dynamic recal. For that, you need to read the [rx,tx]_bad_lane[1,2]_gcrmsg registers. To calculate what you want to know, you need five registers:. rx_bad_lane1_gcrmsg. rx_bad_lane2_gcrmsg. rx_bad_lane_code_gcrmsg. rx_sls_lane_gcrmsg. rx_wtr_max_bad_lanes. In general, if the spares deployed FIR goes on, and the bad_lane_code is a 1, then the newly spared lane resides in the rx_bad_lane1_gcrmsg register. If the spares deployed FIR goes on, and the bad_lane_code is a 2, then the newly spared lane resides in the rx_bad_lane2_gcrmsg register. If the spares deployed FIR goes on, and the bad_lane_code is a 3, then the newly spared lane resides in the rx_sls_lane_gcrmsg register. That might be enough information for what you want to know, trying to keep the answer very general. At the moment, this case where both the spare deployed and max spares exceeded both come on at the same time, is for the EDI where a third bad lane has been found and we have chosen to use the SLS lane as a third spare. EDI normally only has two spare lanes. In that case, I first set the spare deployed FIR as the SLS lane is being used as a third spare. But then a few cycles later, I set the max spares exceeded because I no longer have an SLS lane and cant finish my SLS repair handshake..

Register Name	*RX Bad Lanes 16 To 31 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_BAD_VEC_16_31_PG
Address	800920000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_BAD_VEC_16_31: Lanes found bad by HW (status) or method to force lane bad from software (control)..

Register Name	*RX Lane Disable(d) 0 To 15 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_DISABLED_VEC_0_15_PG
Address	800928000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_DISABLED_VEC_0_15: Lanes disabled by HW (status) or method to force lane to be disabled (save power) from software (control).

Register Name	*RX Lane Disable(d) 16_31 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_DISABLED_VEC_16_31_PG
Address	800930000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RWX	RX_LANE_DISABLED_VEC_16_31: Lanes disabled by HW (status) or method to force lane to be disabled (save power) from software (control).

Register Name	*RX P & N Lanes Swapped 0 To 15 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_SWAPPED_VEC_0_15_PG
Address	800938000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_SWAPPED_VEC_0_15: Wiretest found that the P & N wire legs have been swapped on the lane indicated. Has the effect of basically inverting the signal. Note that this status is invalid if the lane is marked bad.

Register Name	*RX P & N Lanes Swapped 16 To 31 Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_LANE_SWAPPED_VEC_16_31_PG
Address	800940000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_LANE_SWAPPED_VEC_16_31: Wiretest found that the P & N wire legs have been swapped on the lane indicated. Has the effect of basically inverting the signal. Note that this status is invalid if the lane is marked bad.

Register Name	*RX Wiretest Lane Info Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_WIRETEST_LANEINFO_PG
Address	800958000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	ROX	Reserved field. (Access type is rx_wtr_cur_lane_ro_signal)
53:57	RWX	RX_WTR_MAX_BAD_LANES: Wiretest Max Number of Bad Lanes Allowed Per Clk Group.. Also Static Repair, Dynamic Repair & Recal max number of bad lanes per RX bus (NOTE: should match TX side).
58	RO	constant=0b0
59:63	ROX	Reserved field. (Access type is rx_wtr_bad_lane_count_ro_signal)

Register Name	*RX Wiretest GCR Message Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_WIRETEST_GCRMSGS_PG
Address	800960000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_WT_PREV_DONE_GCRMSG: GCR Message: Previous Clk Group Has Completed Wiretest. JFG
49	RWX	RX_WT_ALL_DONE_GCRMSG: GCR Message: All Clk Groups Have Completed Wiretest. JFG
50:63	RO	constant=0b00000000000000

Register Name	*RX Deskew GCR Message Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DESKEW_GCRMSGS_PG
Address	800968000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	RX_DESKEW_SEQ_GCRMSG: GCR Message: RX Deskew Sequencer GCR messages. 0b000 = Indicate prior group deskewed. 0b001 = Indicate all groups deskewed. 0b010 = Indicate prior group completed deskew. 0b011 = Indicate all groups completed deskew. 0b100 = Transmit skew values from prior group. 0b101 = Transmit max skew values to all groups. 0b110 = Unused. 0b111 = No message. Values: DSPREVDESKEWED=>0b000 DSALLDESKEWED=>0b001 DSPREVDONE=>0b010 DSALLDONE=>0b011 DSPREVSKEW=>0b100 DSMAXSKEW=>0b101 UNUSED=>0b110 DSNOMSG=>0b111
51	RO	constant=0b0 Values: DSPREVDESKEWED=>0b000 DSALLDESKEWED=>0b001 DSPREVDONE=>0b010 DSALLDONE=>0b011 DSPREVSKEW=>0b100 DSMAXSKEW=>0b101 UNUSED=>0b110 DSNOMSG=>0b111
52:57	RWX	RX_DESKEW_SKMIN_GCRMSG: GCR Message: Min Skew Value for deskew sequence..
58:63	RWX	RX_DESKEW_SKMAX_GCRMSG: GCR Message: Max Skew Value for deskew sequence..

Register Name	*RX Deskew State Machine Control Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DESKEW_MODE_PG
Address	800978000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RWX	RX_DESKEW_MAX_LIMIT: Maximum Deskewable Skew Fail Threshold .
54:63	RO	constant=0b0000000000

Register Name	*RX Deskew State Machine Status Values*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DESKEW_STATUS_PG
Address	800980000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RWX	RX_DESKEW_MINSKEW_GRP: Deskew Per-Group Raw Skew Min.
54:59	RWX	RX_DESKEW_MAXSKEW_GRP: Deskew Per-Group Raw Skew Max.
60:63	RO	constant=0b0000

Register Name	*RX Bad Lanes Encoded*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_BAD_LANE_ENC_GCRMSG_PG
Address	800988000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RWX	RX_BAD_LANE1_GCRMSG: GCR Message: Encoded bad lane one in relation to the entire RX bus.
55:61	RWX	RX_BAD_LANE2_GCRMSG: GCR Message: Encoded bad lane two in relation to the entire RX bus.
62:63	RWX	RX_BAD_LANE_CODE_GCRMSG: GCR Message: RX Bad Lane Code. 0b00 = Zero Bad Lanes 0b01 = Bad Lane 1 Valid 0b10 = Bad Lanes 1 and 2 Valid 0b11 = 3+ bad lanes Values: 0_BAD_LNS=>0b00 BAD_LN1_VAL=>0b01 BAD_LNS12_VAL=>0b10 3PLUS_BAD_LNS=>0b11

Register Name	*TX Bus Info For RX Ctl Macs*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TX_BUS_INFO_PG
Address	800998000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_TX_BUS_WIDTH: TX Bus Width.
55:61	RWX	RX_RX_BUS_WIDTH: RX Bus Width.
62:63	RO	constant=0b00

Register Name	*RX SLS Lane Encoded*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SLS_LANE_ENC_GCRMSG_PG
Address	8009A0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RWX	RX_SLS_LANE_GCRMSG: GCR Message: Encoded SLS lane in relation to the entire RX bus.
55	RWX	RX_SLS_LANE_VAL_GCRMSG: GCR Message: RX SLS Lane Valid.
56:63	RO	constant=0b00000000

Register Name	*RX Per Group Fence*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_FENCE_PG
Address	8009A8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_FENCE: RX fence bit. 0b0 = Functional data is being driven to nest logic 0b1 = Functional data is gated to zeroes to nest logic. Also indicates that link training not yet complete. Values: UNFENCED=>0b0 FENCED=>0b1
49:63	RO	constant=0b000000000000000 Values: UNFENCED=>0b0 FENCED=>0b1

Register Name	*RX Timeout Select Register 2*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TIMEOUT_SEL2_PG
Address	8009B8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	RX_FUNC_MODE_TIMEOUT_SEL: Selects Functional Mode wait timeout. Note that his should be longer than rx_sls_timeout_sel. 0b000 = 16k UI or 1.7us 0b001 = 128k UI or 13.7us 0b010 = 256k UI or 27.3us 0b011 = 512k UI or 54.6us 0b100 = 1M UI or 109.2us 0b101 = 2M UI or 218.5us 0b110 = 64M UI or 7ms 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:53	RWX	RX_RC_SLOWDOWN_TIMEOUT_SEL: Selects Recal Slowdown timeout. Note that his should be longer than rx_sls_timeout_sel. 0b000 = 0 UI or 0us 0b001 = 128k UI or 13.7us 0b010 = 256k UI or 27.3us 0b011 = 512k UI or 54.6us 0b100 = 1M UI or 109.2us 0b101 = 2M UI or 218.5us 0b110 = 64M UI or 7ms 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
54:55	RWX	RX_PUP_LITE_WAIT_SEL: How long to wait for analog logic to power up an unused spare lane for recal and repair. 0b00 = 833ps (for sim use only) 0b01 = 107ns (default value) 0b10 = 213ns 0b11 = 427ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	*RX Misc Analog Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_MISC_ANALOG_PG
Address	8009C0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RWX	RX_C4_SEL: Select 1 of 4 possible phases for the C4 clock to send along with the data for integration flexibility and tuning for slack into the Rx FIFO.
50	RWX	RX_NEGZ_EN: Turns on a gyrator stage in the CTLE pushing up the high freq corner.
51	RWX	RX_PROT_SPEED_SLCT: TBD (Enable the flux capacitor?)
52:54	RWX	RX_IREF_BC: Bias Code for the Iref macros on the RX side. All eight 3 bit codes enable current out. The cml voltage swings of the output current will vary with this code.
55:63	RO	constant=0b000000000

Register Name	*CRC/ECC Dynamic Repair GCR Message Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_GCRMSG_PG
Address	8009D0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX	RX_DYN_RPR_REQ_GCRMSG: GCR Message: CRC/ECC Tallying logic has a Dynamic Repair Request.
49:55	RWX	RX_DYN_RPR_LANE2RPR_GCRMSG: GCR Message: CRC/ECC Tallying logic bad lane to repair.
56	RWX	RX_DYN_RPR_IP_GCRMSG: GCR Message: CRC/ECC Bad Lane Repair In Progress.
57	RWX	RX_DYN_RPR_COMPLETE_GCRMSG: GCR Message: CRC/ECC Bad Lane Repaired.
58:63	RO	constant=0b000000

Register Name	*CRC/ECC Dynamic Repair Lane Error Frequency Settings*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_ERR_TALLYING1_PG
Address	8009D8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:54	RWX	RX_DYN_RPR_BAD_LANE_MAX: CRC/ECC Dynamic Repair: Max number of times a lane can be found bad before repaired.
55:58	RWX	RX_DYN_RPR_ERR_CNTR1_DURATION: CRC/ECC Dynamic Repair: Duration the lane error counter1 can run before being cleared (determines the allowed error frequency). On a 833ps & 1250ps slow clk:. 0b0000 = 26.7ns & 40.0nS 0b0001 = 853.0ns & 1.3uS 0b0010 = 27.3uS & 41.0uS 0b0011 = 873.5uS & 1.3mS 0b0100 = 1.7mS & 2.6mS 0b0101 = 3.5mS & 5.1mS 0b0110 = 7.0mS & 10.5mS 0b0111 = 14.0mS & 21.0mS 0b1000 = 28.0mS & 41.9mS 0b1001 = 55.9mS & 83.9mS 0b1010 = 111.8mS & 167.8mS 0b1011 = 223.6mS & 335.5mS 0b1100 = 447.2mS & 671.1mS 0b1101 = 894.4mS & 1.3 S 0b1110 = 1.8 S & 2.7 S 0b1111 = infinite Values: TAP0=>0b0000 TAP1=>0b0001 TAP2=>0b0010 TAP3=>0b0011 TAP4=>0b0100 TAP5=>0b0101 TAP6=>0b0110 TAP7=>0b0111 TAProcessor=>0b1000 TAP9=>0b1001 TAP10=>0b1010 TAP11=>0b1011 TAP12=>0b1100 TAP13=>0b1101 TAP14=>0b1110 TAP15=>0b1111
59	RWX	RX_DYN_RPR_CLR_ERR_CNTR1: CRC/ECC Dynamic Repair: Firmware-based clear of lane error counter1 register.
60	RWX	RX_DYN_RPR_DISABLE: CRC/ECC Dynamic Repair: When set, disables dynamic repair error tallying (both per lane and per bus error counters...cntr1 & cntr2).
61:63	RWX	RX_DYN_RPR_ENC_BAD_DATA_LANE_WIDTH: CRC/ECC Dynamic Repair: Width of the enc_bad_data_lane vector used to determine number of 1s in clear code.

Register Name	***RX Final Load To Unload GCR Messages***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_FINAL_L2U_GCRMSGS_PG
Address	8009E0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RWX	RX_EO_FINAL_L2U_DLY_SEQ_GCRMSG: GCR Message: RX Final Load to Unload Delay GCR messages 0b00 = Indicate prior group calculated max load to unload change. 0b01 = Indicate all groups have calculated max load to unload change. 0b10 = Unused. 0b11 = No message. Values: FL2UPREVCHG=>0b00 FL2UALLCHG=>0b01 UNUSED=>0b10 FL2UNOMSG=>0b11
50:55	RWX	RX_EO_FINAL_L2U_DLY_MAXCHG_GCRMSG: GCR Message: Max change in miniumum load to unload delay.
56:57	RO	constant=0b00
58:63	ROX	Reserved field. (Access type is rx_eo_final_l2u_dly_chg_ro_signal)

Register Name	***RX SW Initiated GCR Message Destination IDs***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_DEST_IDS_PG
Address	8009E8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:53	RWX	RX_GCR_MSG_DEBUG_DEST_BUS_ID: GCR Messaging Debug: Destination Bus ID. FOR IO TEAM USE ONLY.
54:59	RWX	RX_GCR_MSG_DEBUG_DEST_GROUP_ID: GCR Messaging Debug: Destination Group ID. FOR IO TEAM USE ONLY.
60:63	RO	constant=0b0000

Register Name	***RX SW Initiated GCR Message Source IDs***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_SRC_IDS_PG
Address	8009F0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:53	RWX	RX_GCR_MSG_DEBUG_SRC_BUS_ID: GCR Messaging Debug: Source Bus ID. FOR IO TEAM USE ONLY.
54:59	RWX	RX_GCR_MSG_DEBUG_SRC_GROUP_ID: GCR Messaging Debug: Source Group ID. FOR IO TEAM USE ONLY.
60:63	RO	constant=0b0000

Register Name	*RX SW Initiated GCR Message Destination Addr*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_DEST_ADDR_PG
Address	8009F8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:56	RWX	RX_GCR_MSG_DEBUG_DEST_ADDR: GCR Messaging Debug: Destination Register Address. FOR IO TEAM USE ONLY.
57:62	RO	constant=0b000000
63	RWX	RX_GCR_MSG_DEBUG_SEND_MSG: GCR Messaging Debug: Send GCR Message on rising edge of this bit.. FOR IO TEAM USE ONLY.

Register Name	*RX SW Initiated GCR Message Write Data*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_GCR_MSG_DEBUG_WRITE_DATA_PG
Address	800A00000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RWX	RX_GCR_MSG_DEBUG_WRITE_DATA: GCR Messaging Debug: Data to Write to Destination Register. FOR IO TEAM USE ONLY.

Register Name	*RX Dynamic Recalibration Status*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_PG
Address	800A08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SERVO_RECAL_IP: RX Servo Lane Calibration In Progress.
49	RO	constant=0b0
50:55	ROX	Reserved field. (Access type is rx_dyn_recal_main_state_ro_signal)
56	RO	constant=0b0
57:63	ROX	Reserved field. (Access type is rx_dyn_recal_hndshk_state_ro_signal)

Register Name	*RX Clock Wiretest Status*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_WT_CLK_STATUS_PG
Address	800A10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	RX_WT_CLK_LANE_INVERTED: Clock Wiretest lane inverted/swapped status . 0b0 = not swapped or inverted 0b1 = P-N swapped or inverted Values: NOW_SWAPPED=>0b0 SWAPPED=>0b1
50:52	RWX	RX_WT_CLK_LANE_BAD_CODE: Clock Wiretest Lane Bad code. 0b000 = lane tested good 0b001 = N leg stuck at 1 0b010 = N leg stuck at 0 0b011 = P leg stuck at 1 0b100 = P leg stuck at 0 0b101 = N or P leg floating or swapping undetermined 0b110 = Unused. 0b111 = Unused Values: NO_ERROR=>0b000 N_STUCK_1=>0b001 N_STUCK_0=>0b010 P_STUCK_1=>0b011 P_STUCK_0=>0b100 N_OR_P_FLOATING=>0b101 NOT_USED_110=>0b110 NOT_USED_111=>0b111
53:63	RO	constant=0b00000000000 Values: NO_ERROR=>0b000 N_STUCK_1=>0b001 N_STUCK_0=>0b010 P_STUCK_1=>0b011 P_STUCK_0=>0b100 N_OR_P_FLOATING=>0b101 NOT_USED_110=>0b110 NOT_USED_111=>0b111

Register Name	*RX Dynamic Recalibration Configuration*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_CONFIG_PG
Address	800A18000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RWX	RX_DYN_RECAL_OVERALL_TIMEOUT_SEL: Dynamic Recalibration Overall Timeout Selects. 0b000 = 27.30us - really small value for sim 0b001 = 436.73us - smallest value for normal operation 0b010 = 873.46uS 0b011 = 1.75mS 0b100 = 3.49mS - Recal should be around 2mS 0b101 = 13.97mS 0b110 = 55.90mS - largest value for normal operation 0b111 = Infinite- For debug purposes Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51	RWX	RX_DYN_RECAL_SUSPEND: Suspend Dynamic Recalibration; otherwise starts automatically after link training.
52:63	RO	constant=0b000000000000

Register Name	***RX Wiretest Miscelleneous Configuration***
Mnemonic	DMI.RX.RXCTL.RX_CTL2_REGS.RX_WT_CONFIG_PG
Address	800A20000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	RWX	RX_WT_CHECK_COUNT: Selects number of extra times the wiretest pattern is checked for a good lane .
53:54	RWX	RX_WT_CHECK_LANES: Selects number of lanes that are checked during all-ones or all-zeroes check during wiretest:.
55:63	RO	constant=0b000000000

Register Name	***RX Dynamic Recalibration GCR Messages***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_GCRMSG_PG
Address	800A28000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_DYN_RECAL_IP_GCRMSG: GCR Message: RX Dynamic Recalibration In Progress.
49	RWX	RX_DYN_RECAL_FAILED_GCRMSG: GCR Message: RX Dynamic Recalibration Failed.
50	RWX	RX_DYN_RECAL_RIPPLE_GCRMSG: GCR Message: RX Dynamic Recalibration: Reached end of bus...ripple back down to the beginning.

Bits	SCOM	Field Mnemonic: Description
51	RWX	RX_DYN_RECAL_TIMEOUT_GCRMSG: GCR Message: RX Dynamic Recalibration: Recal Handshake Timed Out.
52:63	RO	constant=0b000000000000

Register Name	***RX PLL Or DLL Reset And Calibration Controls***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_WIRETEST_PLL_CNTL_PG
Address	800A30000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_WT_CU_PLL_PGOOD: RX PLL/DLL Enable. JFG 0b1 = Sets PGOOD on RX PLL for locking 0b0 = Places RX PLL in reset Values: PGOOD=>0b1 RESET=>0b0
49	RWX	RX_WT_CU_PLL_RESET: RX PLL/DLL Enable Request. JFG 0b1 = Clears PLL PGOOD and begins reset timer. See rx_wt_cu_pll_pgooddly. 0b0 = Do Nothing Values: ENABLE=>0b1 NOT_ENABLE=>0b0
50:52	RWX	RX_WT_CU_PLL_PGOODDLY: RX PLL/DLL PGOOD Delay Selects length of reset period after rx_wt_cu_pll_reset is set.JFG 0b000 = Minimum 16UI for sim bypass 0b001 = Nominal 50ns Reset per PLL Spec 0b010 = Double Nominal 50ns Reset per PLL Spec 0b011 = Typical simulation delay exceeding TX PLL 40-refclk locking period 0b100 = Reserved 0b101 = Reserved 0b110 = 1024 UI 0b111 = Disable rx_wt_cu_pll_reset Values: 16UI=>0b000 50NS=>0b001 100NS=>0b010 960UI=>0b011 UNUSED_100=>0b100 UNUSED_101=>0b101 MAX=>0b110 DISABLE=>0b111
53	ROX	Reserved field. (Access type is rx_wt_cu_pll_lock_ro_signal) Values: 16UI=>0b000 50NS=>0b001 100NS=>0b010 960UI=>0b011 UNUSED_100=>0b100 UNUSED_101=>0b101 MAX=>0b110 DISABLE=>0b111

Bits	SCOM	Field Mnemonic: Description
54	RWX	RX_WT_PLL_REFCLKSEL: Select between IO clock and BIST/Refclock. DMB 0b0 = Selects IO clock 0b1 = Selects BIST refclock Values: IO_CLOCK=>0b0 ALT_REFCLK=>0b1
55	RWX	RX_PLL_REFCLKSEL_SCOM_EN: Selects between PLL controls and GCR register to select refclk. DMB 0b0 = Uses PLL control to select refclk 0b1 = Uses GCR register, rx_wt_pll_refclksel, to select refclock Values: PLL_REFCLK_CNTL=>0b0 SCOM_REFCLK=>0b1
56:63	RO	constant=0b00000000 Values: PLL_REFCLK_CNTL=>0b0 SCOM_REFCLK=>0b1

Register Name	***RX Eye Optimization Step Control***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_STEP_CNTL_PG
Address	800A38000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	RX_EO_ENABLE_LATCH_OFFSET_CAL: RX eye optimization latch offset adjustment enable.
49	RWX	RX_EO_ENABLE_CTLE_CAL: RX eye optimization CTLE/Peakin enable.
50	RWX	RX_EO_ENABLE_VGA_CAL: RX eye optimization VGA gainand offset adjust enable.
51	RO	constant=0b0
52	RWX	RX_EO_ENABLE_DFE_H1_CAL: RX eye optimization DFE H1 adjust enable.
53	RWX	RX_EO_ENABLE_H1AP_TWEAK: RX eye optimization H1/AN PR adjust enable.
54	RWX	RX_EO_ENABLE_DDC: RX eye optimization Dynamic data centering enable.
55	RO	constant=0b0
56	RWX	RX_EO_ENABLE_FINAL_L2U_ADJ: RX eye optimization Final RX FIFO load-to-unload delay adjustment enable.
57	RWX	RX_EO_ENABLE_BER_TEST: RX eye optimization Bit error rate test enable.
58	RWX	RX_EO_ENABLE_RESULT_CHECK: RX eye optimization Final results check enable.
59	RWX	RX_EO_ENABLE_CTLE_EDGE_TRACK_ONLY: RX eye optimization CTLE/Peakin enable with edge tracking only.
60:63	RO	constant=0b0000

Register Name	*RX Eye Optimization Step Status*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_STEP_STAT_PG
Address	800A40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_EO_LATCH_OFFSET_DONE: RX eye optimization latch offset adjustment done.
49	RWX	RX_EO_CTLE_DONE: RX eye optimization CTLE/Peaking done.
50	RWX	RX_EO_VGA_DONE: RX eye optimization VGA gain/offset adjust done.
51	RO	constant=0b0
52	RWX	RX_EO_DFE_H1_DONE: NO LONGER USED--REMOVE for DD2 design.
53	RWX	RX_EO_H1AP_TWEAK_DONE: RX eye optimization H1/AN PR adjust done.
54	RWX	RX_EO_DDC_DONE: RX eye optimization Dynamic data centering done.
55	RO	constant=0b0
56	RWX	RX_EO_FINAL_L2U_ADJ_DONE: RX eye optimization Final RX FIFO load-to-unload adjust done.
57	RWX	RX_EO_DFE_FLAG: RX eye optimization DFE mode flag.
58	RWX	RX_EO_BER_TEST_DONE: RX eye optimization Bit Error rate test done.
59	RWX	RX_EO_RESULT_CHECK_DONE: RX eye optimization Eye width/heightER check done.
60:63	RO	constant=0b0000

Register Name	*RX Eye Optimization Ap Working Registers*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_AP_PG
Address	800A50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AP_EVEN_WORK: RX Ap even working register.
56:63	RWX	RX_AP_ODD_WORK: Rx Ap odd working register.

Register Name	*RX Eye Optimization An Working Registers*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_AN_PG
Address	800A58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RWX	RX_AN_EVEN_WORK: RX An even working register.
56:63	RWX	RX_AN_ODD_WORK: Rx An odd working register.

Register Name	*RX Eye Optimization Amin Working Registers*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_AMIN_PG
Address	800A60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMIN_EVEN_WORK: RX Amin even working register.
56:63	RWX	RX_AMIN_ODD_WORK: Rx Amin odd working register.

Register Name	*RX Eye Optimization Amax Limit Registers*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_AMAX_PG
Address	800A68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	RX_AMAX_HIGH: RX Amax high limit default 125.
56:63	RWX	RX_AMAX_LOW: Rx Amax low limit default 75.

Register Name	*RX Eye Optimization Amp Working Registers*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_AMP_VAL_PG
Address	800A70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_AMP_PEAK_WORK: Rx amp peak working register.
52:55	RWX	RX_AMP_GAIN_WORK: Rx Amp gain working register.
56:57	RO	constant=0b00
58:63	RWX	RX_AMP_OFFSET_WORK: Rx amp offset working register.

Register Name	*RX Eye Optimization Amp Offset Limts*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_AMP_OFFSET_PG
Address	800A78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RWX	RX_AMP_OFFSET_MAX: Rx amp maximum allowable offset.
54:59	RWX	RX_AMP_OFFSET_MIN: Rx Amp minimum allowable offset.
60:63	RO	constant=0b0000

Register Name	*RX Eye Optimization Convergence Control Regs*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_EO_CONVERGENCE_PG
Address	800A80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_EO_CONVERGED_COUNT: RX eye optimization Convergence counter current value.
52:55	RWX	RX_EO_CONVERGED_END_COUNT: RX eye optimization Covergence counter end value.
56:63	RO	constant=0b00000000

Register Name	*RX SLS Handshake Recovery Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SLS_RCVY_PG
Address	800A88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_RCVY_DISABLE: Disable SLS Recovery.
49:50	RO	constant=0b00
51:55	ROX	Reserved field. (Access type is rx_sls_rcvy_state_ro_signal)
56:63	RO	constant=0b00000000

Register Name	*RX SLS Handshake Recovery GCR Messages*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SLS_RCVY_GCRMSG_PG
Address	800A90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_SLS_RCVY_REQ_GCRMSG: GCR Message: SLS Rcvy; RX Lane Repair Req.
49	RWX	RX_SLS_RCVY_IP_GCRMSG: GCR Message: SLS Rcvy; RX Lane Repair IP.
50	RWX	RX_SLS_RCVY_DONE_GCRMSG: GCR Message: SLS Rcvy; RX Lane Repair Done.
51:63	RO	constant=0b0000000000000

Register Name	*RX: TX Lane Info*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TX_LANE_INFO_GCRMSG_PG
Address	800A98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_TX_BAD_LANE_CNTR_GCRMSG: GCR Message: RX Side TX Bad Lane Counter.
50:63	RO	constant=0b00000000000000

Register Name	*CRC/ECC Syndrome Tallying GCR Message Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_ERR_TALLYING_GCRMSG_PG
Address	800AA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_DIS_SYND_TALLYING_GCRMSG: GCR Message: Disable Syndrome Tallying.
49:63	RO	constant=0b000000000000000

Register Name	*RX Trace Mode Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_TRACE_PG
Address	800AA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_TRC_MODE: RX Trace Mode. 0b0000 = Training State Machines 0b0001 = Dynamic Repair State Machines 0b0010 = SLS Handshake State Machines with Recovery 0b0011 = Dynamic Recal State Machines 0b0100 = Recal Handshake State Machine with Recovery 0b0101 = CRC or ECC Tallying Logic 0b0110 = RX SLS Commands 0b0111 = RX Bad Lanes 0b1000 = RX SLS Lanes 0b1001 = GCR 0b1010 = Per Lane / Per Pack Trace (see rx_pp_trc_mode for details) 0b1011 = TBD 0b1100 = TBD 0b1101 = TBD 0b1110 = TBD 0b1111 = TBD Values: TAP0=>0b0000 TAP1=>0b0001 TAP2=>0b0010 TAP3=>0b0011 TAP4=>0b0100 TAP5=>0b0101 TAP6=>0b0110 TAP7=>0b0111 TAProcessor=>0b1000 TAP9=>0b1001 TAP10=>0b1010 TAP11=>0b1011 TAP12=>0b1100 TAP13=>0b1101 TAP14=>0b1110 TAP15=>0b1111
52:53	RO	constant=0b00 Values: TAP0=>0b0000 TAP1=>0b0001 TAP2=>0b0010 TAP3=>0b0011 TAP4=>0b0100 TAP5=>0b0101 TAP6=>0b0110 TAP7=>0b0111 TAProcessor=>0b1000 TAP9=>0b1001 TAP10=>0b1010 TAP11=>0b1011 TAP12=>0b1100 TAP13=>0b1101 TAP14=>0b1110 TAP15=>0b1111
54:59	RWX	RX_TRC_GRP: RX Clock Group to be Traced 111111 will trace whichever clk group currently contains the RX SLS Lane.
60:63	RO	constant=0b0000

Register Name	*RX Recalibraton Step Control*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RC_STEP_CNTL_PG
Address	800AB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_RC_ENABLE_LATCH_OFFSET_CAL: RX recalibration latch offset adjustment enable.
49	RWX	RX_RC_ENABLE_CTLE_CAL: RX recalibration CTLE/Peaking enable.
50	RWX	RX_RC_ENABLE_VGA_CAL: RX recalibration VGA gainand offset adjust enable.
51	RO	constant=0b0
52	RWX	RX_RC_ENABLE_DFE_H1_CAL: RX recalibration DFE H1 adjust enable.
53	RWX	RX_RC_ENABLE_H1AP_TWEAK: RX recalibration H1/AN PR adjust enable.
54	RWX	RX_RC_ENABLE_DDC: RX recalibration Dynamic data centering enable.
55	RO	constant=0b0
56	RWX	RX_RC_ENABLE_BER_TEST: RX recalibration Bit error rate test enable.
57	RWX	RX_RC_ENABLE_RESULT_CHECK: RX recalibration Final results check enable.
58	RO	constant=0b0
59	RWX	RX_RC_ENABLE_CTLE_EDGE_TRACK_ONLY: RX recalibration CTLE/Peaking enable with edge tracking only.
60:63	RO	constant=0b0000

Register Name	*RX Recal Bit Error Rate Count Working Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SERVO_BER_COUNT_PG
Address	800AC8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	RWX	RX_SERVO_BER_COUNT_WORK: Rx servo-based bit error rate count working register.
60:63	RO	constant=0b0000

Register Name	*Dynamic Repair Testfloor/Debug Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_DEBUG_PG
Address	800AD8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	NCX	Reserved field. (Access type is rx_dyn_rpr_bad_lane_valid_debug_wo_pulse_slow_signal)
49:55	RWX	RX_DYN_RPR_ENC_BAD_DATA_LANE_DEBUG: For testfloor/debug purposes, specify the encoded bad data lane to report to the dynamic repair tally logic.
56	RO	constant=0b0
57:63	ROX	Reserved field. (Access type is rx_bad_bus_err_cntr_ro_signal)

Register Name	***CRC/ECC Dynamic Repair Bus Error Frequency Settings***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RPR_ERR_TALLYING2_PG
Address	800AE0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:54	RWX	RX_DYN_RPR_BAD_BUS_MAX: CRC/ECC Dynamic Repair: Max number of times CRC or ECC errors can be found on the bus (not included in the bad lane cntr1 tally) before setting a FIR error.
55:58	RWX	RX_DYN_RPR_ERR_CNTR2_DURATION: CRC/ECC Dynamic Repair: Duration the bad bus cntr2 error counter can run before being cleared (determines the allowed error frequency). On a 833ps & 1250ps slow clk:. 0b0000 = 26.7ns & 40.0nS 0b0001 = 853.0ns & 1.3uS 0b0010 = 27.3uS & 41.0uS 0b0011 = 873.5uS & 1.3mS 0b0100 = 1.7mS & 2.6mS 0b0101 = 3.5mS & 5.1mS 0b0110 = 7.0mS & 10.5mS 0b0111 = 14.0mS & 21.0mS 0b1000 = 28.0mS & 41.9mS 0b1001 = 55.9mS & 83.9mS 0b1010 = 111.8mS & 167.8mS 0b1011 = 223.6mS & 335.5mS 0b1100 = 447.2mS & 671.1mS 0b1101 = 894.4mS & 1.3 S 0b1110 = 1.8 S & 2.7 S 0b1111 = infinite Values: TAP0=>0b0000 TAP1=>0b0001 TAP2=>0b0010 TAP3=>0b0011 TAP4=>0b0100 TAP5=>0b0101 TAP6=>0b0110 TAP7=>0b0111 TAProcessor=>0b1000 TAP9=>0b1001 TAP10=>0b1010 TAP11=>0b1011 TAP12=>0b1100 TAP13=>0b1101 TAP14=>0b1110 TAP15=>0b1111
59	RWX	RX_DYN_RPR_CLR_ERR_CNTR2: CRC/ECC Dynamic Repair: Firmware-based clear of bus error counter2 register.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant=0b0000

Register Name	*Eye Widhth/height Results Check Limits*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RESULT_CHK_PG
Address	800AE8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	RX_MIN_EYE_WIDTH: Minimum acceptable eye width used during init or recal results checking--EDI or EI4. DMB
56:63	RWX	RX_MIN_EYE_HEIGHT: Minimum acceptable eye height used during init or recal results checking--EDI only. DMB

Register Name	*Bit Error Rate Check Max Rate K Limits*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_BER_CHK_PG
Address	800AF0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000
56:63	RWX	RX_MAX_BER_CHECK_COUNT: Maximum acceptable number of bit errors allowable after recal--EDI only.

Register Name	*RX SLS Handshake Recovery Finish GCR Messages*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SLS_RCVY_FIN_GCRMSG_PG
Address	800AF8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_SLV_SHDW_DONE_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for shdw_done.
49	RWX	RX_SLV_SHDW_NOP_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for nop.
50	RWX	RX_SLV_SHDW_RPR_DONE_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for shdw_rpr_done.
51	RWX	RX_SLV_SHDW_RPR_NOP_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for nop.

Bits	SCOM	Field Mnemonic: Description
52	RWX	RX_SLV_UNSHDW_DONE_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for unshdw_done.
53	RWX	RX_SLV_UNSHDW_NOP_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for nop.
54	RWX	RX_SLV_UNSHDW_RPR_DONE_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for unshdw_rpr_done.
55	RWX	RX_SLV_UNSHDW_RPR_NOP_FIN_GCRMSG: GCR Message: Slave RX SLS Lane Repaired; Need to finish slave shadow handshake starting with waiting for nop.
56	RWX	RX_SLV_RECAL_DONE_NOP_FIN_GCRMSG: GCR Message: Slave Recal Done; Need to finish slave recal handshake starting with waiting for nop.
57	RWX	RX_SLV_RECAL_FAIL_NOP_FIN_GCRMSG: GCR Message: Slave Recal Fail; Need to finish slave recal handshake starting with waiting for nop.
58	RWX	RX_SLV_RECAL_PRESULTS_FIN_GCRMSG: GCR Message: Slave Recal Pass Results; Need to finish slave recal handshake starting with waiting for results.
59	RWX	RX_SLV_RECAL_FRESULTS_FIN_GCRMSG: GCR Message: Slave Recal Fail Results; Need to finish slave recal handshake starting with waiting for results.
60	RWX	RX_SLV_RECAL_ABORT_ACK_FIN_GCRMSG: GCR Message: Slave Recal Abort; Need to finish slave recal handshake starting with waiting for nop.
61	RWX	RX_SLV_RECAL_ABORT_MNOP_FIN_GCRMSG: GCR Message: Slave Recal Abort; Need to finish slave recal handshake starting with waiting for nop.
62	RWX	RX_SLV_RECAL_ABORT_SNOP_FIN_GCRMSG: GCR Message: Slave Recal Abort; Need to finish slave recal handshake starting with waiting for nop.
63	RO	constant=0b0

Register Name	***RX Mode Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_MODE1_PP
Address	800B08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	RX_REDUCED_SCRAMBLE_MODE: Sets reduced density of scramble pattern. This must be set consistent with tx_reduced_scramble_mode. 0b00 = Disable reduced density 0b01 = Disable reduced density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density Values: DISABLE_0=>0b00 DISABLE_1=>0b01 ENABLE_DIV2=>0b10 ENABLE_DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	RW	RX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by RX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	RW	RX_ACT_CHECK_TIMEOUT_SEL: Sets Activity check timeout value. 0b000 = 16UI 0b001 = 128 UI 0b010 = 256 UI 0b011 = 512 UI 0b100 = 1024 UI 0b101 = 2048 UI 0b110 = 4096 UI 0b111 = Infinite Values: 16UI=>0b000 128UI=>0b001 256UI=>0b010 512UI=>0b011 1024UI=>0b100 2048UI=>0b101 4096UI=>0b110 INFINITE=>0b111
55:57	RW	RX_BLOCK_LOCK_TIMEOUT_SEL: Sets block lock timeout value. 0b000 = 16UI 0b001 = 1024 UI 0b010 = 2048 UI 0b011 = 4096 UI 0b100 = 8192 UI 0b101 = 16384 UI 0b110 = 32768 UI 0b111 = Infinite Values: 16UI=>0b000 1024UI=>0b001 2048UI=>0b010 4096UI=>0b011 8192UI=>0b100 16384UI=>0b101 32768UI=>0b110 INFINITE=>0b111

Bits	SCOM	Field Mnemonic: Description
58:60	RW	RX_BIT_LOCK_TIMEOUT_SEL: Sets bit lock/edge detect timeout value. 0b000 = 16UI 0b001 = 512 UI 0b010 = 1024 UI 0b011 = 2048 UI 0b100 = 4096 UI 0b101 = 8192 UI 0b110 = 16384 UI 0b111 = Infinite Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111
61:63	RO	constant=0b000 Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111

Register Name	*RX Mode Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE1_PP
Address	800B08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_REDUCED_SCRAMBLE_MODE: Sets reduced density of scramble pattern. This must be set consistent with tx_reduced_scramble_mode. 0b00 = Disable reduced density 0b01 = Disable reduced density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density Values: DISABLE_0=>0b00 DISABLE_1=>0b01 ENABLE_DIV2=>0b10 ENABLE_DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	WOX	RX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by RX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	RX_ACT_CHECK_TIMEOUT_SEL: Sets Activity check timeout value. 0b000 = 16UI 0b001 = 128 UI 0b010 = 256 UI 0b011 = 512 UI 0b100 = 1024 UI 0b101 = 2048 UI 0b110 = 4096 UI 0b111 = Infinite Values: 16UI=>0b000 128UI=>0b001 256UI=>0b010 512UI=>0b011 1024UI=>0b100 2048UI=>0b101 4096UI=>0b110 INFINITE=>0b111
55:57	WOX	RX_BLOCK_LOCK_TIMEOUT_SEL: Sets block lock timeout value. 0b000 = 16UI 0b001 = 1024 UI 0b010 = 2048 UI 0b011 = 4096 UI 0b100 = 8192 UI 0b101 = 16384 UI 0b110 = 32768 UI 0b111 = Infinite Values: 16UI=>0b000 1024UI=>0b001 2048UI=>0b010 4096UI=>0b011 8192UI=>0b100 16384UI=>0b101 32768UI=>0b110 INFINITE=>0b111

Bits	SCOM	Field Mnemonic: Description
58:60	WOX	RX_BIT_LOCK_TIMEOUT_SEL: Sets bit lock/edge detect timeout value. 0b000 = 16UI 0b001 = 512 UI 0b010 = 1024 UI 0b011 = 2048 UI 0b100 = 4096 UI 0b101 = 8192 UI 0b110 = 16384 UI 0b111 = Infinite Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111
61:63	RO	constant=0b000 Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111

Register Name	***RX Mode Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE1_PP
Address	800B08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_REDUCED_SCRAMBLE_MODE: Sets reduced density of scramble pattern. This must be set consistent with tx_reduced_scramble_mode. 0b00 = Disable reduced density 0b01 = Disable reduced density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density Values: DISABLE_0=>0b00 DISABLE_1=>0b01 ENABLE_DIV2=>0b10 ENABLE_DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	WOX	RX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by RX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	RX_ACT_CHECK_TIMEOUT_SEL: Sets Activity check timeout value. 0b000 = 16UI 0b001 = 128 UI 0b010 = 256 UI 0b011 = 512 UI 0b100 = 1024 UI 0b101 = 2048 UI 0b110 = 4096 UI 0b111 = Infinite Values: 16UI=>0b000 128UI=>0b001 256UI=>0b010 512UI=>0b011 1024UI=>0b100 2048UI=>0b101 4096UI=>0b110 INFINITE=>0b111
55:57	WOX	RX_BLOCK_LOCK_TIMEOUT_SEL: Sets block lock timeout value. 0b000 = 16UI 0b001 = 1024 UI 0b010 = 2048 UI 0b011 = 4096 UI 0b100 = 8192 UI 0b101 = 16384 UI 0b110 = 32768 UI 0b111 = Infinite Values: 16UI=>0b000 1024UI=>0b001 2048UI=>0b010 4096UI=>0b011 8192UI=>0b100 16384UI=>0b101 32768UI=>0b110 INFINITE=>0b111

Bits	SCOM	Field Mnemonic: Description
58:60	WOX	RX_BIT_LOCK_TIMEOUT_SEL: Sets bit lock/edge detect timeout value. 0b000 = 16UI 0b001 = 512 UI 0b010 = 1024 UI 0b011 = 2048 UI 0b100 = 4096 UI 0b101 = 8192 UI 0b110 = 16384 UI 0b111 = Infinite Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111
61:63	RO	constant=0b000 Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111

Register Name	***RX Mode Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE1_PP
Address	800B08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_REDUCED_SCRAMBLE_MODE: Sets reduced density of scramble pattern. This must be set consistent with tx_reduced_scramble_mode. 0b00 = Disable reduced density 0b01 = Disable reduced density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density Values: DISABLE_0=>0b00 DISABLE_1=>0b01 ENABLE_DIV2=>0b10 ENABLE_DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	WOX	RX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by RX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	RX_ACT_CHECK_TIMEOUT_SEL: Sets Activity check timeout value. 0b000 = 16UI 0b001 = 128 UI 0b010 = 256 UI 0b011 = 512 UI 0b100 = 1024 UI 0b101 = 2048 UI 0b110 = 4096 UI 0b111 = Infinite Values: 16UI=>0b000 128UI=>0b001 256UI=>0b010 512UI=>0b011 1024UI=>0b100 2048UI=>0b101 4096UI=>0b110 INFINITE=>0b111
55:57	WOX	RX_BLOCK_LOCK_TIMEOUT_SEL: Sets block lock timeout value. 0b000 = 16UI 0b001 = 1024 UI 0b010 = 2048 UI 0b011 = 4096 UI 0b100 = 8192 UI 0b101 = 16384 UI 0b110 = 32768 UI 0b111 = Infinite Values: 16UI=>0b000 1024UI=>0b001 2048UI=>0b010 4096UI=>0b011 8192UI=>0b100 16384UI=>0b101 32768UI=>0b110 INFINITE=>0b111

Bits	SCOM	Field Mnemonic: Description
58:60	WOX	RX_BIT_LOCK_TIMEOUT_SEL: Sets bit lock/edge detect timeout value. 0b000 = 16UI 0b001 = 512 UI 0b010 = 1024 UI 0b011 = 2048 UI 0b100 = 4096 UI 0b101 = 8192 UI 0b110 = 16384 UI 0b111 = Infinite Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111
61:63	RO	constant=0b000 Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111

Register Name	*RX Mode Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE1_PP
Address	800B08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_REDUCED_SCRAMBLE_MODE: Sets reduced density of scramble pattern. This must be set consistent with tx_reduced_scramble_mode. 0b00 = Disable reduced density 0b01 = Disable reduced density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density Values: DISABLE_0=>0b00 DISABLE_1=>0b01 ENABLE_DIV2=>0b10 ENABLE_DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	WOX	RX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by RX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	RX_ACT_CHECK_TIMEOUT_SEL: Sets Activity check timeout value. 0b000 = 16UI 0b001 = 128 UI 0b010 = 256 UI 0b011 = 512 UI 0b100 = 1024 UI 0b101 = 2048 UI 0b110 = 4096 UI 0b111 = Infinite Values: 16UI=>0b000 128UI=>0b001 256UI=>0b010 512UI=>0b011 1024UI=>0b100 2048UI=>0b101 4096UI=>0b110 INFINITE=>0b111
55:57	WOX	RX_BLOCK_LOCK_TIMEOUT_SEL: Sets block lock timeout value. 0b000 = 16UI 0b001 = 1024 UI 0b010 = 2048 UI 0b011 = 4096 UI 0b100 = 8192 UI 0b101 = 16384 UI 0b110 = 32768 UI 0b111 = Infinite Values: 16UI=>0b000 1024UI=>0b001 2048UI=>0b010 4096UI=>0b011 8192UI=>0b100 16384UI=>0b101 32768UI=>0b110 INFINITE=>0b111

Bits	SCOM	Field Mnemonic: Description
58:60	WOX	RX_BIT_LOCK_TIMEOUT_SEL: Sets bit lock/edge detect timeout value. 0b000 = 16UI 0b001 = 512 UI 0b010 = 1024 UI 0b011 = 2048 UI 0b100 = 4096 UI 0b101 = 8192 UI 0b110 = 16384 UI 0b111 = Infinite Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111
61:63	RO	constant=0b000 Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111

Register Name	*RX Mode Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_MODE1_PP
Address	800B08000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_REDUCED_SCRAMBLE_MODE: Sets reduced density of scramble pattern. This must be set consistent with tx_reduced_scramble_mode. 0b00 = Disable reduced density 0b01 = Disable reduced density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density Values: DISABLE_0=>0b00 DISABLE_1=>0b01 ENABLE_DIV2=>0b10 ENABLE_DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	WOX	RX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by RX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	RX_ACT_CHECK_TIMEOUT_SEL: Sets Activity check timeout value. 0b000 = 16UI 0b001 = 128 UI 0b010 = 256 UI 0b011 = 512 UI 0b100 = 1024 UI 0b101 = 2048 UI 0b110 = 4096 UI 0b111 = Infinite Values: 16UI=>0b000 128UI=>0b001 256UI=>0b010 512UI=>0b011 1024UI=>0b100 2048UI=>0b101 4096UI=>0b110 INFINITE=>0b111
55:57	WOX	RX_BLOCK_LOCK_TIMEOUT_SEL: Sets block lock timeout value. 0b000 = 16UI 0b001 = 1024 UI 0b010 = 2048 UI 0b011 = 4096 UI 0b100 = 8192 UI 0b101 = 16384 UI 0b110 = 32768 UI 0b111 = Infinite Values: 16UI=>0b000 1024UI=>0b001 2048UI=>0b010 4096UI=>0b011 8192UI=>0b100 16384UI=>0b101 32768UI=>0b110 INFINITE=>0b111

Bits	SCOM	Field Mnemonic: Description
58:60	WOX	RX_BIT_LOCK_TIMEOUT_SEL: Sets bit lock/edge detect timeout value. 0b000 = 16UI 0b001 = 512 UI 0b010 = 1024 UI 0b011 = 2048 UI 0b100 = 4096 UI 0b101 = 8192 UI 0b110 = 16384 UI 0b111 = Infinite Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111
61:63	RO	constant=0b000 Values: 16UI=>0b000 512UI=>0b001 1024UI=>0b010 2048UI=>0b011 4096UI=>0b100 8192UI=>0b101 16384UI=>0b110 INFINITE=>0b111

Register Name	*RX Control Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_CNTL_FAST_PP
Address	800B10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	RX_PRBS_CHECK_SYNC: Enables checking for the 12 ui scramble sync pattern. 0b0 = Disable checking (forces prbs_synced_b to 1) 0b1 = Enable checking (prbs_synced_b can go to 0) Values: DISABLED=>0b0 ENABLED=>0b1
50	RWX	RX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. 0b0 = Disable reduced density 0b1 = Enable reduced density per the rx_reduced_scramble_mode setting Values: DISABLED=>0b0 ENABLED=>0b1
51	NCX	Reserved field. (Access type is rx_prbs_inc_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
52	NCX	Reserved field. (Access type is rx_prbs_dec_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
53:63	RO	constant=0b00000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*RX Control Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_CNTL_FAST_PP
Address	800B10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	WOX	RX_PRBS_CHECK_SYNC: Enables checking for the 12 ui scramble sync pattern. 0b0 = Disable checking (forces prbs_synced_b to 1) 0b1 = Enable checking (prbs_synced_b can go to 0) Values: DISABLED=>0b0 ENABLED=>0b1
50	WOX	RX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. 0b0 = Disable reduced density 0b1 = Enable reduced density per the rx_reduced_scramble_mode setting Values: DISABLED=>0b0 ENABLED=>0b1
51	NCX	Reserved field. (Access type is rx_prbs_inc_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
52	NCX	Reserved field. (Access type is rx_prbs_dec_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
53:63	RO	constant=0b00000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*RX Control Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_CNTL_FAST_PP
Address	800B10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	WOX	RX_PRBS_CHECK_SYNC: Enables checking for the 12 ui scramble sync pattern. 0b0 = Disable checking (forces prbs_synced_b to 1) 0b1 = Enable checking (prbs_synced_b can go to 0) Values: DISABLED=>0b0 ENABLED=>0b1
50	WOX	RX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. 0b0 = Disable reduced density 0b1 = Enable reduced density per the rx_reduced_scramble_mode setting Values: DISABLED=>0b0 ENABLED=>0b1
51	NCX	Reserved field. (Access type is rx_prbs_inc_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
52	NCX	Reserved field. (Access type is rx_prbs_dec_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
53:63	RO	constant=0b00000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***RX Control Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_CNTL_FAST_PP
Address	800B10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	WOX	RX_PRBS_CHECK_SYNC: Enables checking for the 12 ui scramble sync pattern. 0b0 = Disable checking (forces prbs_synced_b to 1) 0b1 = Enable checking (prbs_synced_b can go to 0) Values: DISABLED=>0b0 ENABLED=>0b1
50	WOX	RX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. 0b0 = Disable reduced density 0b1 = Enable reduced density per the rx_reduced_scramble_mode setting Values: DISABLED=>0b0 ENABLED=>0b1
51	NCX	Reserved field. (Access type is rx_prbs_inc_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
52	NCX	Reserved field. (Access type is rx_prbs_dec_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
53:63	RO	constant=0b00000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*RX Control Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_CNTL_FAST_PP
Address	800B10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	WOX	RX_PRBS_CHECK_SYNC: Enables checking for the 12 ui scramble sync pattern. 0b0 = Disable checking (forces prbs_synced_b to 1) 0b1 = Enable checking (prbs_synced_b can go to 0) Values: DISABLED=>0b0 ENABLED=>0b1
50	WOX	RX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. 0b0 = Disable reduced density 0b1 = Enable reduced density per the rx_reduced_scramble_mode setting Values: DISABLED=>0b0 ENABLED=>0b1
51	NCX	Reserved field. (Access type is rx_prbs_inc_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
52	NCX	Reserved field. (Access type is rx_prbs_dec_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
53:63	RO	constant=0b00000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*RX Control Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_CNTL_FAST_PP
Address	800B10000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	WOX	RX_PRBS_CHECK_SYNC: Enables checking for the 12 ui scramble sync pattern. 0b0 = Disable checking (forces prbs_synced_b to 1) 0b1 = Enable checking (prbs_synced_b can go to 0) Values: DISABLED=>0b0 ENABLED=>0b1
50	WOX	RX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. 0b0 = Disable reduced density 0b1 = Enable reduced density per the rx_reduced_scramble_mode setting Values: DISABLED=>0b0 ENABLED=>0b1
51	NCX	Reserved field. (Access type is rx_prbs_inc_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
52	NCX	Reserved field. (Access type is rx_prbs_dec_wo_pulse_fast_signal) Values: DISABLED=>0b0 ENABLED=>0b1
53:63	RO	constant=0b00000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***RX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DYN_RECAL_TIMEOUTS_PP
Address	800B40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RWX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: RX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5ns 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	RWX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: RX Dynamic Recalibration Status Reporting Timeout Selects. This value MUST be LONGER than the sls_cntr_tap_sel!. 0b00 = 512UI or 53.2ns 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	*RX Dynamic Recalibration Timeout Selects*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DYN_RECAL_TIMEOUTS_PP
Address	800B40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: RX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5ns 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: RX Dynamic Recalibration Status Reporting Timeout Selects. This value MUST be LONGER than the sls_cntr_tap_sel!. 0b00 = 512UI or 53.2ns 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***RX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DYN_RECAL_TIMEOUTS_PP
Address	800B40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: RX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5ns 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: RX Dynamic Recalibration Status Reporting Timeout Selects. This value MUST be LONGER than the sls_cntr_tap_sel!. 0b00 = 512UI or 53.2ns 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***RX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DYN_RECAL_TIMEOUTS_PP
Address	800B40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: RX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5ns 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: RX Dynamic Recalibration Status Reporting Timeout Selects. This value MUST be LONGER than the sls_cntr_tap_sel!. 0b00 = 512UI or 53.2ns 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***RX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DYN_RECAL_TIMEOUTS_PP
Address	800B40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: RX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5ns 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: RX Dynamic Recalibration Status Reporting Timeout Selects. This value MUST be LONGER than the sls_cntr_tap_sel!. 0b00 = 512UI or 53.2ns 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	*RX Dynamic Recalibration Timeout Selects*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_DYN_RECAL_TIMEOUTS_PP
Address	800B40000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	RX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: RX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5ns 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
52:53	WOX	RX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: RX Dynamic Recalibration Status Reporting Timeout Selects. This value MUST be LONGER than the sls_cntr_tap_sel!. 0b00 = 512UI or 53.2ns 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Bits	SCOM	Field Mnemonic: Description
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	*RX BER Control Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_BER_CNTL_PP
Address	800B50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_BER_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) error checking enable control. When 1 enables error checking. When 0 the error checking is disabled. This control enables the BER timer as well as enables the error checker and BER counters. The assumption is that the driver(s) are currently driving PRBS23 and the link has been trained before enabling BER checking.
49	NCX	Reserved field. (Access type is rx_ber_count_clr_wo_pulse_slow_signal)
50	NCX	Reserved field. (Access type is rx_ber_timer_clr_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	*RX BER Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_CNTL_PP
Address	800B50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) error checking enable control. When 1 enables error checking. When 0 the error checking is disabled. This control enables the BER timer as well as enables the error checker and BER counters. The assumption is that the driver(s) are currently driving PRBS23 and the link has been trained before enabling BER checking.
49	NCX	Reserved field. (Access type is rx_ber_count_clr_wo_pulse_slow_signal)
50	NCX	Reserved field. (Access type is rx_ber_timer_clr_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	*RX BER Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_CNTL_PP
Address	800B50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) error checking enable control. When 1 enables error checking. When 0 the error checking is disabled. This control enables the BER timer as well as enables the error checker and BER counters. The assumption is that the driver(s) are currently driving PRBS23 and the link has been trained before enabling BER checking.
49	NCX	Reserved field. (Access type is rx_ber_count_clr_wo_pulse_slow_signal)
50	NCX	Reserved field. (Access type is rx_ber_timer_clr_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***RX BER Control Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_CNTL_PP
Address	800B50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) error checking enable control. When 1 enables error checking. When 0 the error checking is disabled. This control enables the BER timer as well as enables the error checker and BER counters. The assumption is that the driver(s) are currently driving PRBS23 and the link has been trained before enabling BER checking.
49	NCX	Reserved field. (Access type is rx_ber_count_clr_wo_pulse_slow_signal)
50	NCX	Reserved field. (Access type is rx_ber_timer_clr_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***RX BER Control Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_CNTL_PP
Address	800B50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) error checking enable control. When 1 enables error checking. When 0 the error checking is disabled. This control enables the BER timer as well as enables the error checker and BER counters. The assumption is that the driver(s) are currently driving PRBS23 and the link has been trained before enabling BER checking.
49	NCX	Reserved field. (Access type is rx_ber_count_clr_wo_pulse_slow_signal)
50	NCX	Reserved field. (Access type is rx_ber_timer_clr_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***RX BER Control Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_BER_CNTL_PP
Address	800B50000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_BER_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) error checking enable control. When 1 enables error checking. When 0 the error checking is disabled. This control enables the BER timer as well as enables the error checker and BER counters. The assumption is that the driver(s) are currently driving PRBS23 and the link has been trained before enabling BER checking.
49	NCX	Reserved field. (Access type is rx_ber_count_clr_wo_pulse_slow_signal)
50	NCX	Reserved field. (Access type is rx_ber_timer_clr_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***RX BER Mode Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_BER_MODE_PP
Address	800B58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BER_TIMER_FREEZE_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) Timer freeze enable. When set to a 1 the per-pack timer is frozen when any lane error count saturates in that pack.
49	RWX	RX_BER_COUNT_FREEZE_EN: PP Diag BER Lane Error Counter freeze enable. When set to a 1 the per-lane error counters are frozen when the timer saturates in that pack.
50	RO	constant=0b0
51:53	RWX	RX_BER_COUNT_SEL: PP Diag BER Lane Error Counter saturation select. Selects the number of errors that will saturate the counter and cause a freeze event. 0b000 = 1 0b001 = 2 0b010 = 4 0b011 = 8 0b100 = 16 0b101 = 32 0b110 = 64 0b111 = 128 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100 32=>0b101 64=>0b110 128=>0b111

Bits	SCOM	Field Mnemonic: Description
54:56	RWX	RX_BER_TIMER_SEL: PP Diag BER Timer saturation select. Selects the timer value that will saturate the timer and cause a freeze event. 0b000 = 2^39 0b001 = 2^35 0b010 = 2^31 0b011 = 2^27 0b100 = 2^25 0b101 = 2^21 0b110 = 2^17 0b111 = 2^13 Values: 2TOTHE39TH=>0b000 2TOTHE35TH=>0b001 2TOTHE31ST=>0b010 2TOTHE27TH=>0b011 2TOTHE25TH=>0b100 2TOTHE21TH=>0b101 2TOTHE17TH=>0b110 2TOTHE13TH=>0b111
57	RWX	RX_BER_CLR_COUNT_ON_READ_EN: PP Diag BER Lane Error Counter clear on read. When set to a 1 this enables the clearing of a lanes error counter when it is read.
58	RWX	RX_BER_CLR_TIMER_ON_READ_EN: PP Diag BER Timer clear on read. When set to a 1 this enables the clearing of a lanes per-pack timer when it is read from any lane in the pack.
59:63	RO	constant=0b00000

Register Name	*RX BER Mode Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_MODE_PP
Address	800B58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_TIMER_FREEZE_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) Timer freeze enable. When set to a 1 the per-pack timer is frozen when any lane error count saturates in that pack.
49	WOX	RX_BER_COUNT_FREEZE_EN: PP Diag BER Lane Error Counter freeze enable. When set to a 1 the per-lane error counters are frozen when the timer saturates in that pack.
50	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
51:53	WOX	RX_BER_COUNT_SEL: PP Diag BER Lane Error Counter saturation select. Selects the number of errors that will saturate the counter and cause a freeze event. 0b000 = 1 0b001 = 2 0b010 = 4 0b011 = 8 0b100 = 16 0b101 = 32 0b110 = 64 0b111 = 128 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100 32=>0b101 64=>0b110 128=>0b111
54:56	WOX	RX_BER_TIMER_SEL: PP Diag BER Timer saturation select. Selects the timer value that will saturate the timer and cause a freeze event. 0b000 = 2^39 0b001 = 2^35 0b010 = 2^31 0b011 = 2^27 0b100 = 2^25 0b101 = 2^21 0b110 = 2^17 0b111 = 2^13 Values: 2TOTHE39TH=>0b000 2TOTHE35TH=>0b001 2TOTHE31ST=>0b010 2TOTHE27TH=>0b011 2TOTHE25TH=>0b100 2TOTHE21TH=>0b101 2TOTHE17TH=>0b110 2TOTHE13TH=>0b111
57	WOX	RX_BER_CLR_COUNT_ON_READ_EN: PP Diag BER Lane Error Counter clear on read. When set to a 1 this enables the clearing of a lanes error counter when it is read.
58	WOX	RX_BER_CLR_TIMER_ON_READ_EN: PP Diag BER Timer clear on read. When set to a 1 this enables the clearing of a lanes per-pack timer when it is read from any lane in the pack.
59:63	RO	constant=0b00000

Register Name	***RX BER Mode Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_MODE_PP
Address	800B58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_TIMER_FREEZE_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) Timer freeze enable. When set to a 1 the per-pack timer is frozen when any lane error count saturates in that pack.

Bits	SCOM	Field Mnemonic: Description
49	WOX	RX_BER_COUNT_FREEZE_EN: PP Diag BER Lane Error Counter freeze enable. When set to a 1 the per-lane error counters are frozen when the timer saturates in that pack.
50	RO	constant=0b0
51:53	WOX	RX_BER_COUNT_SEL: PP Diag BER Lane Error Counter saturation select. Selects the number of errors that will saturate the counter and cause a freeze event. 0b000 = 1 0b001 = 2 0b010 = 4 0b011 = 8 0b100 = 16 0b101 = 32 0b110 = 64 0b111 = 128 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100 32=>0b101 64=>0b110 128=>0b111
54:56	WOX	RX_BER_TIMER_SEL: PP Diag BER Timer saturation select. Selects the timer value that will saturate the timer and cause a freeze event. 0b000 = 2^39 0b001 = 2^35 0b010 = 2^31 0b011 = 2^27 0b100 = 2^25 0b101 = 2^21 0b110 = 2^17 0b111 = 2^13 Values: 2TOTHE39TH=>0b000 2TOTHE35TH=>0b001 2TOTHE31ST=>0b010 2TOTHE27TH=>0b011 2TOTHE25TH=>0b100 2TOTHE21TH=>0b101 2TOTHE17TH=>0b110 2TOTHE13TH=>0b111
57	WOX	RX_BER_CLR_COUNT_ON_READ_EN: PP Diag BER Lane Error Counter clear on read. When set to a 1 this enables the clearing of a lanes error counter when it is read.
58	WOX	RX_BER_CLR_TIMER_ON_READ_EN: PP Diag BER Timer clear on read. When set to a 1 this enables the clearing of a lanes per-pack timer when it is read from any lane in the pack.
59:63	RO	constant=0b00000

Register Name	***RX BER Mode Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_MODE_PP
Address	800B58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BER_TIMER_FREEZE_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) Timer freeze enable. When set to a 1 the per-pack timer is frozen when any lane error count saturates in that pack.
49	WOX	RX_BER_COUNT_FREEZE_EN: PP Diag BER Lane Error Counter freeze enable. When set to a 1 the per-lane error counters are frozen when the timer saturates in that pack.
50	RO	constant=0b0
51:53	WOX	RX_BER_COUNT_SEL: PP Diag BER Lane Error Counter saturation select. Selects the number of errors that will saturate the counter and cause a freeze event. 0b000 = 1 0b001 = 2 0b010 = 4 0b011 = 8 0b100 = 16 0b101 = 32 0b110 = 64 0b111 = 128 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100 32=>0b101 64=>0b110 128=>0b111
54:56	WOX	RX_BER_TIMER_SEL: PP Diag BER Timer saturation select. Selects the timer value that will saturate the timer and cause a freeze event. 0b000 = 2^39 0b001 = 2^35 0b010 = 2^31 0b011 = 2^27 0b100 = 2^25 0b101 = 2^21 0b110 = 2^17 0b111 = 2^13 Values: 2TOTHE39TH=>0b000 2TOTHE35TH=>0b001 2TOTHE31ST=>0b010 2TOTHE27TH=>0b011 2TOTHE25TH=>0b100 2TOTHE21TH=>0b101 2TOTHE17TH=>0b110 2TOTHE13TH=>0b111
57	WOX	RX_BER_CLR_COUNT_ON_READ_EN: PP Diag BER Lane Error Counter clear on read. When set to a 1 this enables the clearing of a lanes error counter when it is read.
58	WOX	RX_BER_CLR_TIMER_ON_READ_EN: PP Diag BER Timer clear on read. When set to a 1 this enables the clearing of a lanes per-pack timer when it is read from any lane in the pack.
59:63	RO	constant=0b00000

Register Name	***RX BER Mode Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BER_MODE_PP
Address	800B58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_BER_TIMER_FREEZE_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) Timer freeze enable. When set to a 1 the per-pack timer is frozen when any lane error count saturates in that pack.
49	WOX	RX_BER_COUNT_FREEZE_EN: PP Diag BER Lane Error Counter freeze enable. When set to a 1 the per-lane error counters are frozen when the timer saturates in that pack.
50	RO	constant=0b0
51:53	WOX	RX_BER_COUNT_SEL: PP Diag BER Lane Error Counter saturation select. Selects the number of errors that will saturate the counter and cause a freeze event. 0b000 = 1 0b001 = 2 0b010 = 4 0b011 = 8 0b100 = 16 0b101 = 32 0b110 = 64 0b111 = 128 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100 32=>0b101 64=>0b110 128=>0b111
54:56	WOX	RX_BER_TIMER_SEL: PP Diag BER Timer saturation select. Selects the timer value that will saturate the timer and cause a freeze event. 0b000 = 2^39 0b001 = 2^35 0b010 = 2^31 0b011 = 2^27 0b100 = 2^25 0b101 = 2^21 0b110 = 2^17 0b111 = 2^13 Values: 2TOTHE39TH=>0b000 2TOTHE35TH=>0b001 2TOTHE31ST=>0b010 2TOTHE27TH=>0b011 2TOTHE25TH=>0b100 2TOTHE21TH=>0b101 2TOTHE17TH=>0b110 2TOTHE13TH=>0b111
57	WOX	RX_BER_CLR_COUNT_ON_READ_EN: PP Diag BER Lane Error Counter clear on read. When set to a 1 this enables the clearing of a lanes error counter when it is read.
58	WOX	RX_BER_CLR_TIMER_ON_READ_EN: PP Diag BER Timer clear on read. When set to a 1 this enables the clearing of a lanes per-pack timer when it is read from any lane in the pack.
59:63	RO	constant=0b00000

Register Name	***RX BER Mode Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_BER_MODE_PP
Address	800B58000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_BER_TIMER_FREEZE_EN: Per-Pack (PP) Diagnostic Bit Error Rate (BER) Timer freeze enable. When set to a 1 the per-pack timer is frozen when any lane error count saturates in that pack.
49	WOX	RX_BER_COUNT_FREEZE_EN: PP Diag BER Lane Error Counter freeze enable. When set to a 1 the per-lane error counters are frozen when the timer saturates in that pack.
50	RO	constant=0b0
51:53	WOX	RX_BER_COUNT_SEL: PP Diag BER Lane Error Counter saturation select. Selects the number of errors that will saturate the counter and cause a freeze event. 0b000 = 1 0b001 = 2 0b010 = 4 0b011 = 8 0b100 = 16 0b101 = 32 0b110 = 64 0b111 = 128 Values: 1=>0b000 2=>0b001 4=>0b010 8=>0b011 16=>0b100 32=>0b101 64=>0b110 128=>0b111
54:56	WOX	RX_BER_TIMER_SEL: PP Diag BER Timer saturation select. Selects the timer value that will saturate the timer and cause a freeze event. 0b000 = 2^39 0b001 = 2^35 0b010 = 2^31 0b011 = 2^27 0b100 = 2^25 0b101 = 2^21 0b110 = 2^17 0b111 = 2^13 Values: 2TOTHE39TH=>0b000 2TOTHE35TH=>0b001 2TOTHE31ST=>0b010 2TOTHE27TH=>0b011 2TOTHE25TH=>0b100 2TOTHE21TH=>0b101 2TOTHE17TH=>0b110 2TOTHE13TH=>0b111
57	WOX	RX_BER_CLR_COUNT_ON_READ_EN: PP Diag BER Lane Error Counter clear on read. When set to a 1 this enables the clearing of a lanes error counter when it is read.
58	WOX	RX_BER_CLR_TIMER_ON_READ_EN: PP Diag BER Timer clear on read. When set to a 1 this enables the clearing of a lanes per-pack timer when it is read from any lane in the pack.

Bits	SCOM	Field Mnemonic: Description
59:63	RO	constant=0b00000

Register Name	*RX Servo Timeout Select Regs 1*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SERVO_TO1_PP
Address	800B60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	RX_SERVO_TIMEOUT_SEL_A: RX servo operation timeout A used to time latch offset calibration.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	RX_SERVO_TIMEOUT_SEL_B: RX servo operation timeout B used to time CLTE/peaking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	RX_SERVO_TIMEOUT_SEL_C: RX servo operation timeout C used to time vref adjustment.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_SERVO_TIMEOUT_SEL_D: RX servo operation timeout D used to time block locking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO1_PP
Address	800B60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_A: RX servo operation timeout A used to time latch offset calibration.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_B: RX servo operation timeout B used to time CLTE/peaking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_C: RX servo operation timeout C used to time vref adjustment.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_D: RX servo operation timeout D used to time block locking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO1_PP
Address	800B60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_A: RX servo operation timeout A used to time latch offset calibration.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_B: RX servo operation timeout B used to time CLTE/peaking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_C: RX servo operation timeout C used to time vref adjustment.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_D: RX servo operation timeout D used to time block locking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO1_PP
Address	800B60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_A: RX servo operation timeout A used to time latch offset calibration.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_B: RX servo operation timeout B used to time CLTE/peaking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_C: RX servo operation timeout C used to time vref adjustment.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_D: RX servo operation timeout D used to time block locking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO1_PP
Address	800B60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_A: RX servo operation timeout A used to time latch offset calibration.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_B: RX servo operation timeout B used to time CLTE/peaking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_C: RX servo operation timeout C used to time vref adjustment.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_D: RX servo operation timeout D used to time block locking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO1_PP
Address	800B60000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_A: RX servo operation timeout A used to time latch offset calibration.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_B: RX servo operation timeout B used to time CLTE/peaking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_C: RX servo operation timeout C used to time vref adjustment.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_D: RX servo operation timeout D used to time block locking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Servo Timeout Select Regs 2*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SERVO_TO2_PP
Address	800B68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_SERVO_TIMEOUT_SEL_E: RX servo operation timeout E used to time edge tracking .. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	RX_SERVO_TIMEOUT_SEL_F: RX servo operation timeout F used to time eye tracking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	RX_SERVO_TIMEOUT_SEL_G: RX servo operation timeout G used to time BER testing.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_SERVO_TIMEOUT_SEL_H: RX servo operation timeout H used to time EDI Dynamic data centering and EI-4 clock duty cycle distortion adjust.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Servo Timeout Select Regs 2*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO2_PP
Address	800B68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_E: RX servo operation timeout E used to time edge tracking .. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_F: RX servo operation timeout F used to time eye tracking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_G: RX servo operation timeout G used to time BER testing.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_H: RX servo operation timeout H used to time EDI Dynamic data centering and EI-4 clock duty cycle distortion adjust.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO2_PP
Address	800B68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_E: RX servo operation timeout E used to time edge tracking .. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_F: RX servo operation timeout F used to time eye tracking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_G: RX servo operation timeout G used to time BER testing.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_H: RX servo operation timeout H used to time EDI Dynamic data centering and EI-4 clock duty cycle distortion adjust.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO2_PP
Address	800B68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_E: RX servo operation timeout E used to time edge tracking .. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_F: RX servo operation timeout F used to time eye tracking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_G: RX servo operation timeout G used to time BER testing.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_H: RX servo operation timeout H used to time EDI Dynamic data centering and EI-4 clock duty cycle distortion adjust.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO2_PP
Address	800B68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_E: RX servo operation timeout E used to time edge tracking .. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_F: RX servo operation timeout F used to time eye tracking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_G: RX servo operation timeout G used to time BER testing.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_H: RX servo operation timeout H used to time EDI Dynamic data centering and EI-4 clock duty cycle distortion adjust.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO2_PP
Address	800B68000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_E: RX servo operation timeout E used to time edge tracking .. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_F: RX servo operation timeout F used to time eye tracking.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_G: RX servo operation timeout G used to time BER testing.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_H: RX servo operation timeout H used to time EDI Dynamic data centering and EI-4 clock duty cycle distortion adjust.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SERVO_TO3_PP
Address	800B70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_SERVO_TIMEOUT_SEL_I: RX servo operation timeout I used to time Ap and An measurements without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	RX_SERVO_TIMEOUT_SEL_J: RX servo operation timeout J used to time Ap and An measurements with DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	RX_SERVO_TIMEOUT_SEL_K: RX servo operation timeout K used to time Amin measurements with or without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_SERVO_TIMEOUT_SEL_L: RX servo operation timeout L used to time phase rotator bump commands.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO3_PP
Address	800B70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_I: RX servo operation timeout I used to time Ap and An measurements without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_J: RX servo operation timeout J used to time Ap and An measurements with DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_K: RX servo operation timeout K used to time Amin measurements with or without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_SERVO_TIMEOUT_SEL_L: RX servo operation timeout L used to time phase rotator bump commands.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO3_PP
Address	800B70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_I: RX servo operation timeout I used to time Ap and An measurements without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_SERVO_TIMEOUT_SEL_J: RX servo operation timeout J used to time Ap and An measurements with DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
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Bits	SCOM	Field Mnemonic: Description
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Register Name	***RX Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO3_PP
Address	800B70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_I: RX servo operation timeout I used to time Ap and An measurements without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
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Bits	SCOM	Field Mnemonic: Description
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Register Name	***RX Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO3_PP
Address	800B70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_I: RX servo operation timeout I used to time Ap and An measurements without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

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Register Name	***RX Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_SERVO_TO3_PP
Address	800B70000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_SERVO_TIMEOUT_SEL_I: RX servo operation timeout I used to time Ap and An measurements without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

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Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_SERVO_TIMEOUT_SEL_K: RX servo operation timeout K used to time Amin measurements with or without DFE.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
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Register Name	***RX DFE Configuration Register***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DFE_CONFIG_PP
Address	800B78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RWX	RX_PEAK_CFG: RX DFE Peaking settings.
50:52	RWX	RX_AMIN_CFG: RX DFE Amin settings.
53:54	RWX	RX_ANAP_CFG: RX DFE An-Ap settings.
55:56	RWX	RX_H1_CFG: RX DFE H1 settings.
57:59	RWX	RX_H1AP_CFG: RX DFE H1 over Ap settings.
60:61	RWX	RX_DFE_CA_CFG: RX DFE clock adjust settings.
62:63	RWX	RX_SPMUX_CFG: RX DFE speculation mux toggle settings.

Register Name	*RX DFE Configuration Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_CONFIG_PP
Address	800B78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	RX_PEAK_CFG: RX DFE Peaking settings.
50:52	WOX	RX_AMIN_CFG: RX DFE Amin settings.
53:54	WOX	RX_ANAP_CFG: RX DFE An-Ap settings.
55:56	WOX	RX_H1_CFG: RX DFE H1 settings.
57:59	WOX	RX_H1AP_CFG: RX DFE H1 over Ap settings.
60:61	WOX	RX_DFE_CA_CFG: RX DFE clock adjust settings.
62:63	WOX	RX_SPMUX_CFG: RX DFE speculation mux toggle settings.

Register Name	*RX DFE Configuration Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_CONFIG_PP
Address	800B78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	RX_PEAK_CFG: RX DFE Peaking settings.
50:52	WOX	RX_AMIN_CFG: RX DFE Amin settings.
53:54	WOX	RX_ANAP_CFG: RX DFE An-Ap settings.
55:56	WOX	RX_H1_CFG: RX DFE H1 settings.
57:59	WOX	RX_H1AP_CFG: RX DFE H1 over Ap settings.
60:61	WOX	RX_DFE_CA_CFG: RX DFE clock adjust settings.
62:63	WOX	RX_SPMUX_CFG: RX DFE speculation mux toggle settings.

Register Name	*RX DFE Configuration Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_CONFIG_PP
Address	800B78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	RX_PEAK_CFG: RX DFE Peaking settings.

Bits	SCOM	Field Mnemonic: Description
50:52	WOX	RX_AMIN_CFG: RX DFE Amin settings.
53:54	WOX	RX_ANAP_CFG: RX DFE An-Ap settings.
55:56	WOX	RX_H1_CFG: RX DFE H1 settings.
57:59	WOX	RX_H1AP_CFG: RX DFE H1 over Ap settings.
60:61	WOX	RX_DFE_CA_CFG: RX DFE clock adjust settings.
62:63	WOX	RX_SPMUX_CFG: RX DFE speculation mux toggle settings.

Register Name	***RX DFE Configuration Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_CONFIG_PP
Address	800B78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	WOX	RX_PEAK_CFG: RX DFE Peaking settings.
50:52	WOX	RX_AMIN_CFG: RX DFE Amin settings.
53:54	WOX	RX_ANAP_CFG: RX DFE An-Ap settings.
55:56	WOX	RX_H1_CFG: RX DFE H1 settings.
57:59	WOX	RX_H1AP_CFG: RX DFE H1 over Ap settings.
60:61	WOX	RX_DFE_CA_CFG: RX DFE clock adjust settings.
62:63	WOX	RX_SPMUX_CFG: RX DFE speculation mux toggle settings.

Register Name	***RX DFE Configuration Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_DFE_CONFIG_PP
Address	800B78000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	WOX	RX_PEAK_CFG: RX DFE Peaking settings.
50:52	WOX	RX_AMIN_CFG: RX DFE Amin settings.
53:54	WOX	RX_ANAP_CFG: RX DFE An-Ap settings.
55:56	WOX	RX_H1_CFG: RX DFE H1 settings.
57:59	WOX	RX_H1AP_CFG: RX DFE H1 over Ap settings.
60:61	WOX	RX_DFE_CA_CFG: RX DFE clock adjust settings.
62:63	WOX	RX_SPMUX_CFG: RX DFE speculation mux toggle settings.

Register Name	*RX DFE Timers Configuration Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_DFE_TIMERS_PP
Address	800B80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	RX_INIT_TMR_CFG: RX clock init timer settings.
51:53	RWX	RX_BER_CFG: RX DDC Bit error rate timer settings.
54:55	RWX	RX_FIFO_DLY_CFG: RX Fifo Delay Blackout settings.
56:57	RWX	RX_DDC_CFG: RX DDC config settings.
58:60	RWX	RX_DAC_BO_CFG: RX DAC black out period settings.
61:62	RWX	RX_PROT_CFG: RX phase rotator filter settings.
63	RO	constant=0b0

Register Name	*RX DFE Timers Configuration Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_TIMERS_PP
Address	800B80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	WOX	RX_INIT_TMR_CFG: RX clock init timer settings.
51:53	WOX	RX_BER_CFG: RX DDC Bit error rate timer settings.
54:55	WOX	RX_FIFO_DLY_CFG: RX Fifo Delay Blackout settings.
56:57	WOX	RX_DDC_CFG: RX DDC config settings.
58:60	WOX	RX_DAC_BO_CFG: RX DAC black out period settings.
61:62	WOX	RX_PROT_CFG: RX phase rotator filter settings.
63	RO	constant=0b0

Register Name	*RX DFE Timers Configuration Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_TIMERS_PP
Address	800B80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	WOX	RX_INIT_TMR_CFG: RX clock init timer settings.

Bits	SCOM	Field Mnemonic: Description
51:53	WOX	RX_BER_CFG: RX DDC Bit error rate timer settings.
54:55	WOX	RX_FIFO_DLY_CFG: RX Fifo Delay Blackout settings.
56:57	WOX	RX_DDC_CFG: RX DDC config settings.
58:60	WOX	RX_DAC_BO_CFG: RX DAC black out period settings.
61:62	WOX	RX_PROT_CFG: RX phase rotator filter settings.
63	RO	constant=0b0

Register Name	***RX DFE Timers Configuration Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_TIMERS_PP
Address	800B80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	WOX	RX_INIT_TMR_CFG: RX clock init timer settings.
51:53	WOX	RX_BER_CFG: RX DDC Bit error rate timer settings.
54:55	WOX	RX_FIFO_DLY_CFG: RX Fifo Delay Blackout settings.
56:57	WOX	RX_DDC_CFG: RX DDC config settings.
58:60	WOX	RX_DAC_BO_CFG: RX DAC black out period settings.
61:62	WOX	RX_PROT_CFG: RX phase rotator filter settings.
63	RO	constant=0b0

Register Name	***RX DFE Timers Configuration Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_DFE_TIMERS_PP
Address	800B80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	WOX	RX_INIT_TMR_CFG: RX clock init timer settings.
51:53	WOX	RX_BER_CFG: RX DDC Bit error rate timer settings.
54:55	WOX	RX_FIFO_DLY_CFG: RX Fifo Delay Blackout settings.
56:57	WOX	RX_DDC_CFG: RX DDC config settings.
58:60	WOX	RX_DAC_BO_CFG: RX DAC black out period settings.
61:62	WOX	RX_PROT_CFG: RX phase rotator filter settings.
63	RO	constant=0b0

Register Name	*RX DFE Timers Configuration Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_DFE_TIMERS_PP
Address	800B80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	WOX	RX_INIT_TMR_CFG: RX clock init timer settings.
51:53	WOX	RX_BER_CFG: RX DDC Bit error rate timer settings.
54:55	WOX	RX_FIFO_DLY_CFG: RX Fifo Delay Blackout settings.
56:57	WOX	RX_DDC_CFG: RX DDC config settings.
58:60	WOX	RX_DAC_BO_CFG: RX DAC black out period settings.
61:62	WOX	RX_PROT_CFG: RX phase rotator filter settings.
63	RO	constant=0b0

Register Name	*RX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RESET_CFG_PP
Address	800B88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	RX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via rx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*RX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RESET_CFG_PP
Address	800B88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	RX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via rx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*RX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RESET_CFG_PP
Address	800B88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	RX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via rx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*RX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RESET_CFG_PP
Address	800B88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	RX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via rx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*RX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RESET_CFG_PP
Address	800B88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	RX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via rx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*RX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_RESET_CFG_PP
Address	800B88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	RX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via rx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	***RX Recal Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RECAL_TO1_PP
Address	800B90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	RX_RECAL_TIMEOUT_SEL_A: RX recal servo operation timeout A used to time latch offset calibration during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	RX_RECAL_TIMEOUT_SEL_B: RX recal servo operation timeout B used to time CTLE measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111
56:63	RO	constant=0b00000000 Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO1_PP
Address	800B90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	WOX	RX_RECAL_TIMEOUT_SEL_A: RX recal servo operation timeout A used to time latch offset calibration during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_B: RX recal servo operation timeout B used to time CTLE measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111
56:63	RO	constant=0b00000000 Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO1_PP
Address	800B90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	WOX	RX_RECAL_TIMEOUT_SEL_A: RX recal servo operation timeout A used to time latch offset calibration during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_B: RX recal servo operation timeout B used to time CTLE measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111
56:63	RO	constant=0b00000000 Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO1_PP
Address	800B90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	WOX	RX_RECAL_TIMEOUT_SEL_A: RX recal servo operation timeout A used to time latch offset calibration during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_B: RX recal servo operation timeout B used to time CTLE measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111
56:63	RO	constant=0b00000000 Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO1_PP
Address	800B90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	WOX	RX_RECAL_TIMEOUT_SEL_A: RX recal servo operation timeout A used to time latch offset calibration during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_B: RX recal servo operation timeout B used to time CTLE measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111
56:63	RO	constant=0b00000000 Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 1***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO1_PP
Address	800B90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	WOX	RX_RECAL_TIMEOUT_SEL_A: RX recal servo operation timeout A used to time latch offset calibration during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_B: RX recal servo operation timeout B used to time CTLE measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111
56:63	RO	constant=0b00000000 Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RECAL_TO2_PP
Address	800B98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000
56:59	RWX	RX_RECAL_TIMEOUT_SEL_G: RX recal servo operation timeout G Used to time BER testing during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_RECAL_TIMEOUT_SEL_H: RX recal servo operation timeout H Used to time Dynamic data centering during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Recal Servo Timeout Select Regs 2*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO2_PP
Address	800B98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_G: RX recal servo operation timeout G Used to time BER testing during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_H: RX recal servo operation timeout H Used to time Dynamic data centering during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Recal Servo Timeout Select Regs 2*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO2_PP
Address	800B98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_G: RX recal servo operation timeout G Used to time BER testing during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_H: RX recal servo operation timeout H Used to time Dynamic data centering during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Recal Servo Timeout Select Regs 2*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO2_PP
Address	800B98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_G: RX recal servo operation timeout G Used to time BER testing during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_H: RX recal servo operation timeout H Used to time Dynamic data centering during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO2_PP
Address	800B98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_G: RX recal servo operation timeout G Used to time BER testing during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_H: RX recal servo operation timeout H Used to time Dynamic data centering during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 2***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO2_PP
Address	800B98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:55	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_G: RX recal servo operation timeout G Used to time BER testing during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_H: RX recal servo operation timeout H Used to time Dynamic data centering during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Recal Servo Timeout Select Regs 3*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RECAL_TO3_PP
Address	800BA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RWX	RX_RECAL_TIMEOUT_SEL_I: RX recal servo operation timeout I used to time Ap and An measurements without DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	RWX	RX_RECAL_TIMEOUT_SEL_J: RX recal servo operation timeout J used to time Ap and An measurements with DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	RX_RECAL_TIMEOUT_SEL_K: RX recal servo operation timeout K used to time Amin measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	RWX	RX_RECAL_TIMEOUT_SEL_L: RX recal servo operation timeout L used to time bump commands during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Recal Servo Timeout Select Regs 3*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO3_PP
Address	800BA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_RECAL_TIMEOUT_SEL_I: RX recal servo operation timeout I used to time Ap and An measurements without DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_J: RX recal servo operation timeout J used to time Ap and An measurements with DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_K: RX recal servo operation timeout K used to time Amin measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_L: RX recal servo operation timeout L used to time bump commands during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	*RX Recal Servo Timeout Select Regs 3*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO3_PP
Address	800BA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_RECAL_TIMEOUT_SEL_I: RX recal servo operation timeout I used to time Ap and An measurements without DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_J: RX recal servo operation timeout J used to time Ap and An measurements with DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_K: RX recal servo operation timeout K used to time Amin measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_L: RX recal servo operation timeout L used to time bump commands during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO3_PP
Address	800BA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_RECAL_TIMEOUT_SEL_I: RX recal servo operation timeout I used to time Ap and An measurements without DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_J: RX recal servo operation timeout J used to time Ap and An measurements with DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_K: RX recal servo operation timeout K used to time Amin measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_L: RX recal servo operation timeout L used to time bump commands during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO3_PP
Address	800BA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_RECAL_TIMEOUT_SEL_I: RX recal servo operation timeout I used to time Ap and An measurements without DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_J: RX recal servo operation timeout J used to time Ap and An measurements with DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_K: RX recal servo operation timeout K used to time Amin measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_L: RX recal servo operation timeout L used to time bump commands during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal Servo Timeout Select Regs 3***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_RECAL_TO3_PP
Address	800BA0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	WOX	RX_RECAL_TIMEOUT_SEL_I: RX recal servo operation timeout I used to time Ap and An measurements without DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:55	WOX	RX_RECAL_TIMEOUT_SEL_J: RX recal servo operation timeout J used to time Ap and An measurements with DFE during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
56:59	WOX	RX_RECAL_TIMEOUT_SEL_K: RX recal servo operation timeout K used to time Amin measurements during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Bits	SCOM	Field Mnemonic: Description
60:63	WOX	RX_RECAL_TIMEOUT_SEL_L: RX recal servo operation timeout L used to time bump commands during recal.. 0b0000 = 0b0001 = 512 UI 0b0010 = 1K UI 0b0011 = 2K UI 0b0100 = 4096 UI 0b0101 = 8K UI 0b0110 = 16K UI 0b0111 = 32K UI 0b1000 = 64K UI 0b1001 = 128K UI 0b1010 = 256K UI 0b1011 = 512K UI 0b1100 = 1M UI 0b1101 = 2M UI 0b1110 = 4M UI 0b1111 = Infinite Values: 16UI=>0b0000 512UI=>0b0001 1KUI=>0b0010 2KUI=>0b0011 4KUI=>0b0100 8KUI=>0b0101 16KUI=>0b0110 32KUI=>0b0111 64KUI=>0b1000 128KUI=>0b1001 256KUI=>0b1010 512KUI=>0b1011 1MUI=>0b1100 2MUI=>0b1101 4MUI=>0b1110 INFINITE=>0b1111

Register Name	***RX Recal In Progress Control***
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_RECAL_CNTL_PP
Address	800BA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	RX_RECAL_IN_PROGRESS: NO LONGER USED--REMOVE for DD2 design.
49:63	RO	constant=0b000000000000000

Register Name	***RX Recal In Progress Control***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_CNTL_PP
Address	800BA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_RECAL_IN_PROGRESS: NO LONGER USED--REMOVE for DD2 design.
49:63	RO	constant=0b000000000000000

Register Name	***RX Recal In Progress Control***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_CNTL_PP
Address	800BA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_RECAL_IN_PROGRESS: NO LONGER USED--REMOVE for DD2 design.
49:63	RO	constant=0b000000000000000

Register Name	***RX Recal In Progress Control***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_CNTL_PP
Address	800BA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_RECAL_IN_PROGRESS: NO LONGER USED--REMOVE for DD2 design.
49:63	RO	constant=0b000000000000000

Register Name	***RX Recal In Progress Control***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_RECAL_CNTL_PP
Address	800BA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_RECAL_IN_PROGRESS: NO LONGER USED--REMOVE for DD2 design.
49:63	RO	constant=0b000000000000000

Register Name	*RX Recal In Progress Control*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_RECAL_CNTL_PP
Address	800BA8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_RECAL_IN_PROGRESS: NO LONGER USED--REMOVE for DD2 design.
49:63	RO	constant=0b000000000000000

Register Name	*RX Mode2 Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_MODE2_PP
Address	800BB0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	RX_PP_TRC_MODE: Per Pack RX Trace Mode. 0b000 = TBD 0b001 = TBD 0b010 = TBD 0b011 = TBD 0b100 = TBD 0b101 = TBD 0b110 = TBD 0b111 = TBD Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:52	RWX	RX_BIST_JITTER_PULSE_SEL: RX BIST Jitter Select. This setting induces artificial jitter into the data of the PRBS generator during BIST to ensure the deadzone between the two eyes of the BIST pattern is at least two PR steps wide.. JGR 0b00 = Four Jitter Steps 0b01 = Eight Jitter Steps 0b10 = Two Jitter Steps 0b11 = No Jitter Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11

Bits	SCOM	Field Mnemonic: Description
53	RO	constant=0b0 Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
54:59	RWX	RX_BIST_MIN_EYE_WIDTH: RX BIST Min Eye Width. Sets the minimum eye width value in phase rotator steps considered acceptable in order to pass PHYBIST.. JGR
60	RO	constant=0b0
61:62	RWX	RX_WT_PATTERN_LENGTH: RX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
63	RO	constant=0b0 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	***RX Mode2 Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE2_PP
Address	800BB0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	WOX	RX_PP_TRC_MODE: Per Pack RX Trace Mode. 0b000 = TBD 0b001 = TBD 0b010 = TBD 0b011 = TBD 0b100 = TBD 0b101 = TBD 0b110 = TBD 0b111 = TBD Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
51:52	WOX	RX_BIST_JITTER_PULSE_SEL: RX BIST Jitter Select. This setting induces artificial jitter into the data of the PRBS generator during BIST to ensure the deadzone between the two eyes of the BIST pattern is at least two PR steps wide.. JGR 0b00 = Four Jitter Steps 0b01 = Eight Jitter Steps 0b10 = Two Jitter Steps 0b11 = No Jitter Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
53	RO	constant=0b0 Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
54:59	WOX	RX_BIST_MIN_EYE_WIDTH: RX BIST Min Eye Width. Sets the minimum eye width value in phase rotator steps considered acceptable in order to pass PHYBIST.. JGR
60	RO	constant=0b0
61:62	WOX	RX_WT_PATTERN_LENGTH: RX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
63	RO	constant=0b0 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	***RX Mode2 Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE2_PP
Address	800BB0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	WOX	RX_PP_TRC_MODE: Per Pack RX Trace Mode. 0b000 = TBD 0b001 = TBD 0b010 = TBD 0b011 = TBD 0b100 = TBD 0b101 = TBD 0b110 = TBD 0b111 = TBD Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:52	WOX	RX_BIST_JITTER_PULSE_SEL: RX BIST Jitter Select. This setting induces artificial jitter into the data of the PRBS generator during BIST to ensure the deadzone between the two eyes of the BIST pattern is at least two PR steps wide.. JGR 0b00 = Four Jitter Steps 0b01 = Eight Jitter Steps 0b10 = Two Jitter Steps 0b11 = No Jitter Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
53	RO	constant=0b0 Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
54:59	WOX	RX_BIST_MIN_EYE_WIDTH: RX BIST Min Eye Width. Sets the minimum eye width value in phase rotator steps considered acceptable in order to pass PHYBIST.. JGR
60	RO	constant=0b0
61:62	WOX	RX_WT_PATTERN_LENGTH: RX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
63	RO	constant=0b0 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	***RX Mode2 Per-Pack Shadow Register***
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE2_PP
Address	800BB0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	WOX	RX_PP_TRC_MODE: Per Pack RX Trace Mode. 0b000 = TBD 0b001 = TBD 0b010 = TBD 0b011 = TBD 0b100 = TBD 0b101 = TBD 0b110 = TBD 0b111 = TBD Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:52	WOX	RX_BIST_JITTER_PULSE_SEL: RX BIST Jitter Select. This setting induces artificial jitter into the data of the PRBS generator during BIST to ensure the deadzone between the two eyes of the BIST pattern is at least two PR steps wide.. JGR 0b00 = Four Jitter Steps 0b01 = Eight Jitter Steps 0b10 = Two Jitter Steps 0b11 = No Jitter Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
53	RO	constant=0b0 Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
54:59	WOX	RX_BIST_MIN_EYE_WIDTH: RX BIST Min Eye Width. Sets the minimum eye width value in phase rotator steps considered acceptable in order to pass PHYBIST.. JGR
60	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
61:62	WOX	RX_WT_PATTERN_LENGTH: RX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
63	RO	constant=0b0 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*RX Mode2 Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_MODE2_PP
Address	800BB0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	WOX	RX_PP_TRC_MODE: Per Pack RX Trace Mode. 0b000 = TBD 0b001 = TBD 0b010 = TBD 0b011 = TBD 0b100 = TBD 0b101 = TBD 0b110 = TBD 0b111 = TBD Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
51:52	WOX	RX_BIST_JITTER_PULSE_SEL: RX BIST Jitter Select. This setting induces artificial jitter into the data of the PRBS generator during BIST to ensure the deadzone between the two eyes of the BIST pattern is at least two PR steps wide.. JGR 0b00 = Four Jitter Steps 0b01 = Eight Jitter Steps 0b10 = Two Jitter Steps 0b11 = No Jitter Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
53	RO	constant=0b0 Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
54:59	WOX	RX_BIST_MIN_EYE_WIDTH: RX BIST Min Eye Width. Sets the minimum eye width value in phase rotator steps considered acceptable in order to pass PHYBIST.. JGR
60	RO	constant=0b0
61:62	WOX	RX_WT_PATTERN_LENGTH: RX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
63	RO	constant=0b0 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*RX Mode2 Per-Pack Shadow Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_MODE2_PP
Address	800BB0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	WOX	RX_PP_TRC_MODE: Per Pack RX Trace Mode. 0b000 = TBD 0b001 = TBD 0b010 = TBD 0b011 = TBD 0b100 = TBD 0b101 = TBD 0b110 = TBD 0b111 = TBD Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111
51:52	WOX	RX_BIST_JITTER_PULSE_SEL: RX BIST Jitter Select. This setting induces artificial jitter into the data of the PRBS generator during BIST to ensure the deadzone between the two eyes of the BIST pattern is at least two PR steps wide.. JGR 0b00 = Four Jitter Steps 0b01 = Eight Jitter Steps 0b10 = Two Jitter Steps 0b11 = No Jitter Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
53	RO	constant=0b0 Values: STEPS4=>0b00 STEPS8=>0b01 STEPS2=>0b10 STEPS0=>0b11
54:59	WOX	RX_BIST_MIN_EYE_WIDTH: RX BIST Min Eye Width. Sets the minimum eye width value in phase rotator steps considered acceptable in order to pass PHYBIST.. JGR
60	RO	constant=0b0
61:62	WOX	RX_WT_PATTERN_LENGTH: RX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
63	RO	constant=0b0 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*RX BIST Control Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_BIST_GCRMSG_PP
Address	800BB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	RX_BIST_EN: This bit enables the RX BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run RX BIST set the rx_start_bist reg bit.. JGR
49:63	RO	constant=0b000000000000000

Register Name	*RX BIST Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BIST_GCRMSG_PP
Address	800BB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_BIST_EN: This bit enables the RX BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run RX BIST set the rx_start_bist register bit.. JGR
49:63	RO	constant=0b000000000000000

Register Name	*RX BIST Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BIST_GCRMSG_PP
Address	800BB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	RX_BIST_EN: This bit enables the RX BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run RX BIST set the rx_start_bist regsiter bit.. JGR
49:63	RO	constant=0b000000000000000

Register Name	*RX BIST Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BIST_GCRMSG_PP
Address	800BB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BIST_EN: This bit enables the RX BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run RX BIST set the rx_start_bist reg bit.. JGR
49:63	RO	constant=0b000000000000000

Register Name	*RX BIST Control Register*
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_BIST_GCRMSG_PP
Address	800BB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BIST_EN: This bit enables the RX BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run RX BIST set the rx_start_bist reg bit.. JGR
49:63	RO	constant=0b000000000000000

Register Name	*RX BIST Control Register*
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_BIST_GCRMSG_PP
Address	800BB8000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	RX_BIST_EN: This bit enables the RX BIST state machine to begin testing. It is set by the BIST helper sequencer through a GCR message. To properly initialize and run RX BIST set the rx_start_bist **Register** bit.. JGR
49:63	RO	constant=0b000000000000000

Register Name	*RX Scope Control Register*
Mnemonic	DMI.RX.RXCTL.RX_CTL_REGS.RX_SCOPE_CNTL_PP
Address	800BC0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	RX_SCOPE_CONTROL: Bit 0 odd/even (1 is odd) Bit 1 speculation latch 0=0 1=1.
50	NCX	Reserved field. (Access type is rx_bump_scope_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	*RX Scope Control Register*
Mnemonic	DMI.RX.RXPACKS#0.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SCOPE_CNTL_PP
Address	800BC0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	RX_SCOPE_CONTROL: Bit 0 odd/even (1 is odd) Bit 1 speculation latch 0=0 1=1.
50	NCX	Reserved field. (Access type is rx_bump_scope_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	*RX Scope Control Register*
Mnemonic	DMI.RX.RXPACKS#1.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SCOPE_CNTL_PP
Address	800BC0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	RX_SCOPE_CONTROL: Bit 0 odd/even (1 is odd) Bit 1 speculation latch 0=0 1=1.
50	NCX	Reserved field. (Access type is rx_bump_scope_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	*RX Scope Control Register*
Mnemonic	DMI.RX.RXPACKS#2.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SCOPE_CNTL_PP
Address	800BC0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_SCOPE_CONTROL: Bit 0 odd/even (1 is odd) Bit 1 speculation latch 0=0 1=1.
50	NCX	Reserved field. (Access type is rx_bump_scope_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***RX Scope Control Register***
Mnemonic	DMI.RX.RXPACKS#3.RXPACK_DEFAULT.RXPACK.RD.RX_DATA_REGS.RX_SCOPE_CNTL_PP
Address	800BC0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_SCOPE_CONTROL: Bit 0 odd/even (1 is odd) Bit 1 speculation latch 0=0 1=1.
50	NCX	Reserved field. (Access type is rx_bump_scope_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***RX Scope Control Register***
Mnemonic	DMI.RX.RXPACKS#4.RXPACK_4.RXPACK.RD.RX_DATA_REGS.RX_SCOPE_CNTL_PP
Address	800BC0000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	RX_SCOPE_CONTROL: Bit 0 odd/even (1 is odd) Bit 1 speculation latch 0=0 1=1.
50	NCX	Reserved field. (Access type is rx_bump_scope_wo_pulse_slow_signal)
51:63	RO	constant=0b0000000000000

Register Name	***TX Per-Group Clk Mode Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_CLK_MODE_PG
Address	800C04000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_CLK_PDWN: Used to disable the TX clock and put it into a low power state. 0b0 = Clk Enabled (default) 0b1 = Clk Disabled Values: CLK_ENABLE=>0b0 CLK_DISABLE=>0b1
49	RWX	TX_CLK_INVERT: Used to invert the polarity of the clock. 0b0 = Normal Clk Polarity (default) 0b1 = Invert Clk Values: NORMAL_CLK=>0b0 INVERT_CLK=>0b1
50:51	RWX	TX_CLK_QUIESCE_P: Used to force the output of the positive differential leg of the clock lane to a particular value. Note that the 0 and 1 settings for EDI are for lab characterization only, and the circuits are not deemed to have the proper drive strength in those modes to meet production level quality. 0b00 = Functional Data (default) 0b01 = Quiesce Clock Lane to a Static 0 value 0b10 = Quiesce Clock Lane to a Static 1 value 0b11 = Tri-State Clock Lane Output Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
52:53	RWX	TX_CLK_QUIESCE_N: Used to force the output of the negative differential leg of the clock lane to a particular value. Note that the 0 and 1 settings for EDI are for lab characterization only, and the circuits are not deemed to have the proper drive strength in those modes to meet production level quality. 0b00 = Functional Data (default) 0b01 = Quiesce Clock Lane to a Static 0 value 0b10 = Quiesce Clock Lane to a Static 1 value 0b11 = Tri-State Clock Lane Output Values: FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
54	RWX	TX_CLK_DDR_MODE: Used to select TX clock QDR mode or DDR mode. 0b0 = QDR mode (default) 0b1 = DDR mode Values: QDR=>0b0 DDR=>0b1
55:63	RO	constant=0b000000000 Values: QDR=>0b0 DDR=>0b1

Register Name	***TX Per-Group Spare Mode Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_SPARE_MODE_PG
Address	800C0C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_PG_SPARE_MODE_0: Per-group spare mode latch
49	RWX	TX_PG_SPARE_MODE_1: Per-group spare mode latch
50	RWX	TX_PG_SPARE_MODE_2: Per-group spare mode latch
51	RWX	TX_PG_SPARE_MODE_3: Per-group spare mode latch
52	RWX	TX_PG_SPARE_MODE_4: Per-group spare mode latch
53	RWX	TX_PG_SPARE_MODE_5: Per-group spare mode latch
54	RWX	TX_PG_SPARE_MODE_6: Per-group spare mode latch
55	RWX	TX_PG_SPARE_MODE_7: Per-group spare mode latch
56:63	RO	constant=0b00000000

Register Name	***TX Mode Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_MODE_PG
Address	800C1C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:52	RWX	TX_MAX_BAD_LANES: Static Repair, Dynamic Repair & Recal max number of bad lanes per TX bus (NOTE: should match RX side).
53	RWX	TX_MSBSWAP: Used to enable end-for-end or msb swap of TX lanes. For example, lanes 0 and N-1 swap, lanes 1 and N-2 swap, etc. 0b0 = No swap (default) 0b1 = End-for-end swap mode Values: NOMSBSWAP=>0b0 MSBSWAP=>0b1
54	RWX	TX_PDWN_LITE_DISABLE: Disables the power down lite feature of unused spare lanes (generally should match rx_pdwn_lite_disable).
55:63	RO	constant=0b000000000

Register Name	***TX Reset Control Action Register (RCAR)***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_RESET_ACT_PG
Address	800C44000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	NCX	Reserved field. (Access type is tx_reset_cfg_ena_wo_pulse_slow_signal)
49:61	RO	constant=0b0000000000000

Bits	SCOM	Field Mnemonic: Description
62	RWX	TX_CLR_PAR_ERRS: Clear All TX Parity Error Latches. Toggle this field 0->1->0 to clear all TX parity error latches.
63	RWX	TX_FIR_RESET: FIR Reset. Toggle this field 0->1->0 to reset all TX FIR related latches including parity error latches, including the parity error latches.

Register Name	***TX BIST CLK Status Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_BIST_STAT_PG
Address	800C4C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	TX_CLK_BIST_ERR: Indicates a TXBIST clock side error occurred.. JGR 0b0 = No Error 0b1 = A clock side error has has been found Values: NO_ERROR=>0b0 ERROR=>0b1
50	RO	constant=0b0 Values: NO_ERROR=>0b0 ERROR=>0b1
51	ROX	Reserved field. (Access type is tx_clk_bist_done_ro_signal) Values: NO_ERROR=>0b0 ERROR=>0b1
52:63	RO	constant=0b000000000000 Values: NO_ERROR=>0b0 ERROR=>0b1

Register Name	***TX Per-Group FIR Error Source-Isolation Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FIR_PG
Address	800C54000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	TX_PG_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in the per-group TXCTL logic.
56:62	RO	constant=0b0000000
63	RWX	TX_PL_FIR_ERR: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-lane logic.

Register Name	*TX Per-Group FIR Error Source-Isolation Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FIR_MASK_PG
Address	800C5C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	TX_PG_FIR_ERRS_MASK: FIR mask for register or state machine parity checkers in per-group TXCTL logic. A value of 1 masks the error from generating a FIR error.. Bit0: par_err_mask_txctl_regs. Bit1: par_err_mask_gcr_buff. Bit2: Reserved.. Bit3: par_err_mask_tx_stt_rpr_snd_msg_state.. Bit4: par_err_mask_gcrs_ld_state. Bit5: par_err_mask_gcrs_unld_state. Bit6: Reserved.. Bit7: Reserved.
56:62	RO	constant=0b0000000
63	RWX	TX_PL_FIR_ERR_MASK: IOTK ALIAS: FIR mask for the per-lane TX Register checker.

Register Name	*TX Per-Group FIR Error Injection Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FIR_ERROR_INJECT_PG
Address	800C64000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	TX_PG_FIR_ERR_INJ: IOTK ALIAS: While a 1, invert the parity check bit to force an error on the per-group TXCTL register or state machine parity checkers.
56:63	RO	constant=0b00000000

Register Name	*TX Clock Group Identification 1 Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_ID1_PG
Address	800C94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RWX	TX_BUS_ID: This field is used to programmably set the bus number that a clkgrp belongs to.. DMB
54	RO	constant=0b0
55:60	RWX	TX_GROUP_ID: This field is used to programmably set the clock group number within a bus.. DMB
61:63	RO	constant=0b000

Register Name	*TX Clock Group Identification 2 Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_ID2_PG
Address	800C9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RWX	TX_LAST_GROUP_ID: This field is used to programmably set the last clock group number within a bus.. DMB
54:63	RO	constant=0b0000000000

Register Name	*TX Clock Group Identification 3 Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_ID3_PG
Address	800CA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000000000
49:55	RWX	TX_START_LANE_ID: This field is used to programmably set the first lane position in the group but relative to the bus.. DMB
56	RO	constant=0b0
57:63	RWX	TX_END_LANE_ID: This field is used to programmably set the last lane position in the group but relative to the bus.. DMB

Register Name	*TX Clock Control Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_CLK_CNTL_GCRMSG_PG
Address	800CC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000000000000
48:49	RWX	TX_DRV_CLK_PATTERN_GCRMSG: TX Clock Drive Patterns. DMB 0b00 = Drive All 0s Pattern 0b01 = Drive Wiretest Pattern 0b10 = Drive Clock Pattern 0b11 = Unused Values: DRV_0S=>0b00 DRV_WT=>0b01 DRV_C4=>0b10 UNUSED=>0b11

Bits	SCOM	Field Mnemonic: Description
50:63	RO	constant=0b00000000000000 Values: DRV_0S=>0b00 DRV_WT=>0b01 DRV_C4=>0b10 UNUSED=>0b11

Register Name	*TX FFE Test Mode Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FFE_MODE_PG
Address	800CCC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:51	RWX	TX_FFE_TEST_MODE: Driver Segment Test mode. JFG 0b00 = Mission mode enable 0b01 = Driver Output Test Mode 0b10 = Reserved 0b11 = Reserved Values: NORMAL=>0b00 SEG_TEST=>0b01 UNUSED1=>0b10 UNUSED2=>0b11
52:53	RO	constant=0b00 Values: NORMAL=>0b00 SEG_TEST=>0b01 UNUSED1=>0b10 UNUSED2=>0b11
54	RWX	TX_FFE_TEST_OVERRIDE1R: Driver Segment Test 1R Override. JFG 0b0 = Test 1R segments individually 0b1 = Test 1R segments in pairs Values: NORMAL=>0b0 OVERRIDE_1R=>0b1
55	RWX	TX_FFE_TEST_OVERRIDE2R: Driver Segment Test 2R Override. JFG 0b0 = Test 2R segments individually 0b1 = Test 2R segments with all 1R enabled Values: NORMAL=>0b0 OVERRIDE_2R=>0b1
56:63	RO	constant=0b00000000 Values: NORMAL=>0b0 OVERRIDE_2R=>0b1

Register Name	*TX FFE Main Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FFE_MAIN_PG
Address	800CD4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RWX	TX_FFE_MAIN_P_ENC: TBD. JFG
56	RO	constant=0b0
57:63	RWX	TX_FFE_MAIN_N_ENC: TBD. JFG

Register Name	*TX FFE Post Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FFE_POST_PG
Address	800CDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant=0b00000000000000000000000000000000000000000000000000
51:55	RWX	TX_FFE_POST_P_ENC: TBD This field is updated during TX BIST by logic temporarily. JFG
56:58	RO	constant=0b000
59:63	RWX	TX_FFE_POST_N_ENC: TBD. JFG

Register Name	*TX FFE Margin Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_FFE_MARGIN_PG
Address	800CE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:50	RO	constant=0b00000000000000000000000000000000000000000000000000
51:55	RWX	TX_FFE_MARGIN_P_ENC: TBD. JFG
56:58	RO	constant=0b000
59:63	RWX	TX_FFE_MARGIN_N_ENC: TBD. JFG

Register Name	*TX Bad Lanes Encoded*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_BAD_LANE_ENC_GCRMSG_PG
Address	800CEC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_BAD_LANE1_GCRMSG: GCR Message: Encoded bad lane one in relation to the entire TX bus.
55:61	RWX	TX_BAD_LANE2_GCRMSG: GCR Message: Encoded bad lane two in relation to the entire TX bus.
62:63	RWX	TX_BAD_LANE_CODE_GCRMSG: GCR Message: TX Bad Lane Code. 0b00 = Zero Bad Lanes 0b01 = Bad Lane 1 Valid 0b10 = Bad Lanes 1 and 2 Valid 0b11 = 3+ bad lanes Values: 0_BAD_LNS=>0b00 BAD_LN1_VAL=>0b01 BAD_LNS12_VAL=>0b10 3PLUS_BAD_LNS=>0b11

Register Name	***TX SLS Lane Encoded***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_SLS_LANE_ENC_GCRMSG_PG
Address	800CFC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RWX	TX_SLS_LANE_GCRMSG: GCR Message: Encoded SLS lane in relation to the entire TX bus.
55	RWX	TX_SLS_LANE_VAL_GCRMSG: GCR Message: TX SLS Lane Valid.
56:63	RO	constant=0b00000000

Register Name	***TX Wiretest Driver Segment Enable***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_WT_SEG_ENABLE_PG
Address	800D04000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_WT_EN_ALL_CLK_SEGS_GCRMSG: TX Clock Wiretest driver segnments enable.
49	RWX	TX_WT_EN_ALL_DATA_SEGS_GCRMSG: TX Data Wiretest driver segnments enable.
50:63	RO	constant=0b00000000000000

Register Name	*TX Lane Disable(d) 0 To 15 Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_LANE_DISABLED_VEC_0_15_PG
Address	800D1C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	TX_LANE_DISABLED_VEC_0_15: Lanes disabled by HW (status) or method to force lane to be disabled (save power) from software (control)..

Register Name	*TX Lane Disable(d) 16 To 31 Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_LANE_DISABLED_VEC_16_31_PG
Address	800D24000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	TX_LANE_DISABLED_VEC_16_31: Lanes disabled by HW (status) or method to force lane to be disabled (save power) from software (control)..

Register Name	*TX SLS Lane TX Mux Setting*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_SLS_LANE_MUX_GCRMSG_PG
Address	800D2C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_SLS_LANE_SHDW_GCRMSG: GCR Message: SLS lane shadowing or unshadowing functional data (used to set up TX mux controls).
49:63	RO	constant=0b000000000000000

Register Name	*TX Dynamic Repair & Recalibration Messages*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_SLV_MV_SLS_LN_REQ_GCRMSG_PG
Address	800D3C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	TX_SLV_MV_SLS_SHDW_REQ_GCRMSG: GCR Message: Request to TX Slave to Move SLS Lane.
49	RWX	TX_SLV_MV_SLS_SHDW_RPR_REQ_GCRMSG: GCR Message: Request to TX Slave to Move SLS Lane & Set Bad Lane Register.
50	RWX	TX_SLV_MV_SLS_UNSHDW_REQ_GCRMSG: GCR Message: Request to TX Slave to Move SLS Lane.
51	RWX	TX_SLV_MV_SLS_UNSHDW_RPR_REQ_GCRMSG: GCR Message: Request to TX Slave to Move SLS Lane & Set Bad Lane Register.
52:58	RWX	TX_BUS_WIDTH: GCR Message: TX Bus Width.
59	RWX	TX_SLV_MV_SLS_RPR_REQ_GCRMSG: GCR Message: Request to TX Slave to Move SLS Lane & Set Bad Lane Register.
60	RWX	TX_SLS_LANE_SEL_LG_GCRMSG: GCR Message: Sets the tx_sls_lane_sel_gcrmsg for the last good lane per bus during recal bad lane scenarios.
61	RWX	TX_SLS_LANE_UNSEL_LG_GCRMSG: GCR Message: Clears the tx_sls_lane_sel_gcrmsg for the last good lane per bus during recal bad lane scenarios.
62	RWX	TX_SPR_LNS_PDWN_LITE_GCRMSG: GCR Message: Signals the TX side to Power Down Lite (data gate) unused spare lanes at the end of static repair.
63	RO	constant=0b0

Register Name	***TX Wiretest Per-Group & Pack Shadow Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RWX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Wiretest Per-Group & Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Wiretest Per-Group & Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Wiretest Per-Group & Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Wiretest Per-Group & Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Wiretest Per-Group & Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Wiretest Per-Group & Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_WIRETEST_PP
Address	800E84000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	WOX	TX_WT_PATTERN_LENGTH: TX Wiretest Pattern Length. Specifies the length of N in the 3N-up/1N-down wiretest pattern.. 0b00 = 128 (default) 0b01 = 256 0b10 = 512 0b11 = 1024 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11
50:63	RO	constant=0b00000000000000 Values: 128=>0b00 256=>0b01 512=>0b10 1024=>0b11

Register Name	*TX Mode Per-Pack Shadow Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11
50:51	RW	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	RW	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	***TX Mode Per-Pack Shadow Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11
50:51	WOX	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11

Bits	SCOM	Field Mnemonic: Description
52:54	WOX	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	***TX Mode Per-Pack Shadow Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11

Bits	SCOM	Field Mnemonic: Description
50:51	WOX	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	*TX Mode Per-Pack Shadow Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	WOX	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11
50:51	WOX	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	***TX Mode Per-Pack Shadow Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11
50:51	WOX	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	***TX Mode Per-Pack Shadow Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11
50:51	WOX	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11
52:54	WOX	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Bits	SCOM	Field Mnemonic: Description
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	***TX Mode Per-Pack Shadow Register***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_MODE_PP
Address	800E8C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	WOX	TX_REDUCED_SCRAMBLE_MODE: Enables/Disables and sets reduced density of scramble pattern. This must be set consistent with rx_reduced_scramble_mode. 0b00 = Full density 0b01 = Full density 0b10 = Enable Div2 Reduced Density 0b11 = Enable Div4 Reduced Density (EDI only). Values: FULL_0=>0b00 FULL_1=>0b01 DIV2=>0b10 DIV4=>0b11
50:51	WOX	TX_PRBS_SCRAMBLE_MODE: Selects PRBS scramble sequence length. 0b00 = PRBS 23 (default) 0b01 = PRBS 7 (used by TX BIST) 0b10 = PRBS 11 0b11 = PRBS 15 Values: PRBS23=>0b00 PRBS7=>0b01 PRBS11=>0b10 PRBS15=>0b11

Bits	SCOM	Field Mnemonic: Description
52:54	WOX	TX_FIFO_L2U_DLY: This field is used to read or set the TX FIFO load to unload delay according to the following.. 0b000 = 0 to 2 UI 0b001 = 4 to 6 UI (default) 0b010 = 8 to 10 UI 0b011 = 12 to 14 UI 0b100 = 16 to 18 UI 0b101 = 20 to 22 UI 0b110 = 24 to 26 UI 0b111 = 28 to 30 UI Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111
55:63	RO	constant=0b000000000 Values: 0_TO_2_UI=>0b000 4_TO_6_UI=>0b001 8_TO_10_UI=>0b010 12_TO_14_UI=>0b011 16_TO_18_UI=>0b100 20_TO_22_UI=>0b101 24_TO_26_UI=>0b110 28_TO_30_UI=>0b111

Register Name	***TX SLS Command***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	RWX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	RWX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	RWX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	RWX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.
58:63	RO	constant=0b000000

Register Name	*TX SLS Command*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	WOX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	WOX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	WOX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	WOX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.
58:63	RO	constant=0b000000

Register Name	*TX SLS Command*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	WOX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	WOX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	WOX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	WOX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.
58:63	RO	constant=0b000000

Register Name	*TX SLS Command*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	WOX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	WOX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	WOX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	WOX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	WOX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.
58:63	RO	constant=0b000000

Register Name	***TX SLS Command***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	WOX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	WOX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	WOX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	WOX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	WOX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.
58:63	RO	constant=0b000000

Register Name	***TX SLS Command***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	WOX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	WOX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	WOX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	WOX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	WOX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*TX SLS Command*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_SLS_GCRMSG_PP
Address	800E94000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_SND_SLS_CMD_GCRMSG: GCR Message: Send SLS Command or Recalibration Data.
49	WOX	TX_DYN_RECAL_TSR_IGNORE_GCRMSG: GCR Message: Send Dynamic Recal SLS Commands all the time (not just during the Status Reporting interval).
50:55	WOX	TX_SLS_CMD_GCRMSG: GCR Message: TX SLS Command.
56	WOX	TX_SND_SLS_CMD_PREV_GCRMSG: GCR Message: Revert to sending previous SLS Command or Recalibration Data after recovery repair made.
57	WOX	TX_SND_SLS_USING_REG_SCRAMBLE: GCR Message: Send SLS command using normal scramble pattern instead of calibration or 9th pattern.
58:63	RO	constant=0b000000

Register Name	*TX Bit Error Injection Control A Shadow Reg*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	RWX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	RWX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	RWX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Bit Error Injection Control A Shadow Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control A Shadow Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control A Shadow Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control A Shadow Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control A Shadow Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control A Shadow Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_A_PP
Address	800E9C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_A_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern A. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_A_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern A, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_A_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern A. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_A_BER_SEL: Used to set the random bit error injection rate for pattern A. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Bit Error Injection Control B Shadow Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	RWX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	RWX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	RWX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Bit Error Injection Control B Shadow Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control B Shadow Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Bit Error Injection Control B Shadow Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Bit Error Injection Control B Shadow Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Bit Error Injection Control B Shadow Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	*TX Bit Error Injection Control B Shadow Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_B_PP
Address	800EA4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_B_RAND_BEAT_DIS: Used to disable randomization of error inject on different beats of data for pattern B. 0b0 = Error inject on random beat (0:1 on EI4, or 0:3 on EDI) (default) 0b1 = Error inject only on beat 0. Values: ENABLED=>0b0 DISABLED=>0b1

Bits	SCOM	Field Mnemonic: Description
49:51	WOX	TX_ERR_INJ_B_FINE_SEL: Random LSB/fine-grained cycle offset variation control for pattern B, where cycles are deserialized domain cycles (2 UI for EI4, 4 UI for EDI). 0b000 = Random offset in range of 1-32 cycles(default) 0b001 = Random offset in range of 1-16 cycles 0b010 = Random offset in range of 1-8 cycles 0b011 = Random offset in range of 1-4 cycles 0b100 = Random offset in range of 1-2 cycles 0b101 = Fixed offset of 1 cycle 0b110 = Fixed offset of 3 cycles 0b111 = Fixed offset of 7 cycles. Values: 1_33=>0b000 1_16=>0b001 1_8=>0b010 1_4=>0b011 1_2=>0b100 FIXED1=>0b101 FIXED3=>0b110 FIXED7=>0b111
52:55	WOX	TX_ERR_INJ_B_COARSE_SEL: Random MSB/coarse-grained multiplier for the base error rate counter, which controls bit error rate variation for pattern B. There are also a number of nonrandom settings which are specifically chosen to avoid powers of two.
56:57	RO	constant=0b00
58:63	WOX	TX_ERR_INJ_B_BER_SEL: Used to set the random bit error injection rate for pattern B. When set to a binary value of N, the average bit error rate is 1/(2^N*beats*mean(msb)).

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RWX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	RWX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX Dynamic Recalibration Timeout Selects***
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_DYN_RECAL_TIMEOUTS_PP
Address	800EAC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	WOX	TX_DYN_RECAL_INTERVAL_TIMEOUT_SEL: TX Dynamic Recalibration Interval Timeout Selects. 0b000 = 1024UI or 106.5ns very small value for sim only 0b001 = 16kUI or 1.7us 0b010 = 32kUI or 3.4us 0b011 = 64kUI or 6.8us 0b100 = 128kUI or 106.5us 0b101 = 256kUI or 1.7us 0b110 = 8192kUI or 872.4us 0b111 = infinite Values: TAP0=>0b000 TAP1=>0b001 TAP2=>0b010 TAP3=>0b011 TAP4=>0b100 TAP5=>0b101 TAP6=>0b110 TAP7=>0b111

Bits	SCOM	Field Mnemonic: Description
52:53	WOX	TX_DYN_RECAL_STATUS_RPT_TIMEOUT_SEL: TX Dynamic Recalibration Status Reporting Timeout Selects. (Note that the first 1/4 and last 1/4 of this time are actually sending the PRBS pattern, so the actual time the SLS command is on the lane is 1/2 of this value. For more info see Figure 2.4 Eye-opening Initialization Step/Recalibration Timing Description in the workbook.). 0b00 = 512UI or 53.2ns very small value for sim only 0b01 = 1024UI or 106.5ns 0b10 = 2048UI or 212.9ns 0b11 = 4096UI or 426.0ns Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11
54:63	RO	constant=0b0000000000 Values: TAP0=>0b00 TAP1=>0b01 TAP2=>0b10 TAP3=>0b11

Register Name	***TX BIST Control Register***
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	RW	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	***TX BIST Control Register***
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	WOX	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	*TX BIST Control Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	WOX	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	*TX BIST Control Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	WOX	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	*TX BIST Control Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	WOX	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	*TX BIST Control Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	WOX	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	*TX BIST Control Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BIST_CNTL_PP
Address	800EB4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_BIST_EN: This bit enables the TX BIST state machine to begin testing.. JGR
49	WOX	TX_BIST_CLR: TBD.. JGR
50:63	RO	constant=0b00000000000000

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	RWX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	RWX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000
58:63	RWX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	WOX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	WOX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000
58:63	WOX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	WOX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	WOX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000
58:63	WOX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	WOX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	WOX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000

Bits	SCOM	Field Mnemonic: Description
58:63	WOX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	WOX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	WOX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000
58:63	WOX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	WOX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	WOX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000
58:63	WOX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Bit Error Injection Control SLS Shadow Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_BER_CNTL_SLS_PP
Address	800EBC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_ERR_INJ_SLS_MODE: Used to set the random bit error injection for pattern A to work during SLS transmission only.
49	WOX	TX_ERR_INJ_SLS_ALL_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on all SLS command transmissions.
50	WOX	TX_ERR_INJ_SLS_RECAL: Used to qualify the SLS mode error injection for pattern A, to inject on the calibration lane only when not sending an SLS command.
51:57	RO	constant=0b0000000
58:63	WOX	TX_ERR_INJ_SLS_CMD: Used to qualify the SLS mode error injection for pattern A, to inject on only this SLS command transmission.

Register Name	*TX Control Per-Pack Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Control Per-Pack Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***TX Control Per-Pack Register***
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	WOX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***TX Control Per-Pack Register***
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	WOX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***TX Control Per-Pack Register***
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	WOX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	***TX Control Per-Pack Register***
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	WOX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Control Per-Pack Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_CNTL_PP
Address	800EC4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	WOX	TX_ENABLE_REDUCED_SCRAMBLE: Enables reduced density of scramble pattern. Normally this is set automatically in the functional mode training state. Users should use tx_reduced_scramble_mode to throttle density. 0b0 = Disable reduced density 0b1 = Enable reduced density per the tx_reduced_scramble_mode setting. Values: DISABLED=>0b0 ENABLED=>0b1
49:63	RO	constant=0b000000000000000 Values: DISABLED=>0b0 ENABLED=>0b1

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:63	RWX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX Configurable Reset Control Register (CRCR)*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_RESET_CFG_PP
Address	800ECC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	WOX	TX_RESET_CFG_HLD: Configurable Reset Hold List. List of functions and values to preserve state or hold value over a Configurable Reset (via tx_reset_cfg_ena). Any 1 excludes that value/function from a reset action.. List TBD.. JFG

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RWX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	RWX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	WOX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	WOX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	WOX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	WOX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	WOX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	WOX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	WOX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	WOX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	WOX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	WOX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL1_PP
Address	800ED4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	WOX	TX_TDR_DAC_CNTL: Controls Variable Threshold Receiver for TDR function. DMB
56	RO	constant=0b0
57	WOX	TX_TDR_PHASE_SEL: Controls Phase Select for TDR function, 0 is for _n loeg, 1 is for _p leg.. DMB
58:63	RO	constant=0b000000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	RWX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:59	WOX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL2_PP
Address	800EDC000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_OFFSET: Offset value for TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXCTL.TX_CTL_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RWX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#0.TXPACK_0.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#1.TXPACK_1.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#2.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:59	WOX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#3.TXPACK_DEFAULT.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#4.TXPACK_4.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX TDR Control Register*
Mnemonic	DMI.TX.TXPACKS#5.TXPACK_5.TXPACK.DD.TX_DATA_REGS.TX_TDR_CNTL3_PP
Address	800EE4000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	WOX	TX_TDR_PULSE_WIDTH: With of TDR pulse.. DMB
60:63	RO	constant=0b0000

Register Name	*TX Impedance Cal Control And Status Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_PB
Address	800F04000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	NCX	Reserved field. (Access type is tx_zcal_req_wo_pulse_slow_signal)
50	ROX	Reserved field. (Access type is tx_zcal_done_ro_signal)
51	RWX	TX_ZCAL_ERROR: Impedance Calibration Sequence Error. Indicates, independent of tx_zcal_done, whether no calibration answer was found, or state machine failed. Cleared on tx_zcal_req.. JFG
52	ROX	Reserved field. (Access type is tx_zcal_busy_ro_signal)
53	NCX	Reserved field. (Access type is tx_zcal_force_sample_wo_pulse_slow_signal)
54	ROX	Reserved field. (Access type is tx_zcal_cmp_out_ro_signal)
55:63	ROX	Reserved field. (Access type is tx_zcal_sample_cnt_ro_signal)

Register Name	*TX Impedance Cal N Value Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_NVAL_PB
Address	800F0C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:56	RWX	TX_ZCAL_N: Calibration Circuit NSeg Enable Value This holds the current value of the enabled segments and is 4x multiple of the actual segment count. May be read for current calibration result set during Calibration Sequence. May be written to immediately update circuit enables on each write. Used with tx_zcal_swo_* for manual calibration. Do not write when tx_zcal_req = 1. (binary code - 0x00 is zero slices and 0xA1 is maximum slices).. JFG
57:63	RO	constant=0b0000000

Register Name	*TX Impedance Cal P Value Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_PVAL_PB
Address	800F14000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:56	RWX	TX_ZCAL_P: Calibration Circuit PSeg Enable Value This holds the current value of the enabled segments and is 4x multiple of the actual segment count. May be read for current calibration result set during Calibration Sequence. May be written to immediately update circuit enables on each write. Used with tx_zcal_swo_* for manual calibration. Do not write when tx_zcal_req = 1. (binary code - 0x00 is zero slices and 0xA1 is maximum slices).. JFG

Bits	SCOM	Field Mnemonic: Description
57:63	RO	constant=0b0000000

Register Name	*TX Impedance Cal P 4x Value Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_P_4X_PB
Address	800F1C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RWX	TX_ZCAL_P_4X: Calibration Circuit PSeg-4X Enable Value This holds the current value of the enabled segments and is 2x multiple of the actual segment count. May be read for current calibration result set during Calibration Sequence. May be written to immediately update circuit enables on each write. Used with tx_zcal_swo_* for manual calibration. Do not write when tx_zcal_req = 1. (binary code - 0x00 is zero slices and 0x15 is maximum slices).. JFG
53:63	RO	constant=0b00000000000

Register Name	*TX Impedance Cal SW Workaround 1 Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_SWO1_PB
Address	800F24000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	TX_ZCAL_SWO_EN: Impedance Calibration Software Override. Steers all calibration controls directly from these register fields. Effectively disables state machine logic. 0b0 = Inactive. 0b1 = Enable. Values: INACTIVE=>0b0 ENABLED=>0b1
49	RWX	TX_ZCAL_SWO_CAL_SEGS: Impedance Calibration Software Bank Select. Enable PSeg calibration. 0b0 = Select NSeg bank comparison. 0b1 = Select PSeg bank comparison. Values: NSEGCAL=>0b0 PSEGCAL=>0b1
50	RWX	TX_ZCAL_SWO_CMP_INV: Impedance Calibration Software Compare Invert. Swap calibration circuit comparator inputs. 0b0 = Select NSeg bank comparison. 0b1 = Select PSeg bank comparison. Values: NSEGCAL=>0b0 PSEGCAL=>0b1

Bits	SCOM	Field Mnemonic: Description
51	RWX	TX_ZCAL_SWO_CMP_OFFSET: Impedance Calibration Software Offset Flush. Equalize comparator offset in calibration circuit. 0b0 = Disable Offset 0b1 = Enable Offset. Values: DISABLE=>0b0 ENABLE=>0b1
52	RWX	TX_ZCAL_SWO_CMP_RESET: Impedance Calibration Software Comparator reset. Reset comparator in calibration circuit. 0b0 = Disable reset 0b1 = Enable reset. Values: DISABLE=>0b0 ENABLE=>0b1
53	RWX	TX_ZCAL_SWO_POWERDOWN: Impedance Calibration Software Circuit Powerdown. Powerdown calibration circuit. (default). JFG 0b0 = Disable powerdown 0b1 = Enable powerdown. Values: DISABLE=>0b0 ENABLE=>0b1
54	RWX	TX_ZCAL_CYA_DATA_INV: Impedance Calibration CYA Sample Inversion. Select inverted comparator values in case of hardware error. 0b0 = No sample inversion 0b1 = Invert samples. Values: TRUE=>0b0 INVERT=>0b1
55	RWX	TX_ZCAL_TEST_OVR_2R: Impedance Calibration Test-Only 2R segment override. Override 2R segment enable. 0b0 = No override 0b1 = Override. Values: FALSE=>0b0 TRUE=>0b1
56:61	RO	constant=0b000000 Values: FALSE=>0b0 TRUE=>0b1
62:63	RWX	TX_ZCAL_DEBUG_MODE: Calibration Circuit Debug Mode Select. This enables outputs for use with the minikerf but does not enable the minikerf. Reference tx_minikerf.. (default). JFG 0b00 = Debug mode disabled 0b01 = probeA=rcin_p, probeB=rcin_n Observe filter input nodes, rcin_n is off-chip. 0b10 = probeA=comp_in_p, probeB=comp_in_n Observe comparator inputs. 0b11 = Debug mode disabled Values: DISABLED00=>0b00 FILTERS=>0b01 COMPARATORS=>0b10 DISABLED11=>0b11

Register Name	*TX Impedance Cal SW Workaround 2 Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_IMPCAL_SWO2_PB
Address	800F2C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RWX	TX_ZCAL_SM_MIN_VAL: Impedance Calibration Minimum Search Threshold Low-side segment count limit used in calibration process. (binary code - 0x00 is zero slices and 0x50 is maximum slices).
55:61	RWX	TX_ZCAL_SM_MAX_VAL: Impedance Calibration Maximum Search Threshold High-side segment count limit used in calibration process. (binary code - 0x00 is zero slices and 0x50 is maximum slices)
62:63	RO	constant=0b00

Register Name	*TX Iref Bias Code Input*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_ANALOG_IREF_PB
Address	800F34000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RWX	TX_IREF_BC: Bias Code for the Iref macros on the TX side. All eight 3 bit codes enable current out. The CML voltage swings of the output current will vary with this code.. SMC
51:63	RO	constant=0b0000000000000

Register Name	*TX Minikerf Control Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_MINIKERF_PB
Address	800F3C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	TX_MINIKERF: TX Minikerf Cntl Reg: . Bits (3:13) are only used when (0:2)=001. Bits (14:15) are spare. (0:2) is level 1 steering, . (0:2)=000 - reserved . (0:2)=001 - use bits (3:5) level 2 steering, (6:13) dac controls, (14:15) spare . (0:2)=010 - impedance control termref_mk_probe_ana(0:1) except on the memory buffer which uses rx_minikerf_pg . (0:2)=011 - reserved . (0:2)=100 - reserved . (0:2)=101 - tx tank pll clk on c4 pads except in the memory buffer, which has dedicated c4 pads from the clk_4t1sst_drvr.(0:2)=110 - reserved.(0:2)=111 - reserved. SMC

Register Name	*TX Initfile Version Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_INIT_VERSION_PB
Address	800F44000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	TX_INIT_VERSION: Initfile Version. This field is used to hold the initfile version for debug purposes.

Register Name	*TX Scratch Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.TX_SCRATCH_REG_PB
Address	800F4C000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RWX	TX_SCRATCH_REG: Scratch Register. This field is used to enable FW procedures to communicate.

Register Name	*Per-Bus BUSCTL FIR Error Reset Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_RESET_PB
Address	800F80000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:61	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000
62	RWX	RX_PB_CLR_PAR_ERRS: Clear All RX Parity Error Latches. Toggle this field 0->1->0 to clear parity error latches in the BUSCTL logic.
63	RWX	RX_PB_FIR_RESET: FIR Reset. Toggle this field 0->1->0 to reset the BUSCTL logic FIR related latches, including the isolation and parity error latches.

Register Name	*Per-Bus FIR Error Source-Isolation Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_PB
Address	800F88000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RWX	RX_PB_FIR_ERRS: IOTK ALIAS: A 1 in this field indicates that a register or state machine parity error has occurred in per-bus logic.
58:63	RO	constant=0b000000

Register Name	*Per-Bus FIR Error Source-Isolation Mask Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_MASK_PB
Address	800F90000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RWX	RX_PB_FIR_ERRS_MASK: IOTK ALIAS: FIR mask for rx_fir_pb errors.
58:63	RO	constant=0b000000

Register Name	*Per-Bus FIR Error Injection Register*
Mnemonic	DMI.BUSCTL.BUS_CTL_REGS.RX_FIR_ERROR_INJECT_PB
Address	800F98000201043F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RWX	RX_PB_FIR_ERRS_INJ: IOTK ALIAS: RX Per-Bus Parity Error Injection. Allows injection of non-destructive parity errors in either register or statemachine latch banks. The register or state value is not affected.
58:63	RO	constant=0b000000

5. PCB Slave 3: MEM Chiplet

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
FBIST.FBM.FBMCRCR	0x0000000003010499	1551
FBIST.FBM.FBMDCM0	0x00000000030104B8	1558
FBIST.FBM.FBMDCM1	0x00000000030104B9	1558
FBIST.FBM.FBMDCM10	0x00000000030104C2	1560
FBIST.FBM.FBMDCM11	0x00000000030104C3	1560
FBIST.FBM.FBMDCM12	0x00000000030104C4	1561
FBIST.FBM.FBMDCM13	0x00000000030104C5	1561
FBIST.FBM.FBMDCM14	0x00000000030104C6	1561
FBIST.FBM.FBMDCM15	0x00000000030104C7	1561
FBIST.FBM.FBMDCM2	0x00000000030104BA	1558
FBIST.FBM.FBMDCM3	0x00000000030104BB	1558
FBIST.FBM.FBMDCM4	0x00000000030104BC	1559
FBIST.FBM.FBMDCM5	0x00000000030104BD	1559
FBIST.FBM.FBMDCM6	0x00000000030104BE	1559
FBIST.FBM.FBMDCM7	0x00000000030104BF	1559
FBIST.FBM.FBMDCM8	0x00000000030104C0	1560
FBIST.FBM.FBMDCM9	0x00000000030104C1	1560
FBIST.FBM.FBMDCR	0x0000000003010497	1551
FBIST.FBM.FBMDMEC0	0x00000000030104B3	1556
FBIST.FBM.FBMDMEC1	0x00000000030104B4	1556
FBIST.FBM.FBMDMEC2	0x00000000030104B5	1557
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MBU.MBA01.MBA_SRQ.MBA_PMU6Q	0x000000000301043D	1488
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MBU.MBA01.MBA_SRQ.PC.MBAREF1Q	0x0000000003010433	1481
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MBU.MBA01.MBA_SRQ.PC.MBARPC1Q	0x0000000003010435	1483
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MBU.MBA01.MBA_WRD.MBABS6	0x0000000003010446	1506
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MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_0	0x0000000003010E15	1739
MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_1	0x0000000003010E16	1740
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MBU.MBA23.MBA_MCBIST.SCOMFIR.MBAFIRACT1	0x0000000003010E07	1731
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MBU.MBA23.MBA_SRQ.MBA_PMU6Q	0x0000000003010C3D	1704
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TCM.CLK_REGION	0x0000000003030006	1841
TCM.CLOCK_STAT	0x0000000003030008	1842
TCM.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000003040010	1848
TCM.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000003040011	1848
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TCM.EPS.FIR.SPA_MASK	0x0000000003040007	1846
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TCM.EPS.PSC.PSCOM_ERROR_MASK	0x0000000003010002	1463
TCM.EPS.PSC.PSCOM_MODE_REG	0x0000000003010000	1461
TCM.EPS.PSC.PSCOM_STATUS_ERROR_REG	0x0000000003010001	1462
TCM.EPS.PSC.PSCOM_WRITE_PROTECT_REG	0x0000000003010005	1464
TCM.EPS.THERM.CONTROL_REG	0x0000000003050012	1851
TCM.EPS.THERM.DTS_RESULT0	0x0000000003050000	1848
TCM.EPS.THERM.DTS_TRC_RESULT	0x0000000003050003	1848
TCM.EPS.THERM.ENC_CPM_RESULT0	0x0000000003050008	1849
TCM.EPS.THERM.ERR_STATUS_REG	0x0000000003050013	1852
TCM.EPS.THERM.INJECT_REG	0x0000000003050011	1851
TCM.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000003050016	1854
TCM.EPS.THERM.SKITTER_DATA0	0x0000000003050019	1854
TCM.EPS.THERM.SKITTER_DATA1	0x000000000305001A	1854
TCM.EPS.THERM.SKITTER_DATA2	0x000000000305001B	1854
TCM.EPS.THERM.SKITTER_FORCE_REG	0x0000000003050014	1853
TCM.EPS.THERM.SKITTER_MODE_REG	0x0000000003050010	1850
TCM.EPS.THERM.THERM_MODE_REG	0x000000000305000F	1849
TCM.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000000305001C	1855
TCM.EPS.THERM.VOLT_MODE_REG	0x0000000003050015	1853
TCM.EPS.THERM.VOLT_READ0	0x000000000305000B	1849
TCM.ERROR_STATUS	0x0000000003030009	1843

Mnemonic	Address	Page
TCM.FIR_MASK	0x0000000003040002	1845
TCM.GP0	0x0000000003000000	1457
TCM.GP1	0x0000000003000001	1458
TCM.GP2	0x0000000003000002	1459
TCM.GP4	0x0000000003000003	1459
TCM.GPIO_ATOMIC_LOCK_REG	0x00000000030003FF	1461
TCM.GPIO_PROTECT_MODE_REG	0x00000000030003FE	1461
TCM.LOCAL_FIR	0x000000000304000A	1847
TCM.OPCG_REG0	0x0000000003030002	1839
TCM.OPCG_REG1	0x0000000003030003	1840
TCM.OPCG_REG2	0x0000000003030004	1840
TCM.OPCG_REG3	0x0000000003030005	1841
TCM.PHASE_SHADOW	0x0000000003030001	1839
TCM.RFIR	0x0000000003040001	1845
TCM.SCANSELQ	0x0000000003030007	1842
TCM.SYNC_CONFIG	0x0000000003030000	1838
TCM.TRA.MBA01TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000003010880	1681
TCM.TRA.MBA01TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000003010881	1681
TCM.TRA.MBA23TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x00000000030110C0	1838
TCM.TRA.MBA23TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x00000000030110C1	1838
TCM.XFIR	0x0000000003040000	1845
TPTOP.NET.PCBSLMEM.ASSIST_INTERRUPT_REG	0x00000000030F0011	1856
TPTOP.NET.PCBSLMEM.ATOMIC_LOCK_REG	0x00000000030F03FF	1863
TPTOP.NET.PCBSLMEM.ATTN_INTERRUPT_REG	0x00000000030F001A	1859
TPTOP.NET.PCBSLMEM.CLK_ADJ_REG	0x00000000030F0015	1857
TPTOP.NET.PCBSLMEM.CLK_ADJ_SET	0x00000000030F0016	1858
TPTOP.NET.PCBSLMEM.ERROR_REG	0x00000000030F001F	1860
TPTOP.NET.PCBSLMEM.GP3_REG	0x00000000030F0012	1857
TPTOP.NET.PCBSLMEM.HANG_PULSE_0_REG	0x00000000030F0020	1861
TPTOP.NET.PCBSLMEM.HANG_PULSE_1_REG	0x00000000030F0021	1861
TPTOP.NET.PCBSLMEM.HANG_PULSE_2_REG	0x00000000030F0022	1861
TPTOP.NET.PCBSLMEM.HANG_PULSE_3_REG	0x00000000030F0023	1862
TPTOP.NET.PCBSLMEM.HANG_PULSE_4_REG	0x00000000030F0024	1862
TPTOP.NET.PCBSLMEM.HANG_PULSE_5_REG	0x00000000030F0025	1862
TPTOP.NET.PCBSLMEM.HANG_PULSE_6_REG	0x00000000030F0026	1862
TPTOP.NET.PCBSLMEM.HEARTBEAT_REG	0x00000000030F0018	1858
TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_1	0x00000000030F0001	1855
TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_2	0x00000000030F0002	1855
TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_3	0x00000000030F0003	1856
TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_4	0x00000000030F0004	1856
TPTOP.NET.PCBSLMEM.PLL_LOCK_REG	0x00000000030F0019	1858
TPTOP.NET.PCBSLMEM.PRE_COUNTER_REG	0x00000000030F0028	1863
TPTOP.NET.PCBSLMEM.PRIMARY_ADDRESS_REG	0x00000000030F0000	1855
TPTOP.NET.PCBSLMEM.PROTECT_MODE_REG	0x00000000030F03FE	1863
TPTOP.NET.PCBSLMEM.RECOV_INTERRUPT_REG	0x00000000030F001B	1859
TPTOP.NET.PCBSLMEM.SLAVE_CONFIG_REG	0x00000000030F001E	1859
TPTOP.NET.PCBSLMEM.TIMEOUT_REG	0x00000000030F0010	1856
TPTOP.NET.PCBSLMEM.VITAL_SCAN_OUT	0x00000000030F0017	1858
TPTOP.NET.PCBSLMEM.XSTOP_INTERRUPT_REG	0x00000000030F001C	1859

The memory buffer registers are listed in the following tables.

Register Name	*GP Register 0*
Mnemonic	TCM.GP0
Address	0000000003000000 (PCB) 0000000003000004 (PCB1) 0000000003000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	TC_UNIT_ABSTCLK_MUXSEL_DC: Select ABIST clock source for Arrays on Chiplet Boundary. When set to 1, clocks where used from Chiplet with ABIST, Reset(0b0)
1	RWX	WOX_AND	WOX_OR	TC_UNIT_SYNCCLK_MUXSEL_DC: Select the sync clock for async latches (init value 1), Reset(0b1)
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC_OUT: Prevent plats from going into flush mode (init value 1), Reset(0b1)
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (init value 1, drop before dropping flushmode_inh), Reset(0b1)
4	RWX	WOX_AND	WOX_OR	TC_GPIO_AVP_MODE_DC_OUT: Enable AVP mode, Reset(0b0)
5	RWX	WOX_AND	WOX_OR	TC_ASIC_CORE_FORCETOKNOWN_DC: LBIST: Force known value on analog outputs; DDRN, Reset(0b0)
6	RWX	WOX_AND	WOX_OR	TC_GPIO_CC_SCAN_DIS_DC_B_OUT: Disable scan - set output of scan chain to zero, Reset(0b0)
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable Skitter measuring during Bist, Reset(0b0)
8	RWX	WOX_AND	WOX_OR	TC_GPIO_LBIST_EN_DC_OUT: LBIST mode, Reset(0b0)
9	RWX	WOX_AND	WOX_OR	TC_UNIT_LBIST_AC_MODE_DC: LBIST AC mode, Reset(0b0)
10	RWX	WOX_AND	WOX_OR	TC_UNIT_LBIST_ARY_WRT_THRU_DC: Array write thru mode - set Array in bypass mode, Reset(0b0)
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST, Reset(0b0)
12	RWX	WOX_AND	WOX_OR	TC_GPIO_ABIST_START_TEST_DC_OUT: Set to start ABIST testing, Reset(0b0)
13	RWX	WOX_AND	WOX_OR	NOT_USED0: not used, Reset(0b0)
14	RWX	WOX_AND	WOX_OR	TC_UNIT_ATPG_EN_DC: ATPG mode, Reset(0b0)
15	RWX	WOX_AND	WOX_OR	TC_GPIO_SCAN_PROTECT_DC_OUT: Scan protection enable (init value 1), Reset(0b1)
16	RWX	WOX_AND	WOX_OR	TC_ASIC_CORE_FORCETOKNOWN2_DC: LBIST: Force known value on analog outputs; DDRS, Reset(0b1)
17	RWX	WOX_AND	WOX_OR	NOT_USED2: not used, Reset(0b0)
18	RWX	WOX_AND	WOX_OR	NOT_USED3: not used, Reset(0b0)
19	RWX	WOX_AND	WOX_OR	NOT_USED4: not used, Reset(0b1)
20	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_START: Start trace to debug macros, Reset(0b0)
21	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_STOP: Stop trace to debug macros, Reset(0b0)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	TP_GPIO_TRACE_RESET: Reset trace to debug macros, Reset(0b0)
23	RWX	WOX_AND	WOX_OR	NOT_USED5: not used, Reset(0b0)
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio, Reset(0b0)
26	RWX	WOX_AND	WOX_OR	NOT_USED6: not used, Reset(0b0)
27	RWX	WOX_AND	WOX_OR	NOT_USED7: not used, Reset(0b0)
28:31	RWX	WOX_AND	WOX_OR	NOT_USED8: not used, Reset(0b0)
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7), Reset(0b0)
40:42	RWX	WOX_AND	WOX_OR	NOT_USED10: not used, Reset(0b0)
43:45	RWX	WOX_AND	WOX_OR	NOT_USED11: not used, Reset(0b0)
46	RWX	WOX_AND	WOX_OR	TC_PLLMEMIO_PADTEST_T_K: Wrap Sel for BSC, Reset(0b0)
47	RWX	WOX_AND	WOX_OR	TC_PLLMEMIO_PADTEST_C_K: Int Mode for BSC, Reset(0b0)
48	RWX	WOX_AND	WOX_OR	NOT_USED12: not used, Reset(0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED13: not used, Reset(0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED14: not used, Reset(0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED15: not used, Reset(0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED16: not used, Reset(0b0)
53	RWX	WOX_AND	WOX_OR	NOT_USED17: not used, Reset(0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED18: not used, Reset(0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED19: not used, Reset(0b0)
56	RWX	WOX_AND	WOX_OR	NOT_USED20: not used, Reset(0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED21: not used, Reset(0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED22: not used, Reset(0b0)
59	RWX	WOX_AND	WOX_OR	NOT_USED23: not used, Reset(0b0)
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: mask for pcb error (access or parity) in CC, Reset(0b0)
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: mask for pcb write while OPCG_IP / scan collision in CC, Reset(0b0)
62	RWX	WOX_AND	WOX_OR	TC_CC_LCC_EDGE_DELAYED_DC: Offset the clocking in the f domain by one cycle, Reset(0b1)
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (init value 1), Reset(0b1)

Register Name	*GP Register 1*
Mnemonic	TCM.GP1
Address	0000000003000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	MEMN_ABIST_DONE: memn_abist_done, Reset(0)
1	ROX	MEMS_ABIST_DONE: mems_abist_done, Reset(0)
2	ROX	TRA_ABIST_DONE: tra_abist_done, Reset(0)

Bits	PCB	Field Mnemonic: Description
3	ROX	NOT_USED1: not used, Reset(0)
4	ROX	NOT_USED9: Diagnostic out port, Reset(0)
5	ROX	NOT_USED25: not used, Reset(0)
6	ROX	NOT_USED26: not used, Reset(0)
7	ROX	NOT_USED27: not used, Reset(0)
8	ROX	NOT_USED28: not used, Reset(0)
9	ROX	NOT_USED29: not used, Reset(0)
10	ROX	NOT_USED30: not used, Reset(0)
11	ROX	NOT_USED31: not used, Reset(0)
12	ROX	NOT_USED32: not used, Reset(0)
13	ROX	NOT_USED33: not used, Reset(0)
14	ROX	NOT_USED34: not used, Reset(0)
15	ROX	TC_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs, Reset(0)
16	ROX	NOT_USED35: not used, Reset(0)
17	ROX	NOT_USED36: not used, Reset(0)
18	ROX	NOT_USED37: not used, Reset(0)
19	ROX	NOT_USED38: not used, Reset(0)
20	ROX	NOT_USED39: not used, Reset(0)
21	ROX	NOT_USED40: not used, Reset(0)
22	ROX	NOT_USED41: not used, Reset(0)
23	ROX	NOT_USED42: not used, Reset(0)

Register Name	***GP Register 2***
Mnemonic	TCM.GP2
Address	0000000003000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking

Register Name	***GP Register 4***
Mnemonic	TCM.GP4
Address	0000000003000003 (PCB) 0000000003000006 (PCB1) 0000000003000007 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select - Reset(0b000000)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
6:7	RWX	WOX_AND	WOX_OR	NOT_USED43: not used, Reset(0b00)
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select - Reset(0b000000)
14:15	RWX	WOX_AND	WOX_OR	NOT_USED44: not used, Reset(0b00)
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select - Reset(0b000000)
22:23	RWX	WOX_AND	WOX_OR	NOT_USED45: not used, Reset(0b00)
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: tc_probe3_sel_dc(0:5) / tc_ex_amux_sel_dc(0:3), -, Reset(0b000000)
30	RWX	WOX_AND	WOX_OR	NOT_USED46: not used, Reset(0b0)
31	RWX	WOX_AND	WOX_OR	NOT_USED47: not used, Reset(0b0)
32	RWX	WOX_AND	WOX_OR	TC_NBTI0_RING_SEL_DC_00: Reset(0b0)
33	RWX	WOX_AND	WOX_OR	TC_NBTI0_RING_SEL_DC_01: Reset(0b0)
34	RWX	WOX_AND	WOX_OR	TC_NBTI0_RING_SEL_DC_02: Reset(0b1)
35	RWX	WOX_AND	WOX_OR	TC_NBTI0_RING_SEL_DC_03: Reset(0b0)
36	RWX	WOX_AND	WOX_OR	TC_NBTI0_HDR_ENABLE_DC_B: Reset(0b0)
37	RWX	WOX_AND	WOX_OR	TC_NBTI0_ACDC_STRESS_SELECT_DC: Reset(0b0)
38	RWX	WOX_AND	WOX_OR	TC_NBTI0_STRESS_DC: Reset(0b0)
39	RWX	WOX_AND	WOX_OR	NOT_USED48: not used, Reset(0b0)
40	RWX	WOX_AND	WOX_OR	NOT_USED49: not used, Reset(0b1)
41	RWX	WOX_AND	WOX_OR	NOT_USED50: not used, Reset(0b0)
42	RWX	WOX_AND	WOX_OR	NOT_USED51: not used, Reset(0b0)
43	RWX	WOX_AND	WOX_OR	NOT_USED52: not used, Reset(0b0)
44	RWX	WOX_AND	WOX_OR	NOT_USED53: not used, Reset(0b0)
45	RWX	WOX_AND	WOX_OR	NOT_USED54: not used, Reset(0b0)
46	RWX	WOX_AND	WOX_OR	NOT_USED55: not used, Reset(0b1)
47	RWX	WOX_AND	WOX_OR	NOT_USED56: not used, Reset(0b0)
48	RWX	WOX_AND	WOX_OR	NOT_USED57: not used, Reset(0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED58: not used, Reset(0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED59: not used, Reset(0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED60: not used, Reset(0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED61: not used, Reset(0b1)
53	RWX	WOX_AND	WOX_OR	NOT_USED62: not used, Reset(0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED63: not used, Reset(0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED64: not used, Reset(0b0)
56	RWX	WOX_AND	WOX_OR	NOT_USED65: not used, Reset(0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED66: not used, Reset(0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED67: not used, Reset(0b1)
59	RWX	WOX_AND	WOX_OR	NOT_USED68: not used, Reset(0b0)
60	RWX	WOX_AND	WOX_OR	NOT_USED69: not used, Reset(0b0)
61	RWX	WOX_AND	WOX_OR	NOT_USED70: not used, Reset(0b0)
62	RWX	WOX_AND	WOX_OR	NOT_USED71: not used, Reset(0b0)
63	RWX	WOX_AND	WOX_OR	NOT_USED72: not used, Reset(0b0)

Register Name	*CC Protect Mode Register*
Mnemonic	TCM.GPIO_PROTECT_MODE_REG
Address	00000000030003FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_READ_PROTECT_ENABLE: Enable read protection
1	RW	GPIO_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	*Atomic Lock Register*
Mnemonic	TCM.GPIO_ATOMIC_LOCK_REG
Address	00000000030003FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	GPIO_ATOMIC_ID: Atomic ID

Register Name	*PSCOMLE Mode Register*
Mnemonic	TCM.EPS.PSC.PSCOM_MODE_REG
Address	0000000003010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: abort_on_PCB_addr_parity_error
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: abort_on_PCB_wdata_parity_error
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: abort_on_DL_return_P0_error
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: abort_on_DL_return_wdata_parity_error
4	RW	WATCHDOG_ENABLE: watchdog_enable
5:6	RW	SCOM_HANG_LIMIT: 0b11: 256, 0b10:512, 0b01:768, 0b00:1023
7	RW	FORCE_ALL_RINGS: set to logic 1 if all rings should be enable independent of ring address
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: fsm_selfreset_on_statevec_parityerror_enable
9:11	RW	RESERVED_PSCOM_MODE_LT: reserved

Register Name	***PSCOMLE Error Register***
Mnemonic	TCM.EPS.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000003010001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated_PCB_wdata_parity_error
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated_PCB_address_parity_error
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated_DL_return_wdata_parity_error
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated_DL_return_P0_error
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated_UL_rdata_parity_error
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated_UL_P0_error
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated_parity_error_on_interface_machine
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated_parity_error_on_p2s_machine
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated_timeout_while_waiting_for_ULCCH
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated_timeout_while_waiting_for_DLDCH_return
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated_timeout_while_waiting_for_ULDCH
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated_pscom_parallel_write_nvld
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated_pscom_parallel_read_nvld
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated_pscom_parallel_addr_invalid
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated_PCB_command_parity_error
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated_General_timeout
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated_satellite_acknowledge_access_violation
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated_satellite_acknowledge_invalid_register
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped_PCB_wdata_parity_error
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped_PCB_address_parity_error
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped_DL_return_wdata_parity_error
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped_DL_return_P0_error
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped_UL_rdata_parity_error
23	RWX	TRAPPED_UL_P0_ERROR: Trapped_UL_P0_error
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped_parity_error_on_interface_machine
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped_parity_error_on_p2s_machine
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped_timeout_while_waiting_for_ULCCH
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped_timeout_while_waiting_for_DLDCH_return
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped_timeout_while_waiting_for_ULDCH
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped_pscom_parallel_write_nvld
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped_pscom_parallel_read_nvld

Bits	PCB	Field Mnemonic: Description
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped_pscom_parallel_addr_invalid
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped_PCB_command_parity_error
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped_General_timeout
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped_satellite_acknowledge_access_violation
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped_satellite_acknowledge_invalid_register

Register Name	***PSCOMLE Error Mask Register***
Mnemonic	TCM.EPS.PSC.PSCOM_ERROR_MASK
Address	0000000003010002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: mask_PCB_wdata_parity_error
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: mask_PCB_address_parity_error
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: mask_DL_return_wdata_parity_error
3	RW	MASK_DL_RETURN_P0_ERROR: mask_DL_return_P0_error
4	RW	MASK_UL_RDATA_PARITY_ERROR: mask_UL_rdata_parity_error
5	RW	MASK_UL_P0_ERROR: mask_UL_P0_error
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: mask_parity_error_on_interface_machine
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: mask_parity_error_on_p2s_machine
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: mask_timeout_while_waiting_for_ULCCH
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: mask_timeout_while_waiting_for_DLDCH_return
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: mask_timeout_while_waiting_for_ULDCH
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: mask_pscom_parallel_write_nvld
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: mask_pscom_parallel_read_nvld
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: mask_pscom_parallel_addr_invalid
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: mask_PCB_command_parity_error
15	RW	MASK_GENERAL_TIMEOUT: mask_general_timeout
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: mask_satellite_acknowledge_access_violation
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: mask_satellite_acknowledge_invalid_register

Register Name	***PSCOMLE Address Trap Register***
Mnemonic	TCM.EPS.PSC.ADDR_TRAP_REG
Address	0000000003010003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB_address_of_last_transaction_with_error
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB_read_notwrite_of_last_transaction_with_error
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: reserved_0
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2Parallel_state_machine_at_time_of_error
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit: set to 1 if no parity error detected of Sat. No and Ack-bits
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: set if write parity error detected by satellite
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: set if invalid read or write access detected by satellite
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: set if invalid register address detected by satellite

Register Name	***Debug Status Register***
Mnemonic	TCM.EPS.PSC.DEBUG_STATUS_REG
Address	0000000003010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: local trace run
1:2	RWX	TRACE_STATE_LAT: trace state latch
3	RWX	TRACE_FREEZE: trace freeze
4:5	RWX	COND3_STATE_LT: condition 3 state latch
6:7	RWX	COND5_STATE_LT: condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: condition event history for condtition0_lt
9	RWX	HISTORY_CONDITION1_LT: condition event history for condtition1_lt
10	RWX	HISTORY_COND2_3_EVENT: condition event history for cond2_3_event
11	RWX	HISTORY_COND2_TIMEOUT: condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: reserved, set to zero

Register Name	***PSCOMLE Modewrite Protect Enable Register***
Mnemonic	TCM.EPS.PSC.PSCOM_WRITE_PROTECT_REG
Address	0000000003010005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_SERIAL_RING_WRITE_PROTECT: enable_serial_ring_write_protect

Bits	PCB	Field Mnemonic: Description
1	RW	RESERVED_WRITE_PROTECT: enable_serial_ring_write_protect

Register Name	*Atomic Lock Register*
Mnemonic	TCM.EPS.PSC.ATOMIC_LOCK_REG
Address	00000000030103FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	*MBA CAL FIR Register (MBACALFIR)*
Mnemonic	MBU.MBA01.MBA_SRQ.MBACALFIRQ
Address	0000000003010400 (SCOM) 0000000003010401 (SCOM1) 0000000003010402 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_RECOVERABLE_ERROR: When set, a MBA recoverable error has occurred. These include cal[0:3]_cfg, rrq, wrq and power control parity errors
1	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_NONRECOVERABLE_ERROR: When set, a MBA nonrecoverable error has occurred. These include dsm, tmr, farb and SIR parity errors
2	RWX	WOX_AND	WOX_OR	MBACALFIRQ_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WAT__ERROR: When set, an error has been detected in the MBA debug WAT logic
4	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR_0: When set, a RCD parity error has been detected on DDR port 0
5	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR0_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr0
6	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR1_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr1
7	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR_1: When set, a RCD parity error has been detected on DDR port 1
8	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBX_TO_MBA_PAR_ERROR: When set, indicates a rdcmd_par, rdcmd_par_rc, rdcmd_par rd1, rdcmd_par_rc rd1, wrcmd_par, wrcmd_par_rc or a wrd_idx_par error has been detected.
9	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_WRD_UE: When set, indicates that a mba_wrd ue has been detected

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_WRD_CE: When set, indicates that a mba_wrd ce has been detected
11	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_MAINT_UE: When set, indicates that a mba_maint ue has been detected
12	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_MAINT_CE: When set, indicates that a mba_maint ce has been detected
13	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR phy(s) did not clear a pending calibration update request.
14	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_DATA_CE: When set, indicates that a ce detected on the wrq data buffer data.
15	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_DATA_UE: When set, indicates that a ue detected on the wrq data buffer data.
16	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_DATA_SUE: When set, indicates that a sue detected on the wrq data buffer data.
17	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
18	RWX	WOX_AND	WOX_OR	MBACALFIRQ_SM_1HOT_ERR: When set, indicates a state machine one hot error.
19	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRD_SCOM_ERROR: When set indicates the WRD_MAC scom satellite detected an internal error.
20	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred
21	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
22:63	RO	N/A	N/A	constant=0b0000000000000000000000000000000000000000000000

Register Name	***MBA CAL FIR Mask Register (MBACALFIR_MASK)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBACALFIR_MASK
Address	0000000003010403 (SCOM) 0000000003010404 (SCOM1) 0000000003010405 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_RECOVERABLE_ERROR: When set, a MBA recoverable error has occurred. These include cal[0:3]_cfg, rrq, wrq and power control parity errors
1	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_NONRECOVERABLE_ERROR: When set, a MBA nonrecoverable error has occurred. These include dsm, tmr, farb and SIR parity errors
2	RW	WO_AND	WO_OR	MBACALFIR_MASK_REFRESH_OVERRUN: When set, a refresh request was detected to a rank that is in high-priority refresh state, indicating that the high-priority refresh was not serviced before another refresh request is received.
3	RW	WO_AND	WO_OR	MBACALFIR_MASK_WAT__ERROR: When set, an error has been detected in the MBA debug WAT logic
4	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR_0: When set, a RCD parity error has been detected on DDR port 0

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR0_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr0
6	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR1_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr1
7	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR_1: When set, a RCD parity error has been detected on DDR port 1
8	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBX_TO_MBA_PAR_ERROR: When set, indicates a rdcmd_par, rdcmd_par_rc, rdcmd_par rd1, rdcmd_par_rc rd1, wrcmd_par, wrcmd_par_rc or a wrd_idx_par error has been detected.
9	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_WRD_UE: When set, indicates that a mba_wrd ue has been detected
10	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_WRD_CE: When set, indicates that a mba_wrd ce has been detected
11	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_MAINT_UE: When set, indicates that a mba_maint ue has been detected
12	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_MAINT_CE: When set, indicates that a mba_maint ce has been detected
13	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR phy(s) did not clear a pending calibration update request.
14	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_DATA_CE: When set, indicates that a ce detected on the wrq data buffer data.
15	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_DATA_UE: When set, indicates that a ue detected on the wrq data buffer data.
16	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_DATA_SUE: When set, indicates that a sue detected on the wrq data buffer data.
17	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
18	RW	WO_AND	WO_OR	MBACALFIR_MASK_SM_1HOT_ERR: When set, indicates a state machine one hot error.
19	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRD_SCOM_ERROR: When set indicates the WRD_MAC scom satellite detected an internal error.
20	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred
21	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
22:63	RO	N/A	N/A	constant=0b0000000000000000000000000000000000000000000000000

Register Name	***MBA CAL FIR Action 0 Register (MBACALFIR_ACTION0)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBACALFIR_ACTION0
Address	0000000003010406 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:21	RW	MBACALFIR_ACTION0_FIR_ACTION0: MBA action0 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
22:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	***MBA CAL FIR Action 1 Register (MBACALFIR_ACTION1)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBACALFIR_ACTION1
Address	0000000003010407 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:21	RW	MBACALFIR_ACTION1_FIR_ACTION1: MBA action1 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
22:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	***Data State Machine Configurations***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_DSM0Q
Address	000000000301040A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_DSM0Q_CFG_RODT_START_DLY: Delay from read command to ODT turn on
6:11	RW	MBA_DSM0Q_CFG_RODT_END_DLY: Delay from read command to ODT turn off
12:17	RW	MBA_DSM0Q_CFG_WODT_START_DLY: Delay from write command to ODT turn on
18:23	RW	MBA_DSM0Q_CFG_WODT_END_DLY: Delay from write command to ODT turn off
24:29	RW	MBA_DSM0Q_CFG_WRDONE_DLY: Delay from write command to write done to MBS
30:35	RW	MBA_DSM0Q_CFG_WRDATA_DLY: Delay from write command to stating the write data flow
36:41	RW	MBA_DSM0Q_CFG_RDTAG_DLY: Delay from read command to rd data valid back to MBS
42	RW	MBA_DSM0Q_CFG_RDTAG_MBX_CYCLE: Determines the mem clock 1/2 cycle that the rdtag entry is released from the dsm queue. 0 = release when mbx clock is low 1= release when mbx clock is high
43:48	RW	MBA_DSM0Q_CFG_RODT_BC4_END_DLY: Delay from read command to ODT turn off for BC4 command
49:54	RW	MBA_DSM0Q_CFG_WODT_BC4_END_DLY: Delay from write command to ODT turn off for BC4 command
55	RW	MBA_DSM0Q_CFG_SYNC_RDTAG_ENABLE: Enable synchronous rdtag interface between MBA and MBS
56:57	RW	MBA_DSM0Q_CFG_GOLDEN_DELAY_MODE: Programmable delay to apply to synchronization pulse between MBS and MBA for synchronous rdtag mode
58:63	RW	MBA_DSM0Q_RESERVED_58_63: Reserved

Register Name	*DDR Data Bus Timing Parameters*
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_TMR0Q
Address	000000000301040B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR0Q_RRSMSR_DLY: Read to Read same mastersame rank
4:7	RW	MBA_TMR0Q_RRSMDR_DLY: Read to Read same masterdifferent rank
8:11	RW	MBA_TMR0Q_RRDM_DLY: Read to Read to different master
12:15	RW	MBA_TMR0Q_RWSMSR_DLY: Read to Write same mastersame rank
16:19	RW	MBA_TMR0Q_RWSMDR_DLY: Read to Write same masterdifferent rank
20:23	RW	MBA_TMR0Q_RWDM_DLY: Read to Write different master
24:29	RW	MBA_TMR0Q_WRSMSR_DLY: Write to read same mastersame rank
30:35	RW	MBA_TMR0Q_WRSMDR_DLY: Write to read same masterdifferent rank
36:39	RW	MBA_TMR0Q_WRDM_DLY: Write to Read different master
40:43	RW	MBA_TMR0Q_WWSMSR_DLY: Write to Write same mastersame rank
44:47	RW	MBA_TMR0Q_WWSMDR_DLY: Write to Write same masterdifferent rank
48:51	RW	MBA_TMR0Q_WWDM_DLY: Write to Write different master
52:55	RW	MBA_TMR0Q_RROP_DLY: Read open page to read delay
56:59	RW	MBA_TMR0Q_WWOP_DLY: Write open page to write delay
60:63	RW	MBA_TMR0Q_TRRD: Activate to activate delay

Register Name	*DDR Bank Busy Parameters*
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_TMR1Q
Address	000000000301040C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RW	MBA_TMR1Q_CFG_TRAP: Read with auto precharge total time(max)
7:13	RW	MBA_TMR1Q_CFG_TWAP: Write with auto precharge total time
14:19	RW	MBA_TMR1Q_CFG_TFAW: Four activate window time
20:23	RW	MBA_TMR1Q_RRSBG_DLY: (DDR4) Ras to Ras same bank group(Trrd_l)
24:28	RW	MBA_TMR1Q_WRSBG_DLY: (DDR4) write to read same bank group(twtr_l)
29	RW	MBA_TMR1Q_CFG_DDR4_CL_INTL_DIS: Disable bank group interleaving for DDR4.
30:63	RW	MBA_TMR1Q_RESERVED_30_63: Reserved

Register Name	***DDR Write Command Parameters***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_WRQ0Q
Address	000000000301040D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBA_WRQ0Q_CFG_WRITE_HW_MARK: Write highwater mark(force writes HPenables writes)
5	RW	MBA_WRQ0Q_CFG_WRQ_FIFO_MODE: Prevent reordering in the WRQ(only entry0 can be selected) HP Cleaner writes will not get selected till they are in entry 0.
6	RW	MBA_WRQ0Q_CFG_DISABLE_WR_PG_MODE: Disable page commands for WRQ
7:18	RW	MBA_WRQ0Q_CFG_WRQ_ENTRY0_HP_DLY: Time for entry0 of the WRQ before it forces HP setting this dial to a 0, will disable entry0 HP
19	RW	MBA_WRQ0Q_CFG_WRQ_FLUSH_WR_RANK: When one write is issued to a rank, try to force more writes to that rank to avoid multiple write to read same rank penalties.
20	RW	MBA_WRQ0Q_CFG_WRQ_ENABLE_NON_HP_WR: Allow writes when they do not meet a condition like entry0_flush, or rd_idle_allow_wr, etc
21:32	RW	MBA_WRQ0Q_CFG_ENTRY0_MIN_FOR_RRQ_IDLE_WR: This is an added condition to allowing writes when the RRQ is idle. This addition allows for multiple writes to stack up in the WRQ before starting the write burst.
33:37	RW	MBA_WRQ0Q_CFG_RRQ_IDLE_LOW_WATERMARK: RRQ idle will also allow writes if the above condition is met of the wrq meets the cfg_rrq_idle_low_watermark condition. For example if this dial is set to 8, and there are more then 8 entries in the wrq then the condition will allow writes when the rrq_idle period is met.
38:43	RW	MBA_WRQ0Q_CFG_WRQ_SKIP_LIMIT: The number of times entry0 of the WRQ can be skipped before entry0 prevents older writes from being issued until entry0 is sent.
44	RW	MBA_WRQ0Q_CFG_WRQ_CLN_HP_ENABLE: Set to 1 to enable cleaner_hp_flush event. When the cleaner is backed up, it will tell the MBA wrq to flush writes to a specific rank. Set to 0, this input into MBA is ignored.
45:52	RW	MBA_WRQ0Q_CFG_WRQ_HANG_THRESHOLD: Hang detection for entry0 of WRQ. Incrememnts every mcbist_srq_hang_pulse(2048 phase hold cycles), and will set a fir when the count=threshold and another pulse is received. Since this checks for count=threshold, a value of 0 is not valid.
53:60	RW	MBA_WRQ0Q_CFG_RRQ_HANG_THRESHOLD: Hang detection for entry0 of RRQ. Incrememnts every mcbist_srq_hang_pulse(2048 phase hold cycles), and will set a fir when the count=threshold and another pulse is received. Since this checks for count=threshold, a value of 0 is not valid.
61:63	RW	MBA_WRQ0Q_RESERVED_61_63: Reserved

Register Name	***DDR Read Command Parameters***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_RRQ0Q
Address	000000000301040E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_RRQ0Q_CFG_RRQ_SKIP_LIMIT: Number of times the bottom entry in the RRQ can be skipped before preventing the entry from being skipped
6:10	RW	MBA_RRQ0Q_CFG_RRQ_REORDER_DEPTH: RRQ reordering depth, 0x10 use all 16 entries 0x0F use bottom 15 entries ... 0x00 use bottom entry(fifo mode)
11	RW	MBA_RRQ0Q_CFG_DISABLE_RD_PG_MODE: Disable page commands for RRQ

Bits	SCOM	Field Mnemonic: Description
12	RW	MBA_RRQ0Q_CFG_DISABLE_FAST_PATH: Disable MBA RRQ fastpath
13:23	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR0: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=000
24:34	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR1: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=001
35:45	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR2: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=011
46:56	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR3: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=111
57:63	RW	MBA_RRQ0Q_RESERVED_57_63: Reserved

Register Name	***DDR Calibration Registers***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_CAL0Q
Address	000000000301040F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL0Q_CFG_CAL_INTERVAL_TMR0_ENABLE: Enable interval tmr0
1:2	RW	MBA_CAL0Q_CFG_TIME_BASE_TMR0: Time base for interval tmr0 counter Values: 1_CYCLE=>0b00 256_CYCLES=>0b01 16384_CYCLE=>0b10 16777216_CYCLES=>0b11
3:11	RW	MBA_CAL0Q_CFG_INTERVAL_COUNTER_TMR0: Interval timer based on time_base(time_base*interval_counter)
12	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops, should always be 1 if the timer is enabled
13:16	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
17	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1
18	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops
19:22	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
23	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2
24	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops
25:28	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_TYPE: 01xx External ZQ calibration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
29	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3
30:38	RW	MBA_CAL0Q_CFG_CAL_TMR0_Z_SYNC: The timer value will be set to this value during z sync.

Bits	SCOM	Field Mnemonic: Description
39:46	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR: Wait time for DDR soft reset upon calibration timeout fail.
47:48	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR_TB: Timebase interval for ddr_reset_tmr Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
49	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_ENABLE: Enable DDR soft reset upon calibration timeout fail. 0 Do not issue soft DDR reset upon calibration timeout. 1 Issue DDR soft reset upon calibration timeout.
50	RW	MBA_CAL0Q_CFG_CAL_TMR0_SINGLE_RANK: Enable single-rank mode for timer0 calibrations. Calibrations programmed in tmr0 will run on 1 rank at a time per timer expiration. 0 Issue calibrations for all enabled ranks per timer expiration. 1 Issue calibrations for 1 rank at a time per timer expiration.
51	RW	MBA_CAL0Q_INJECT_CAL0_PAR_ERROR: Setting to 1 will inject one parity error, must be set to 0 and then 1 again to inject another error 0 No error inject 1 Inject one parity error
52	RW	MBA_CAL0Q_INJECT_1HOT_SM_ERROR: Setting to 1 will inject one 1hot sm error, must be set to 0 and then 1 again to inject another error 0 No error inject 1 Inject one 1hot sm error
53:55	RW	MBA_CAL0Q_CFG_CAL_SINGLE_PORT_MODE: Single port mode config, default is both ports are calibrated at the same time, options are single port calibrated at a time with both ports powered up single port calibrated at a time with one port powered up single port calibrated at a time with one port powered up and only the rank requested by the DDR PHY powered up, only to be used in single rank mode Values: DEFAULT=>0b000 SINGLE_PORT_CAL_BOTH_PORT_PUP=>0b100 SINGLE_PORT_CAL_ONE_PORT_PUP=>0b110 SINGLE_PORT_CAL_ONE_PORT_ONE_RANK_PUP=>0b111
56:63	RW	MBA_CAL0Q_RESERVED_56_63: Reserved

Register Name	***DDR Calibration Registers***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_CAL1Q
Address	0000000003010410 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL1Q_CFG_CAL_INTERVAL_TMR1_ENABLE: Enable interval tmr1
1:2	RW	MBA_CAL1Q_CFG_TIME_BASE_TMR1: Time base for interval tmr1 counter Values: 1_CYCLE=>0b00 256_CYCLES=>0b01 16384_CYCLE=>0b10 16777216_CYCLES=>0b11
3:11	RW	MBA_CAL1Q_CFG_INTERVAL_COUNTER_TMR1: Interval timer based on time_base(time_base*interval_counter)
12	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops, should always be 1 if the timer is enabled
13:16	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
17	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1

Bits	SCOM	Field Mnemonic: Description
18	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops
19:22	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
23	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2
24	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops
25:28	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_TYPE: 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
29	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3
30:38	RW	MBA_CAL1Q_CFG_CAL_TMR1_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL1Q_CFG_CAL_TMR1_SINGLE_RANK: Enable single-rank mode for timer1 calibrations. Calibrations programmed in tmr1 will run on 1 rank at a time per timer expiration. 0 Issue calibrations for all enabled ranks per timer expiration. 1 Issue calibrations for 1 rank at a time per timer expiration.
40:63	RW	MBA_CAL1Q_RESERVED_40_63: Reserved

Register Name	***DDR Calibration Registers***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_CAL2Q
Address	0000000003010411 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL2Q_CFG_CAL_INTERVAL_TMR2_ENABLE: Enable interval tmr2
1:2	RW	MBA_CAL2Q_CFG_TIME_BASE_TMR2: Time base for interval tmr2 counter Values: 1_CYCLE=>0b00 256_CYCLES=>0b01 16384_CYCLE=>0b10 16777216_CYCLES=>0b11
3:11	RW	MBA_CAL2Q_CFG_INTERVAL_COUNTER_TMR2: Interval timer based on time_base(time_base*interval_counter)
12	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops, should always be 1 if the timer is enabled
13:16	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
17	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1
18	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops
19:22	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
23	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2

Bits	SCOM	Field Mnemonic: Description
24	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops
25:28	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_TYPE: 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
29	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3
30:38	RW	MBA_CAL2Q_CFG_CAL_TMR2_Z_SYNC: The timer value will be set to this value during z sync
39	RW	MBA_CAL2Q_CFG_CAL_TMR2_SINGLE_RANK: Enable single-rank mode for timer2 calibrations. Calibrations programmed in tmr2 will run on 1 rank at a time per timer expiration. 0 Issue calibrations for all enabled ranks per timer expiration. 1 Issue calibrations for 1 rank at a time per timer expiration.
40:63	RW	MBA_CAL2Q_RESERVED_40_63: Reserved

Register Name	***DDR Calibration Length Registers***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_CAL3Q
Address	0000000003010412 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_TB: Internal ZQ time base Time base for internal ZQ cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
2:9	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_LENGTH: Number of internal ZQ time bases required to meet max internal zq length
10:11	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_TB: External ZQ time base Time base for external ZQ cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
12:19	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_LENGTH: Number of external ZQ time bases required to meet max external zq length
20:21	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_TB: ReadclkSysclk time base Time base for readclksysclk cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
22:29	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_LENGTH: Number of Readclksysclk time bases required to meet max rdclk length
30:31	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_TB: Dqs alignment time base Time base for DQS alignment cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11

Bits	SCOM	Field Mnemonic: Description
32:39	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_LENGTH: Number of Dqs alignment time bases required to meet max dqs alignment length
40:41	RW	MBA_CAL3Q_CFG_MPR_READEYE_TB: Readeye time base Time base for readeye cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
42:49	RW	MBA_CAL3Q_CFG_MPR_READEYE_LENGTH: Number of readeye time bases required to meet max external zq length
50:51	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_TB: All Periodics time base Time base for all periodic cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
52:59	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_LENGTH: Number of all_periodic time bases required to meet max calibration length for all periodic calibration (in parallel)
60:63	RW	MBA_CAL3Q_RESERVED_60_63: Reserved

Register Name	***Final Arb Parameters***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_FARB0Q
Address	0000000003010413 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:10	RW	MBA_FARB0Q_CFG_MAX_CAS_PER_INTERVAL: Reserved.
11:23	RW	MBA_FARB0Q_CFG_M_OVER_N_INTERVAL: Reserved.
24:30	RW	MBA_FARB0Q_CFG_MAX_READS_IN_A_ROW: Limits the max number of reads in a row, before forcing a write. There must be a write in the WRQ for the counting to start. 0x00 Disabled 0x01 1 read before allowing a write 0x7F 127 reads before forcing a write
31:37	RW	MBA_FARB0Q_CFG_MAX_WRITES_IN_A_ROW: Limits the max number of writes in a row, before forcing a read. There must be a read in the RRQ for the counting to start. 0x00 Disabled 0x01 1 write before allowing a read 0x7F 127 write before forcing a read
38	RW	MBA_FARB0Q_CFG_PARITY_AFTER_CMD: Determines when parity will be driven 0b0 parity driven same cycle as the command 0b1parity driven the cycle after the command (also turns on OE for the parity cycle)
39	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_RAS0: Inject a parity error on next RAS on port 0 according to inject type selected in bit 59
40	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CAS0: Inject a parity error on next CAS on port 0 according to inject type selected in bit 59
41	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_RAS1: Inject a parity error on next RAS on port 1 according to inject type selected in bit 59
42	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CAS1: Inject a parity error on next CAS on port 1 according to inject type selected in bit 59
43:47	RW	MBA_FARB0Q_CFG_PARITY_DETECT_TIME: Measures the time from an injected error till when the error is detected back at the MBA
48:53	RW	MBA_FARB0Q_CFG_RCD_PROTECTION_TIME: Time interval in which commands were sent out before a rcd parity error occurrence that should be re-issued. Should be set >= to cfg_parity_detect_time

Bits	SCOM	Field Mnemonic: Description
54	RW	MBA_FARB0Q_CFG_DISABLE_RCD_RECOVERY: Disable the rcd recovery procedure.
55	RW	MBA_FARB0Q_CFG_OE_ALWAYS_ON: Force DDR OE to always be on(never tristate the ddr addr drivers)
56	RW	MBA_FARB0Q_CFG_FLIP_PORT1_ADDR: Set to 1 to enable port 1 Address bit flipping. Address bits that will be flipped: bank(0:2), Addr(3:9, 11, 13-15)
57	RW	MBA_FARB0Q_CFG_DISABLE_REFRESH_DURING_NOISE_WDW: Default 0, allows refreshes during a noise window. Set to 1, to disable refreshes during a noise window.
58	RW	MBA_FARB0Q_CFG_NM_PER_SLOT_ENABLED: Reserved.
59	RW	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CONSTANT: If set, parity errors are injected continuously; otherwise, parity errors are injected only once
60	RW	MBA_FARB0Q_CFG_IGNORE_RCD_PARITY_ERR: If set, rcd parity errors are not logged and recovery is not started. When this is set, cfg_disable_rcd_recovery becomes irrelevant because recovery is never started.
61:63	RW	MBA_FARB0Q_RESERVED_61_63: Reserved

Register Name	***Final Arb Parameters***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_FARB1Q
Address	0000000003010414 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_FARB1Q_CFG_M0S0_CS: Chip selects for M0S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
6:11	RW	MBA_FARB1Q_CFG_M0S1_CS: Chip selects for M0S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
12:17	RW	MBA_FARB1Q_CFG_M0S2_CS: Chip selects for M0S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
18:23	RW	MBA_FARB1Q_CFG_M0S3_CS: Chip selects for M0S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
24:29	RW	MBA_FARB1Q_CFG_M0S4_CS: Chip selects for M0S4 OR M2S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
30:35	RW	MBA_FARB1Q_CFG_M0S5_CS: Chip selects for M0S5 OR M2S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
36:41	RW	MBA_FARB1Q_CFG_M0S6_CS: Chip selects for M0S6 or M2S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
42:47	RW	MBA_FARB1Q_CFG_M0S7_CS: Chip selects for M0S7 or M2S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
48:51	RW	MBA_FARB1Q_CFG_CS_S0_MASK: Mask bits for the chip select. This mask register masks the actual chip select bits while allowing chip_id bits to go out for 2N mode. Set by cs_mapping gdial.
52	RW	MBA_FARB1Q_CFG_S0_DIS_SMDR: Set to 1 if using a 5D config in slot 0, This will using the different master parms instead of the SMDR.
53:63	RW	MBA_FARB1Q_CFG_S0_RSV0: Reserved

Register Name	***Final Arb Parameters***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_FARB2Q
Address	0000000003010415 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_FARB2Q_CFG_M1S0_CS: Chip selects for M1S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
6:11	RW	MBA_FARB2Q_CFG_M1S1_CS: Chip selects for M1S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
12:17	RW	MBA_FARB2Q_CFG_M1S2_CS: Chip selects for M1S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
18:23	RW	MBA_FARB2Q_CFG_M1S3_CS: Chip selects for M1S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
24:29	RW	MBA_FARB2Q_CFG_M1S4_CS: Chip selects for M1S4 or M3S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
30:35	RW	MBA_FARB2Q_CFG_M1S5_CS: Chip selects for M1S5 or M3S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
36:41	RW	MBA_FARB2Q_CFG_M1S6_CS: Chip selects for M1S6 or M3S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
42:47	RW	MBA_FARB2Q_CFG_M1S7_CS: Chip selects for M1S7 or M3S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
48:63	RW	MBA_FARB2Q_CFG_S0_RSV1: Reserved

Register Name	***N/M Throttling Control***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_FARB3Q
Address	0000000003010416 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:14	RW	MBA_FARB3Q_CFG_NM_N_PER_MBA: The N value for the NM throttling across a single MBA. The max command count that can occur over a time interval M.
15:30	RW	MBA_FARB3Q_CFG_NM_N_PER_CHIP: The N value for the NM throttling across both MBAs. The max command count that can occur over a time interval M.
31:44	RW	MBA_FARB3Q_CFG_NM_M: The M value for the NM throttling. This counts DRAM clock cycles.
45:47	RW	MBA_FARB3Q_CFG_NM_RAS_WEIGHT: The increment to be added to the N count each time a RAS is sent.
48:50	RW	MBA_FARB3Q_CFG_NM_CAS_WEIGHT: The increment to be added to the N count each time a CAS is sent.
51	RW	MBA_FARB3Q_CFG_NM_PER_SLOT_ENABLED: Default 0, NM events counted per MBA. Set to 1 to count NM events per slot.
52	RW	MBA_FARB3Q_CFG_NM_COUNT_OTHER_MBA_DIS: Set to 1 to turn Counter 2 into a per-MBA counter, disregarding any incrementing from the other MBA (NOTE: also set this to a '1' if you want to fence the other MBA).
53:63	RW	MBA_FARB3Q_RESERVED_53_63: Reserved

Register Name	***MBA Error Report Register***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_ERR_REPORTQ
Address	000000000301041A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_ERR: Rdcmd parity error from MBX MBACALFIR Bit 8
1	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_RC_ERR: Rdcmd RC parity error from MBX MBACALFIR Bit 8

Bits	SCOM	Field Mnemonic: Description
2	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_RD1_ERR: Rdcmd RD1 parity error from MBX MBACALFIR Bit 8
3	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_RC_RD1_ERR: Rdcmd RC RD1 parity error from MBX MBACALFIR Bit 8
4	ROX	MBA_ERR_REPORTQ_MBA_WRCMD_PAR_ERR: Wrcmd parity error from MBX MBACALFIR Bit 8
5	ROX	MBA_ERR_REPORTQ_MBA_WRCMD_PAR_RC_ERR: Wrcmd RC parity error from MBX MBACALFIR Bit 8
6	ROX	MBA_ERR_REPORTQ_MBA_WRD_IDX_PAR_ERR: WRD index parity error from MBX MBACALFIR Bit 8
7	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_7: reserved
8	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_8: reserved
9	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_9: reserved
10	ROX	MBA_ERR_REPORTQ_WRQ_HANG_ERR: WRQ hang error MBACALFIR Bit 17
11	ROX	MBA_ERR_REPORTQ_RRQ_HANG_ERR: RRQ hang error MBACALFIR Bit 17
12	ROX	MBA_ERR_REPORTQ_DSM_PE_ERR: Parity error in DSM config reg(s) MBACALFIR Bit 1
13	ROX	MBA_ERR_REPORTQ_TMR_PE_ERR: Parity error in TMR config reg(s) MBACALFIR Bit 1
14	ROX	MBA_ERR_REPORTQ_RRQ_PE_ERR: Parity error in RRQ config reg(s) MBACALFIR Bit 1
15	ROX	MBA_ERR_REPORTQ_WRQ_PE_ERR: Parity error in WRQ config reg(s) MBACALFIR Bit 1
16	ROX	MBA_ERR_REPORTQ_FARB_PE_ERR: Parity error in FARB config reg(s) MBACALFIR Bit 1
17	ROX	MBA_ERR_REPORTQ_PC_PE_ERR: Parity error in PC config reg(s) MBACALFIR Bit 1
18	ROX	MBA_ERR_REPORTQ_CAL0_PE_ERR: Parity error in Cal0 config reg MBACALFIR Bit 0
19	ROX	MBA_ERR_REPORTQ_CAL1_PE_ERR: Parity error in Cal1 config reg MBACALFIR Bit 0
20	ROX	MBA_ERR_REPORTQ_CAL2_PE_ERR: Parity error in Cal2 config reg MBACALFIR Bit 0
21	ROX	MBA_ERR_REPORTQ_CAL3_PE_ERR: Parity error in Cal3 config reg MBACALFIR Bit 0
22	ROX	MBA_ERR_REPORTQ_DDR_IF_SM_1HOT_ERR: DDR state machine one hot error MBACALFIR Bit 18
23	ROX	MBA_ERR_REPORTQ_CAL_SM_1HOT_ERR: Calibration state machine one hot error MBACALFIR Bit 18
24	ROX	MBA_ERR_REPORTQ_RANK_SM_1HOT_ERR: Rank state machine one hot error MBACALFIR Bit 18
25	ROX	MBA_ERR_REPORTQ_PC_CAL_REFFSM_1HOT_ERR: Refresh state machine one hot error MBACALFIR Bit 18
26	ROX	MBA_ERR_REPORTQ_PC_CAL_PCFSM_1HOT_ERR: Power Control state machine one hot error MBACALFIR Bit 18
27	ROX	MBA_ERR_REPORTQ_FARB_CAL_RECVFSM_1HOT_ERR: Recovery state machine one hot error MBACALFIR Bit 18
28	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_28: reserved
29	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_29: reserved
30	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_30: reserved
31	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_31: reserved
32	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_32: reserved
33	ROX	MBA_ERR_REPORTQ_SIR_CERR: SIR error MBACALFIR Bit 1
34	ROX	MBA_ERR_REPORTQ_RDCMD_RDCHECK_ERR: Read cmd index check error from MBX MBACALFIR Bit 8
35	ROX	MBA_ERR_REPORTQ_WRD_RDCHECK_ERR: Write cmd index check error from MBX MBACALFIR Bit 8
36	ROX	MBA_ERR_REPORTQ_CAL0_INVALID_ACCESS: Cal0 invalid access MBASECUREFIR Bit 0
37	ROX	MBA_ERR_REPORTQ_CAL1_INVALID_ACCESS: Cal1 invalid access MBASECUREFIR Bit 1
38	ROX	MBA_ERR_REPORTQ_CAL2_INVALID_ACCESS: Cal2 invalid access MBASECUREFIR Bit 2

Bits	SCOM	Field Mnemonic: Description
39	ROX	MBA_ERR_REPORTQ_CAL3_INVALID_ACCESS: Cal3 invalid access MBASECUREFIR Bit 3
40	ROX	MBA_ERR_REPORTQ_DDR_INVALID_ACCESS: DDR invalid access MBASECUREFIR Bit 4
41	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_41: reserved
42	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_42: reserved
43:63	RO	constant=0b00000000000000000000

Register Name	***MBA Secure Fault Isolation Register (MCASFIR)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBASIRQ
Address	000000000301041B (SCOM) 000000000301041C (SCOM1) 000000000301041D (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL0Q_ACCESS: If set, a non-inband write access to MBA_CALQ0 was detected with protection_en active
1	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL1Q_ACCESS: If set, a non-inband write access to MBA_CALQ1 was detected with protection_en active
2	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL2Q_ACCESS: If set, a non-inband write access to MBA_CAL2Q was detected with protection_en active
3	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL3Q_ACCESS: If set, a non-inband write access to MBA_CAL3Q was detected with protection_en active
4	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_DDR_CONFIG_REG_ACCESS: If set, a non-inband write access to a DDR configuration register was detected with protection_en active
5	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_SIR_MASK_OR_ACTION_REGISTER_ACCESS: If set, a non-inband write access to the MBSSIR mask or action registers was detected with protection_en active
6:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Secure Fault Isolation Mask Register (MBASIRMASK)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBASIRMASK
Address	000000000301041E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBASIRMASK_SIR_MASK: Masks SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Secure Fault Isolation Action0 Register (MBASIRACT0)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBASIRACT0
Address	0000000003010421 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBASIRACT0_ACTION_0: Action 0 for SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Secure Fault Isolation Action0 Register (MBASIRACT1)***
Mnemonic	MBU.MBA01.MBA_SRQ.MBASIRACT1
Address	0000000003010422 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBASIRACT1_ACTION_1: Action 1 for SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***Refresh Register 0***
Mnemonic	MBU.MBA01.MBA_SRQ.PC.MBAREF0Q
Address	0000000003010432 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREF0Q_CFG_REFRESH_ENABLE: Refresh enable
1:2	RW	MBAREF0Q_CFG_REFRESH_INTERVAL_TIMEBASE_SELECT: NOTE: Settings 10 and 11 are for characterizationstess testing only. Values: USE_DEFAULT_REFRESH_INTERVAL=>0b00 USE_A_1_IN_8K_PULSE_AS_A_REFRESH_INTERVAL_TIMEBASE=>0b10 USE_A_1_IN_2_22_PULSE_AS_A_REFRESH_INTERVAL_TIMEBASE=>0b11
3	RW	MBAREF0Q_RESERVED_3: Reserved
4:7	RW	MBAREF0Q_CFG_REFRESH_PRIORITY_THRESHOLD: Once the number of queued refreshes to a rank reaches this threshold, that rank's refreshes become high priority. Values greater than 0x8 can potentially lead to a refresh interval-DRAM spec violation. A value of 0xf is illegal.
8:18	RW	MBAREF0Q_CFG_REFRESH_INTERVAL: For example, for a system with two master ranks and 4 slaves per master (8 ranks total), a desired refresh interval of 7.8us, and DDR-1600 memory, cfg_refresh_interval=7.881.25.008=97 (round down)
19:29	RW	MBAREF0Q_CFG_REFRESH_RESET_INTERVAL: NOTE: refresh reset interval should be set to a value less than the refresh interval
30:39	RW	MBAREF0Q_CFG_TRFC: Refresh to activate rank protection timer
40:49	RW	MBAREF0Q_CFG_REFR_TSV_STACK: Refresh to Refresh spacing within the same TSV stack timer

Bits	SCOM	Field Mnemonic: Description
50:60	RW	MBAREF0Q_CFG_REFR_CHECK_INTERVAL: For example, if using DDR-1600 memory and expecting a refresh to occur every 7.8us: cfg_refr_check_interval=7.81.25.008=780=0x30C If using DDR-1600 memory and expecting a refresh every 3.9us: cfg_refr_check_interval=3.91.25.008=390=0x186
61:63	RW	MBAREF0Q_RESERVED_61_63: Reserved

Register Name	***Rank-to-primary-CKE Mapping Table***
Mnemonic	MBU.MBA01.MBA_SRQ.PC.MBAREF1Q
Address	0000000003010433 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAREF1Q_CFG_MRNK0_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
4:7	RW	MBAREF1Q_CFG_MRNK1_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
8:11	RW	MBAREF1Q_CFG_MRNK2_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
12:15	RW	MBAREF1Q_CFG_MRNK3_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
16:19	RW	MBAREF1Q_CFG_MRNK4_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011

Bits	SCOM	Field Mnemonic: Description
20:23	RW	MBAREF1Q_CFG_MRNK5_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
24:27	RW	MBAREF1Q_CFG_MRNK6_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
28:31	RW	MBAREF1Q_CFG_MRNK7_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
32:63	RO	constant=0b00000000000000000000000000000000 Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011

Register Name	***Power Control Register 0***
Mnemonic	MBU.MBA01.MBA_SRQ.PC.MBARPC0Q
Address	0000000003010434 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBARPC0Q_CFG_LP2_ENTRY_REQ: Setreset by firmware. When set, MBA powers down all ranks and sets cfg_lp2_state=1. Set by firmware during LP2 entry procedure, after all traffic and refresh has been stopped. Cleared by firmware during LP2 exit procedure.
1	ROX	MBARPC0Q_CFG_LP2_STATE: Read only status bit; set by hardware when cfg_lp2_entry_req is active AND all ranks are powered down; reset by hardware when cfg_lp2_entry_req is reset
2	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS_ENABLE: This is an overall enable for power domain control. If power control is disabled, the CKEs will always be set to a '1'.

Bits	SCOM	Field Mnemonic: Description
3:5	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS: Maxall_minall means power control will not limit the number of domains accessible at a given time. Power domains will not be powered down even if they go idle, unless min_domain_reduction is enabled. Maxall_minx will permit idle power down to reduce the number of domains powered up once a domain has gone idle, but it won't restrict the maximum domains powered up. Max1_minx restricts the number of domains that can be powered up at a given time to 1. Values: MAXALL_MINALL=>0b000 MAXALL_MIN1=>0b001 MAXALL_MIN0=>0b010 MAX1_MIN1=>0b011 MAX1_MIN0=>0b100
6:10	RW	MBARPC0Q_CFG_PUP_AVAIL: Specifies how many DRAM command clocks for power control to wait from CKE going high to activate
11:15	RW	MBARPC0Q_CFG_PDN_PUP: Specifies how many DRAM command clocks for power control to wait from CKE going low to high again (enforces minimum time in power down)
16:20	RW	MBARPC0Q_CFG_PUP_PDN: Specifies how many DRAM command clocks for power control to wait from CKE going high to low again (enforces minimum time powered up)
21	RW	MBARPC0Q_RESERVED_21: Reserved
22	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_ENABLE: This allows a dynamic reduction of the minimum domains to 0 when no memory traffic has been seen over the specified cfg_min_domain_reduction_time; min domains will be restored once traffic is seen; the adjusted min domains won't be reflected in or over-write the cfg_min_max_domains setting (adjustment made internal to logic).
23:32	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_TIME: Specifies how many DRAM command clocks the MBA must be idle before min_cke is reduced to 0.
33	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_ENABLE: Once a configurable time has been met since the last activate, a subsequent domain can be powered up, even if the powering-down domain has not been powered down yet.
34:41	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_TIME: Specifies how many DRAM command clocks the MBA must be idle before minimum domains is reduced to 0.
42	RW	MBARPC0Q_CFG_FORCE_SPARE_PUP: Forces all spare CKEs to couple with their respective primary CKEs. This bit should not be toggled during runtime or when calibration is enabled.
43:63	RW	MBARPC0Q_RESERVED_43_63: Reserved

Register Name	***Rank-to-CKE Power Domain Mapping Table***
Mnemonic	MBU.MBA01.MBA_SRQ.PC.MBARPC1Q
Address	0000000003010435 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBARPC1Q_CFG_MRNK0_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
4:7	RW	MBARPC1Q_CFG_MRNK1_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
8:11	RW	MBARPC1Q_CFG_MRNK2_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
12:15	RW	MBARPC1Q_CFG_MRNK3_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
16:19	RW	MBARPC1Q_CFG_MRNK4_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1

Bits	SCOM	Field Mnemonic: Description
20:23	RW	MBARPC1Q_CFG_MRNK5_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
24:27	RW	MBARPC1Q_CFG_MRNK6_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
28:31	RW	MBARPC1Q_CFG_MRNK7_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
32:35	RW	MBARPC1Q_CFG_MRNK0_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
36:39	RW	MBARPC1Q_CFG_MRNK1_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
40:43	RW	MBARPC1Q_CFG_MRNK2_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
44:47	RW	MBARPC1Q_CFG_MRNK3_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
48:51	RW	MBARPC1Q_CFG_MRNK4_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
52:55	RW	MBARPC1Q_CFG_MRNK5_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
56:59	RW	MBARPC1Q_CFG_MRNK6_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
60:63	RW	MBARPC1Q_CFG_MRNK7_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1

Register Name	***Refresh Avoidance Control Register***
Mnemonic	MBU.MBA01.MBA_SRQ.PC.MBAREFAQ
Address	0000000003010436 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREFAQ_CFG_REFRESH_LP_DYN_WAIT_ENABLE: When enabled, a low priority refresh wait function takes into account the power state of the rank, how long the rank has been idle and the rank's refresh backlog queue count when scheduling a low priority refresh. If disabled, a low priority refresh is scheduled once the read reorder queue has been idle for a programmable number of cycles.
1	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BIAS_ENABLE: When enabled, the refresh logic sends a signal to bias the prefetch and final arbitration logic ahead of issuing a high priority refresh.
2	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BLOCK_ENABLE: When enabled, the refresh logic sends a block signal when issuing a high priority refresh. The block signal prevents new demand requests to the refreshing rank from overwhelming the read reorder queue.
3	RW	MBAREFAQ_RESERVED_3: Reserved
4:7	RW	MBAREFAQ_CFG_REFRESH_PUP_THRESHOLD: If cfg_refresh_lp_dyn_wait_enable=1, then the logic waits until the refresh backlog queue reaches this threshold before powering up to service a low priority refresh. If power control is disabled (rank never powered down), this setting becomes irrelevant as the rank will always be powered up, and the refresh will still be gated until the appropriate idle time has been met. This setting should not be set greater than cfg_priority_threshold (the refresh high priority threshold).

Bits	SCOM	Field Mnemonic: Description
8:10	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ1_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
11:13	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ2_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
14:16	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ3_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
17:19	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ4_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
20:22	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ5_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
23:25	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ6_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111

Bits	SCOM	Field Mnemonic: Description
26:31	RW	MBAREFAQ_CFG_RRQ_REF_HINT_DLY: Programmable timer that determines the delay from the refresh pending backlog = HP threshold to the assertion of a scheduling hint to the read reorder queue to accommodate the impending high priority refresh. (B) NOTE: This delay counts in multiples of 4 DDR clocks (per default hp ref sub counter setting)
32:37	RW	MBAREFAQ_CFG_ASSERT_REFRESH_BLOCK_DLY: Programmable timer that determines the delay from the refresh pending backlog = HP threshold to where subsequent commands from MBS to the refresh rank are blocked. This must be greater than cfg_rrq_ref_hint_dly. (C) NOTE: This delay counts in multiples of 4 DDR clocks (per default hp ref sub counter setting)
38:43	RW	MBAREFAQ_CFG_FORCE_HP_REF_REQ_DLY: Programmable timer that determines the delay from the refresh pending backlog = HP threshold to where the refresh must be serviced by the final command arbiter. This must be greater than cfg_assert_refresh_block_dly. (D) NOTE: This delay counts in multiples of 4 DDR clocks (per default hp ref sub counter setting)
44:49	RW	MBAREFAQ_CFG_REF_BLOCK_STOP_DLY: Programmable setting which is subtracted from the tRFC timer. The result is used to determine when the block signal can be deasserted leading up to the end of a tRFC period. This allows new commands targeting the refresh domain being refreshed to progress to the rrq so that they are ready to go as soon as tRFC ends. (N)
50:63	RW	MBAREFAQ_RESERVED_50_63: Reserved

Register Name	***Performance Monitor Counts0***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU0Q
Address	0000000003010437 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU0Q_READ_COUNT: Read count, increments every read, wraps
32:63	ROX	MBA_PMU0Q_WRITE_COUNT: Write count, increments every write, wraps

Register Name	***Performance Monitor Counts1***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU1Q
Address	0000000003010438 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU1Q_ACTIVATE_COUNT: Bank activate count, increments for every activate , wraps
32:63	ROX	MBA_PMU1Q_PU_COUNTS: Counts the number of rising edges for a CKE, wraps

Register Name	***Performance Monitor Counts2***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU2Q
Address	0000000003010439 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU2Q_FRAME_COUNT: Frame count, increments every dram clock(2:1) clock
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***Performance Monitor Counts4***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU3Q
Address	0000000003010 43A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_PMU3Q_LOW_IDLE_THRESHOLD: Each time the low idle (no reads or writes queued) threshold is met, the low idle count will increment; between periods of command activity, there may be multiple low-idle-threshold-width windows of command inactivity. For each of these windows, the low idle count will be incremented. (counts 2:1Dram addr frequency) counts MBA idle cycles
16:31	RW	MBA_PMU3Q_MED_IDLE_THRESHOLD: Each time the med idle (no reads or writes queued) threshold is met, the med idle count will increment; between periods of command activity, there may be multiple med-idle-threshold-width windows of command inactivity. For each of these windows, the med idle count will be incremented.
32:63	RW	MBA_PMU3Q_HIGH_IDLE_THRESHOLD: Each time the high idle (no reads or writes queued) threshold is met, the high idle count will increment; between periods of command activity, there may be multiple high-idle-threshold-width windows of command inactivity. For each of these windows, the high idle count will be incremented.

Register Name	***Performance Monitor Counts***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU4Q
Address	0000000003010 43B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU4Q_BASE_IDLE_COUNT: Increments every MBA idle cycle (counts 2:1Dram addr frequency)
32:63	ROX	MBA_PMU4Q_LOW_IDLE_COUNT: Counts the number of times the low idle threshold was met (counts 2:1Dram addr frequency)

Register Name	***Performance Monitor Counts***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU5Q
Address	0000000003010 43C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU5Q_MED_IDLE_COUNT: Counts the number of times the med idle threshold was met (counts 2:1Dram addr frequency)
32:63	ROX	MBA_PMU5Q_HIGH_IDLE_COUNT: Counts the number of times the high idle threshold was met (counts 2:1Dram addr frequency)

Register Name	***Performance Monitor Counts***
Mnemonic	MBU.MBA01.MBA_SRQ.MBA_PMU6Q
Address	000000000301043D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:17	RWX_WCLRPART	MBA_PMU6Q_TOTAL_GAP_COUNTS: Increments by 1 for any gap that is greater than or equal to the gap programmed by the gap length field (see bits 36-38 for info)
18:35	RWX_WCLRPART	MBA_PMU6Q_SPECIFIC_GAP_COUNT: Total number of gaps greater than or equal to gap length caused by reason specified in field 39:42.
36:38	RW	MBA_PMU6Q_GAP_LENGTH_ADDER: The gap length is this field +4. So a value of 0 will count gaps that occur every 4 cycles.
39:42	RW	MBA_PMU6Q_SPECIFIC_GAP_CONDITION: This field chooses the condition for the specific gap counter(18:35) refresh_busy => 0b0001; bank_busy => 0b0010; power_down_busy => 0b0011; high_priority_write => 0b0100; entry_0_HP => 0b0101; NM_busy => 0b0110; read_queue_empty => 0b0111; write_queue_empty => 0b1000; read_and_write_queue_empty => 0b1001; bg_busy => 0b1010; data_bus_busy => 0b1011; out_of_timers => 0b1100; Values: TFAW_BUSY=>0b0000 REFRESH_BUSY=>0b0001 BANK_BUSY=>0b0010 POWER_DOWN_BUSY=>0b0011 HIGH_PRIORITY_WRITE=>0b0100 ENTRY_0_HP=>0b0101 NM_BUSY=>0b0110 READ_QUEUE_EMPTY=>0b0111 WRITE_QUEUE_EMPTY=>0b1000 READ_AND_WRITE_QUEUE_EMPTY=>0b1001 BG_BUSY=>0b1010 DATA_BUS_BUSY=>0b1011 OUT_OF_TIMERS=>0b1100
43:60	RWX_WCLRPART	MBA_PMU6Q_CMD_TO_CMD_COUNT: Count the number of times the following command pattern occurs that is specified in bits 61:63.
61:63	RW	MBA_PMU6Q_COMMAND_PATTERN_TO_COUNT: Type of command pattern for counter in bits 43:60 should count. Values: RWSM_READ_TO_WRITE_SAME_MASTER=>0b000 RWDM_READ_TO_WRITE_DIFFERENT_MASTER=>0b001 RWXX_READ_TO_WRITE=>0b010 WRSM_WRITE_TO_READ_SAME_MASTER=>0b011 WRDM_WRITE_TO_READ_DIFFERENT_MASTER=>0b100 WRXX_WRITE_TO_READ=>0b101 RRDM_READ_TO_READ_DIFFERENT_MASTER=>0b110 WWDM_WRITE_TO_WRITE_DIFFERENT_MASTER=>0b111

Register Name	***MBA Bit Steer Control Register 0***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS0
Address	0000000003010440 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS0_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS0_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS0_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 1***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS1
Address	0000000003010441 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS1_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS1_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS1_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 2***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS2
Address	0000000003010442 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS2_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS2_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS2_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 3***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS3
Address	0000000003010443 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS3_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS3_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS3_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 4***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS4
Address	0000000003010444 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS4_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS4_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS4_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 5***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS5
Address	0000000003010445 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS5_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS5_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS5_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 6***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS6
Address	0000000003010446 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS6_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS6_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS6_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 7***
Mnemonic	MBU.MBA01.MBA_WRD.MBABS7
Address	0000000003010447 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS7_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS7_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS7_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Error Injection***
Mnemonic	MBU.MBA01.MBA_WRD.MBA_INJQ
Address	0000000003010448 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBA_INJQ_CFG_RDTAG_ERR_INJ: Self resetting bit. Writing a one will send a rdtag error inject pulse. After the pulse is sent it will be reset to 0
1	RWX	MBA_INJQ_CFG_RRQ_POP_ERR_INJ: Self resetting bit. Writing a one will send a rrq pop error inject pulse. After the pulse is sent it will be reset to 0
2	RW	MBA_INJQ_CFG_WR_ECC_INJ_MODE: Inject mode for write data ECC injection. Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	MBA_INJQ_CFG_WR_ECC_ERR_INJ: Inject enable. The write inject type (CE, UE, etc..) and specific write data bit(s) corrupted are indicated by the MBA Error Control Register. For single shot mode, bit must be cleared and re-set to enable another error inject. For continuous mode, error injection will occur on valid operations until bit is cleared.

Bits	SCOM	Field Mnemonic: Description
4	RW	MBA_INJQ_CFG_WRD_BUFF_INJ_MODE: Inject mode for write re-order data buffer ECC Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
5	RW	MBA_INJQ_CFG_WRD_BUFFER_CE_INJ: Inject CE error into write reorder data buffer. For single shot mode, but must be cleared and reset to enable another error inject. For continuous mode, error injection will occur on valid operations until bit is cleared. Values: NO_CE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER=>0b0 CE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER_BASED_ON_INJ_MODE=>0b1
6	RW	MBA_INJQ_CFG_WRD_BUFFER_UE_INJ: Inject UE error into write reorder data buffer. For single shot mode, but must be cleared and reset to enable another error inject. For continuous mode, error injection will occur on valid operations until bit is cleared. Values: NO_UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER=>0b0 UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER_BASED_ON_INJ_MODE=>0b1
7:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000 Values: NO_UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER=>0b0 UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER_BASED_ON_INJ_MODE=>0b1

Register Name	***MBA WRD Mode***
Mnemonic	MBU.MBA01.MBA_WRD.MBA_WRD_MODE
Address	0000000003010449 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_WRD_MODE_CFG_WRD_ECC_CHK_DISABLE: Set to disable 8B ECC checking on WRD data bus.
1	RW	MBA_WRD_MODE_CFG_WRD_ECC_COR_DISABLE: Set to disable 8B ECC correction on WRD data bus.
2:4	RW	MBA_WRD_MODE_ECC_METADATA_MODE: Number of metadata in 65th byte. Values: 0_METADATA_8_CHECKBITS=>0b000 1_METADATA_7_CHECKBITS=>0b100 2_METADATA_6_CHECKBITS=>0b010 6_METADATA_2_CHECKBITS___DEFAULT_FOR_VENICE__CENTAUR__=>0b011
5	RW	MBA_WRD_MODE_CFG_MAINT_ECC_CHK_DISABLE: Set to disable 8B ECC checking on maintenance buffer output.
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***FBIST Memory FIR Register***
Mnemonic	FBIST.FBM.FBM_FIR_REG
Address	0000000003010480 (SCOM) 0000000003010481 (SCOM1) 0000000003010482 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_FBM_SCOM_UE: Config reg parity error
1	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_FBM_CMD_CHK_1HOT: Downstream Checker state machine one hot error
2	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_FBM_DS_DATA_DROP: Downstream write data dropped
3	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_FBM_DGEN_1HOT: Read data generation state machine one hot error
4	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_FBM_DGEN_RD_DATA_DROP: Read data generation request dropped
5:14	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_RESERVED_5_14: Reserved_5_14
15	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_INTERNAL_SCOM_ERROR: Internal Scom Error
16	RWX	WOX_AND	WOX_OR	FBM_FIR_REG_INTERNAL_SCOM_ERROR_CLONE: Internal Som Error Clone
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	***FBIST Memory FIR Mask Register***
Mnemonic	FBIST.FBM.FBM_FIR_MASK_REG
Address	0000000003010483 (SCOM) 0000000003010484 (SCOM1) 0000000003010485 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_FBM_SCOM_UE: Masks FIR(0)
1	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_FBM_CMD_CHK_1HOT: Masks FIR(1)
2	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_FBM_DS_DATA_DROP: Masks FIR(2)
3	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_FBM_DGEN_1HOT: Masks FIR(3)
4	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_FBM_DGEN_RD_DATA_DROP: Masks FIR(4)
5:14	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_RESERVED_5_14: Reserved_5_14
15	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_INTERNAL_SCOM_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	FBM_FIR_MASK_REG_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(16)
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	***FBIST Memory FIR Action 0 Register***
Mnemonic	FBIST.FBM.FBM_FIR_ACTION0_REG
Address	0000000003010486 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	FBM_FIR_ACTION0_REG_FBM_SCOM_UE: Action 0 FIR(0)
1	RW	FBM_FIR_ACTION0_REG_FBM_CMD_CHK_1HOT: Action 0 FIR(1)

Bits	SCOM	Field Mnemonic: Description
2	RW	FBM_FIR_ACTION0_REG_FBM_DS_DATA_DROP: Action 0 FIR(2)
3	RW	FBM_FIR_ACTION0_REG_FBM_DGEN_1HOT: Action 0 FIR(3)
4	RW	FBM_FIR_ACTION0_REG_FBM_DGEN_RD_DATA_DROP: Action 0 FIR(4)
5:14	RW	FBM_FIR_ACTION0_REG_RESERVED_5_14: Reserved_5_14
15	RW	FBM_FIR_ACTION0_REG_INTERNAL_SCOM_ERROR: Action 0 FIR(15)
16	RW	FBM_FIR_ACTION0_REG_INTERNAL_SCOM_ERROR_CLONE: Action 0 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	***FBIST Memory FIR Action 1 Register***
Mnemonic	FBIST.FBM.FBM_FIR_ACTION1_REG
Address	0000000003010487 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	FBM_FIR_ACTION1_REG_FBM_SCOM_UE: Action 1 FIR(0)
1	RW	FBM_FIR_ACTION1_REG_FBM_CMD_CHK_1HOT: Action 1 FIR(1)
2	RW	FBM_FIR_ACTION1_REG_FBM_DS_DATA_DROP: Action 1 FIR(2)
3	RW	FBM_FIR_ACTION1_REG_FBM_DGEN_1HOT: Action 1 FIR(3)
4	RW	FBM_FIR_ACTION1_REG_FBM_DGEN_RD_DATA_DROP: Action 1 FIR(4)
5:14	RW	FBM_FIR_ACTION1_REG_RESERVED_5_14: Reserved_5_14
15	RW	FBM_FIR_ACTION1_REG_INTERNAL_SCOM_ERROR: Action 1 FIR(15)
16	RW	FBM_FIR_ACTION1_REG_INTERNAL_SCOM_ERROR_CLONE: Action 1 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	***FBIST Mem Side Memory Registers 0***
Mnemonic	FBIST.FBM.FBMMR0
Address	000000003301048B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR0_CFG_FBM_CMD0: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
4:5	RW	FBMMR0_CFG_FBM_CMD0_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR0_CFG_FBM_CMD0_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBMMR0_CFG_FBM_CMD0_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR0_CFG_FBM_CMD0_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR0_CFG_FBM_CMD0_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBMMR0_CFG_FBM_CMD0_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR0_CFG_FBM_CMD0_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBMMR0_CFG_FBM_CMD1: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
20:21	RW	FBMMR0_CFG_FBM_CMD1_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR0_CFG_FBM_CMD1_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBMMR0_CFG_FBM_CMD1_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR0_CFG_FBM_CMD1_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR0_CFG_FBM_CMD1_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBMMR0_CFG_FBM_CMD1_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR0_CFG_FBM_CMD1_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBMMR0_CFG_FBM_CMD2: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
36:37	RW	FBMMR0_CFG_FBM_CMD2_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR0_CFG_FBM_CMD2_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBMMR0_CFG_FBM_CMD2_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR0_CFG_FBM_CMD2_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR0_CFG_FBM_CMD2_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBMMR0_CFG_FBM_CMD2_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR0_CFG_FBM_CMD2_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBMMR0_CFG_FBM_CMD3: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:53	RW	FBMMR0_CFG_FBM_CMD3_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR0_CFG_FBM_CMD3_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBMMR0_CFG_FBM_CMD3_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR0_CFG_FBM_CMD3_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR0_CFG_FBM_CMD3_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBMMR0_CFG_FBM_CMD3_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR0_CFG_FBM_CMD3_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Mem Side Memory Registers 1***
Mnemonic	FBIST.FBM.FBMMR1
Address	000000000301048C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR1_CFG_FBM_CMD4: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBMMR1_CFG_FBM_CMD4_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR1_CFG_FBM_CMD4_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBMMR1_CFG_FBM_CMD4_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR1_CFG_FBM_CMD4_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR1_CFG_FBM_CMD4_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBMMR1_CFG_FBM_CMD4_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR1_CFG_FBM_CMD4_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
16:19	RW	FBMMR1_CFG_FBM_CMD5: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBMMR1_CFG_FBM_CMD5_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR1_CFG_FBM_CMD5_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBMMR1_CFG_FBM_CMD5_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR1_CFG_FBM_CMD5_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR1_CFG_FBM_CMD5_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBMMR1_CFG_FBM_CMD5_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR1_CFG_FBM_CMD5_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
32:35	RW	FBMMR1_CFG_FBM_CMD6: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBMMR1_CFG_FBM_CMD6_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR1_CFG_FBM_CMD6_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBMMR1_CFG_FBM_CMD6_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR1_CFG_FBM_CMD6_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR1_CFG_FBM_CMD6_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBMMR1_CFG_FBM_CMD6_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR1_CFG_FBM_CMD6_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
48:51	RW	FBMMR1_CFG_FBM_CMD7: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBMMR1_CFG_FBM_CMD7_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR1_CFG_FBM_CMD7_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBMMR1_CFG_FBM_CMD7_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR1_CFG_FBM_CMD7_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR1_CFG_FBM_CMD7_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBMMR1_CFG_FBM_CMD7_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR1_CFG_FBM_CMD7_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Mem Side Memory Registers 2***
Mnemonic	FBIST.FBM.FBMMR2
Address	000000000301048D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR2_CFG_FBM_CMD8: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBMMR2_CFG_FBM_CMD8_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR2_CFG_FBM_CMD8_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBMMR2_CFG_FBM_CMD8_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR2_CFG_FBM_CMD8_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR2_CFG_FBM_CMD8_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
14	RW	FBMMR2_CFG_FBM_CMD8_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR2_CFG_FBM_CMD8_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBMMR2_CFG_FBM_CMD9: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBMMR2_CFG_FBM_CMD9_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR2_CFG_FBM_CMD9_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBMMR2_CFG_FBM_CMD9_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR2_CFG_FBM_CMD9_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR2_CFG_FBM_CMD9_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
30	RW	FBMMR2_CFG_FBM_CMD9_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR2_CFG_FBM_CMD9_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBMMR2_CFG_FBM_CMD10: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBMMR2_CFG_FBM_CMD10_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR2_CFG_FBM_CMD10_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBMMR2_CFG_FBM_CMD10_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR2_CFG_FBM_CMD10_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR2_CFG_FBM_CMD10_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBMMR2_CFG_FBM_CMD10_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR2_CFG_FBM_CMD10_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBMMR2_CFG_FBM_CMD11: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBMMR2_CFG_FBM_CMD11_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR2_CFG_FBM_CMD11_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBMMR2_CFG_FBM_CMD11_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR2_CFG_FBM_CMD11_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR2_CFG_FBM_CMD11_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBMMR2_CFG_FBM_CMD11_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR2_CFG_FBM_CMD11_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Mem Side Memory Registers 3***
Mnemonic	FBIST.FBM.FBMMR3
Address	000000000301048E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR3_CFG_FBM_CMD12: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBMMR3_CFG_FBM_CMD12_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR3_CFG_FBM_CMD12_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
8:11	RW	FBMMR3_CFG_FBM_CMD12_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR3_CFG_FBM_CMD12_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR3_CFG_FBM_CMD12_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBMMR3_CFG_FBM_CMD12_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR3_CFG_FBM_CMD12_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBMMR3_CFG_FBM_CMD13: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBMMR3_CFG_FBM_CMD13_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR3_CFG_FBM_CMD13_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
24:27	RW	FBMMR3_CFG_FBM_CMD13_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR3_CFG_FBM_CMD13_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR3_CFG_FBM_CMD13_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBMMR3_CFG_FBM_CMD13_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR3_CFG_FBM_CMD13_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBMMR3_CFG_FBM_CMD14: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBMMR3_CFG_FBM_CMD14_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR3_CFG_FBM_CMD14_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
40:43	RW	FBMMR3_CFG_FBM_CMD14_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR3_CFG_FBM_CMD14_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR3_CFG_FBM_CMD14_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBMMR3_CFG_FBM_CMD14_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR3_CFG_FBM_CMD14_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBMMR3_CFG_FBM_CMD15: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBMMR3_CFG_FBM_CMD15_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR3_CFG_FBM_CMD15_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
56:59	RW	FBMMR3_CFG_FBM_CMD15_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR3_CFG_FBM_CMD15_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR3_CFG_FBM_CMD15_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBMMR3_CFG_FBM_CMD15_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR3_CFG_FBM_CMD15_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	*FBIST Mem Side Memory Registers 4*
Mnemonic	FBIST.FBM.FBMMR4
Address	000000000301048F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR4_CFG_FBM_CMD16: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
4:5	RW	FBMMR4_CFG_FBM_CMD16_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR4_CFG_FBM_CMD16_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBMMR4_CFG_FBM_CMD16_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR4_CFG_FBM_CMD16_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR4_CFG_FBM_CMD16_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBMMR4_CFG_FBM_CMD16_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR4_CFG_FBM_CMD16_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBMMR4_CFG_FBM_CMD17: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
20:21	RW	FBMMR4_CFG_FBM_CMD17_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR4_CFG_FBM_CMD17_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBMMR4_CFG_FBM_CMD17_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR4_CFG_FBM_CMD17_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR4_CFG_FBM_CMD17_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBMMR4_CFG_FBM_CMD17_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR4_CFG_FBM_CMD17_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBMMR4_CFG_FBM_CMD18: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
36:37	RW	FBMMR4_CFG_FBM_CMD18_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR4_CFG_FBM_CMD18_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBMMR4_CFG_FBM_CMD18_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR4_CFG_FBM_CMD18_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR4_CFG_FBM_CMD18_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBMMR4_CFG_FBM_CMD18_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR4_CFG_FBM_CMD18_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBMMR4_CFG_FBM_CMD19: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111

Bits	SCOM	Field Mnemonic: Description
52:53	RW	FBMMR4_CFG_FBM_CMD19_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR4_CFG_FBM_CMD19_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBMMR4_CFG_FBM_CMD19_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR4_CFG_FBM_CMD19_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR4_CFG_FBM_CMD19_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBMMR4_CFG_FBM_CMD19_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR4_CFG_FBM_CMD19_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Mem Side Memory Registers 5***
Mnemonic	FBIST.FBM.FBMMR5
Address	0000000003010490 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR5_CFG_FBM_CMD20: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBMMR5_CFG_FBM_CMD20_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR5_CFG_FBM_CMD20_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBMMR5_CFG_FBM_CMD20_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR5_CFG_FBM_CMD20_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR5_CFG_FBM_CMD20_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBMMR5_CFG_FBM_CMD20_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR5_CFG_FBM_CMD20_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
16:19	RW	FBMMR5_CFG_FBM_CMD21: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBMMR5_CFG_FBM_CMD21_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR5_CFG_FBM_CMD21_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBMMR5_CFG_FBM_CMD21_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR5_CFG_FBM_CMD21_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR5_CFG_FBM_CMD21_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBMMR5_CFG_FBM_CMD21_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR5_CFG_FBM_CMD21_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
32:35	RW	FBMMR5_CFG_FBM_CMD22: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBMMR5_CFG_FBM_CMD22_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR5_CFG_FBM_CMD22_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBMMR5_CFG_FBM_CMD22_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR5_CFG_FBM_CMD22_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR5_CFG_FBM_CMD22_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBMMR5_CFG_FBM_CMD22_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR5_CFG_FBM_CMD22_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Bits	SCOM	Field Mnemonic: Description
48:51	RW	FBMMR5_CFG_FBM_CMD23: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBMMR5_CFG_FBM_CMD23_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR5_CFG_FBM_CMD23_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBMMR5_CFG_FBM_CMD23_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR5_CFG_FBM_CMD23_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR5_CFG_FBM_CMD23_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBMMR5_CFG_FBM_CMD23_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR5_CFG_FBM_CMD23_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Mem Side Memory Registers 6***
Mnemonic	FBIST.FBM.FBMMR6
Address	0000000003010491 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR6_CFG_FBM_CMD24: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBMMR6_CFG_FBM_CMD24_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR6_CFG_FBM_CMD24_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
8:11	RW	FBMMR6_CFG_FBM_CMD24_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR6_CFG_FBM_CMD24_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR6_CFG_FBM_CMD24_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
14	RW	FBMMR6_CFG_FBM_CMD24_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR6_CFG_FBM_CMD24_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBMMR6_CFG_FBM_CMD25: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBMMR6_CFG_FBM_CMD25_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR6_CFG_FBM_CMD25_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
24:27	RW	FBMMR6_CFG_FBM_CMD25_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR6_CFG_FBM_CMD25_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR6_CFG_FBM_CMD25_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
30	RW	FBMMR6_CFG_FBM_CMD25_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR6_CFG_FBM_CMD25_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBMMR6_CFG_FBM_CMD26: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBMMR6_CFG_FBM_CMD26_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR6_CFG_FBM_CMD26_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
40:43	RW	FBMMR6_CFG_FBM_CMD26_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR6_CFG_FBM_CMD26_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR6_CFG_FBM_CMD26_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
46	RW	FBMMR6_CFG_FBM_CMD26_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR6_CFG_FBM_CMD26_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBMMR6_CFG_FBM_CMD27: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBMMR6_CFG_FBM_CMD27_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR6_CFG_FBM_CMD27_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse
56:59	RW	FBMMR6_CFG_FBM_CMD27_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR6_CFG_FBM_CMD27_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR6_CFG_FBM_CMD27_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1

Bits	SCOM	Field Mnemonic: Description
62	RW	FBMMR6_CFG_FBM_CMD27_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR6_CFG_FBM_CMD27_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Mem Side Memory Registers 7***
Mnemonic	FBIST.FBM.FBMMR7
Address	0000000003010492 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMR7_CFG_FBM_CMD28: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
4:5	RW	FBMMR7_CFG_FBM_CMD28_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
6:7	RW	FBMMR7_CFG_FBM_CMD28_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
8:11	RW	FBMMR7_CFG_FBM_CMD28_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
12	RW	FBMMR7_CFG_FBM_CMD28_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
13	RW	FBMMR7_CFG_FBM_CMD28_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
14	RW	FBMMR7_CFG_FBM_CMD28_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
15	RW	FBMMR7_CFG_FBM_CMD28_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
16:19	RW	FBMMR7_CFG_FBM_CMD29: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
20:21	RW	FBMMR7_CFG_FBM_CMD29_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
22:23	RW	FBMMR7_CFG_FBM_CMD29_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
24:27	RW	FBMMR7_CFG_FBM_CMD29_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
28	RW	FBMMR7_CFG_FBM_CMD29_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
29	RW	FBMMR7_CFG_FBM_CMD29_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
30	RW	FBMMR7_CFG_FBM_CMD29_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
31	RW	FBMMR7_CFG_FBM_CMD29_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
32:35	RW	FBMMR7_CFG_FBM_CMD30: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
36:37	RW	FBMMR7_CFG_FBM_CMD30_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
38:39	RW	FBMMR7_CFG_FBM_CMD30_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
40:43	RW	FBMMR7_CFG_FBM_CMD30_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
44	RW	FBMMR7_CFG_FBM_CMD30_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
45	RW	FBMMR7_CFG_FBM_CMD30_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
46	RW	FBMMR7_CFG_FBM_CMD30_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
47	RW	FBMMR7_CFG_FBM_CMD30_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1
48:51	RW	FBMMR7_CFG_FBM_CMD31: Command Type All other combinations default to read with good cresp See spec for more detail. Values: CACHE_READ_NO_SFU=>0b0000 CACHE_READ_SFU=>0b0001 DDR_READ_NO_SFU=>0b0010 DDR_READ_SFU=>0b0011 WRITE=>0b0100 WRITE_CACHE_BLOCK_ZERO=>0b0101 RMW=>0b1000 RAND=>0b1111
52:53	RW	FBMMR7_CFG_FBM_CMD31_CRSP: Command Cresp Type (used to determine if a command is speculative or non speculative) If a value other than 00 is selected the command will be a speculative command. In FBIST cache mode if set to 10 the code will change to 11 since 10 is not allowed in FBIST cache mode. Values: NO_CRESP=>0b00 BAD_CRESP=>0b01 GOOD_CRESP_SF_UPDATE=>0b10 GOOD_CRESP_NO_SF_UPDATE=>0b11
54:55	RW	FBMMR7_CFG_FBM_CMD31_AMODE: Command Address Mode 00 - seq forward 01 - seq reverse 10 - rand forward 11 - rand reverse

Bits	SCOM	Field Mnemonic: Description
56:59	RW	FBMMR7_CFG_FBM_CMD31_DPAT: Command Data Pattern (used for write only on FBIST Nest side) All patterns may be inverted using bit 14 (cfg_fbn_cmd[0:31]_inv) and bit 0-15 of FBNDCR Values: ALL_ZERO=>0b0000 DATA_EQUALS_ADDRESS=>0b0001 RANDOM=>0b0010 USER_DEFINED=>0b0011 ALL_1=>0b0100 5_REPEAT=>0b0101 3_REPEAT=>0b0110 6_REPEAT=>0b0111 F0_REPEAT=>0b1000 FF00_REPEAT=>0b1001 FFFF0000_REPEAT=>0b1010 FFFFFFFF00000000_REPEAT=>0b1011 FFFFFFFFFFFF0000_REPEAT=>0b1100 RESERVED_UDF=>0b1101 RESERVED_DEA=>0b1110 RESERVED_RANDOM=>0b1111
60	RW	FBMMR7_CFG_FBM_CMD31_EXORD: Command Execution Order Values: EXEC_WHEN_RDY=>0b0 WAIT_FOR_PREV_CMD=>0b1
61	RW	FBMMR7_CFG_FBM_CMD31_RES: Command Reserved Values: DEFAULT=>0b0 DO_NOTHING=>0b1
62	RW	FBMMR7_CFG_FBM_CMD31_INV: Command data pattern invert (used with FBNDCR to determine which bytes are inverted) Values: DATA_INV_OFF=>0b0 DATA_INV_ON=>0b1
63	RW	FBMMR7_CFG_FBM_CMD31_VLD: Command Valid Bit Values: CMD_VALID=>0b0 CMD_INVALID=>0b1

Register Name	***FBIST Memory Parameter Register 0***
Mnemonic	FBIST.FBM.FBMPARM0
Address	0000000003010493 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	FBMPARM0_CFG_FBM_MODE: Sets the FBIST mode Values: DDR_MODE=>0b0 CACHE_MODE=>0b1
1	RW	FBMPARM0_CFG_FBM_SYS_TYPE: Values: PSERIES=>0b0 (POWER8) Reserved=>0b1
2	RW	FBMPARM0_CFG_FBM_MBA_CHK: Configures which MBA will be checked Values: CHECK_MBA01=>0b0 CHECK_MBA23=>0b1

Bits	SCOM	Field Mnemonic: Description
3	RW	FBMPARM0_CFG_FBM_US_MUX_SEL: Mux select for the upstream data path either fbist or ddr traffic. Default is 0. For normal chip mode. Values: DDR_TRAFFIC=>0b0 FBIST_TRAFFIC=>0b1
4	RW	FBMPARM0_CFG_FBM_DDR_MODE_OVRD: When on, this will shut off the fbist memory side logic. Allowing DDR mode to be used with DRAMs. This is not supported and should be used as a debug consideration only.
5:7	RW	FBMPARM0_RESERVED_5_7: Reserved Values: RESERVED_5_7=>0b000
8	RW	FBMPARM0_CFG_FBM_ADDR_CHK: Turn on or off address checking
9	RW	FBMPARM0_RESERVED_9: Reserved
10	RW	FBMPARM0_CFG_FBM_DP_TAG_LOC: The dptag includes an invert bit, the data pattern and wr tag bits. The 12 dp pattern bits will be placed in the 12b starting at bit 32 of the DWs selected. Be sure that the RMW command avoids writing to these bit positions. RMW is allowed to overwrite these bit positions ONLY for an entire cache line merge. Values: TAG_IN_DW048C=>0b0 TAG_IN_DW159D=>0b1
11	RW	FBMPARM0_CFG_FBM_DDR4: Choose ddr3 or ddr4 mem type Values: DDR3=>0b0 DDR4=>0b1
12	RW	FBMPARM0_CFG_FBM_DS_CRC: Turn on or off Downstream CRC generation
13	RW	FBMPARM0_CFG_FBM_US_CRC: Turn on or off upstream crc checking
14:15	RW	FBMPARM0_RESERVED_14_15: Reserved Reserved
16	RW	FBMPARM0_CFG_FBM_RST_KEEPER: FBM Reset keeper Values: DOES_NOTHING=>0b0 RESET_KEEPER=>0b1
17	RW	FBMPARM0_CFG_FBM_CACHELINE_CHK: Choose a specific command tag to read a full cache line into the expected data register, or use the next full upstream cache line Values: USER_SPECIFIED=>0b0 NEXT=>0b1
18	RW	FBMPARM0_CFG_FBM_2N_ADDR: Turn on or off 2N addr mode
19	RW	FBMPARM0_CFG_FBN_MBSXCRQ5: Should be set to same value as register bit mbsxcrq(5)
20:63	RO	constant=0b00000000000000000000000000000000000000000000

Register Name	***FBIST Memory Read Data Delay Register***
Mnemonic	FBIST.FBM.FBMRDDR
Address	0000000003010494 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FBMRDDR_CFG_FBM_DATA_RD_DLY: Amount of delay in memory clock 2 cycles before the pseudo read data is made available to MBS.
8:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*FBIST Memory Data Config Register*
Mnemonic	FBIST.FBM.FBMDCR
Address	0000000003010497 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	FBMDCR_CFG_FBM_DATA_INV: Data inversion configuration is used in conjunction with the data pattern inversion bits in the fbmmr0:7 registers. Each bit from 0 through 16 determines which dw of data will be inverted. In example, if b0 is 1 then dw0 will be inverted should the data pattern inversion bit for the commands (in fbmmr0:7) is also set. This allows the used to create data traffic on certain buses that will flip every cycle, etc.
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*FBIST Memory Command Reporting Config Register*
Mnemonic	FBIST.FBM.FBMCRCR
Address	0000000003010499 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FBMCRCR_CFG_FBM_CMD_CHK_TAG: Bits 0:7 The user specified command checking tag, used to select a tag to read out the full cache line (bit0 is ignored). Used with fbmparm0(17)
8:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*FBIST Memory RMW Cmd Register*
Mnemonic	FBIST.FBM.FBMRMWC
Address	000000003301049A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMRMWC_CFG_FBM_RMW_FUNC: Default is for RMW partial write. No ALU support at this time
4	RW	FBMRMWC_RESERVED_4: 1.Reserved
5:11	RW	FBMRMWC_CFG_FBM_RMW_TSZ: Default set for 1 Byte Partial write
12	RW	FBMRMWC_RESERVED_12: Reserved
13:19	RW	FBMRMWC_CFG_FBM_RMW_ADDR: Sets the byte address in the cache line for the partial write (be sure not to use the location of the wrtag and data pattern tag) Special considerations should be taken when running a test with random data as the first byte of each DW is used to reconstruct the data for checking.
20:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***FBIST Memory Memory Config Register 0***
Mnemonic	FBIST.FBM.FBMMC0
Address	000000000301049E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	FBMMC0_CFG_FBM_M0S0: Master0 Slave0 setup for mem config
4:7	RW	FBMMC0_CFG_FBM_M0S1: Master0 Slave1 setup for mem config
8:11	RW	FBMMC0_CFG_FBM_M0S2: Master0 Slave2 setup for mem config
12:15	RW	FBMMC0_CFG_FBM_M0S3: Master0 Slave3 setup for mem config
16:19	RW	FBMMC0_CFG_FBM_M1S0: Master1Slave0 setup for mem config
20:23	RW	FBMMC0_CFG_FBM_M1S1: Master1 Slave1 setup for mem config
24:27	RW	FBMMC0_CFG_FBM_M1S2: Master1 Slave2 setup for mem config
28:31	RW	FBMMC0_CFG_FBM_M1S3: Master1 Slave3 setup for mem config
32:35	RW	FBMMC0_CFG_FBM_M2S0: Master2 Slave0 setup for mem config
36:39	RW	FBMMC0_CFG_FBM_M3S0: Master3 Slave0 setup for mem config
40:43	RW	FBMMC0_CFG_FBM_MEM_TYPE: Mem type selection Values: ALL_MASTER_NO_TSVNO_LR=>0b0000 4_MASTER_2H_TSV=>0b0001 4_MASTER_4HS=>0b0010
44:63	RO	constant=0b00000000000000000000 Values: ALL_MASTER_NO_TSVNO_LR=>0b0000 4_MASTER_2H_TSV=>0b0001 4_MASTER_4HS=>0b0010

Register Name	***FBIST Memory User Data Config Registers 0***
Mnemonic	FBIST.FBM.FBMUD0
Address	00000000030104A2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD0_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 1***
Mnemonic	FBIST.FBM.FBMUD1
Address	00000000030104A3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD1_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 2*
Mnemonic	FBIST.FBM.FBMUD2
Address	00000000030104A4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD2_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 3*
Mnemonic	FBIST.FBM.FBMUD3
Address	00000000030104A5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD3_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 4*
Mnemonic	FBIST.FBM.FBMUD4
Address	00000000030104A6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD4_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 5*
Mnemonic	FBIST.FBM.FBMUD5
Address	00000000030104A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD5_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 6*
Mnemonic	FBIST.FBM.FBMUD6
Address	00000000030104A8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD6_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 7*
Mnemonic	FBIST.FBM.FBMUD7
Address	00000000030104A9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD7_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 8*
Mnemonic	FBIST.FBM.FBMUD8
Address	00000000030104AA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD8_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory User Data Config Registers 9*
Mnemonic	FBIST.FBM.FBMUD9
Address	00000000030104AB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD9_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 10***
Mnemonic	FBIST.FBM.FBMUD10
Address	00000000030104AC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD10_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 11***
Mnemonic	FBIST.FBM.FBMUD11
Address	00000000030104AD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD11_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 12***
Mnemonic	FBIST.FBM.FBMUD12
Address	00000000030104AE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD12_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 13***
Mnemonic	FBIST.FBM.FBMUD13
Address	00000000030104AF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD13_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 14***
Mnemonic	FBIST.FBM.FBMUD14
Address	00000000030104B0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD14_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory User Data Config Registers 15***
Mnemonic	FBIST.FBM.FBMUD15
Address	00000000030104B1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMUD15_CFG_FBM_DATA_USR_N: User defined data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Miss Error Counter 0***
Mnemonic	FBIST.FBM.FBMDMEC0
Address	00000000030104B3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBMDMEC0_FBM_ERR_CNTR0: Data miscompare error counter
8:15	ROX	FBMDMEC0_FBM_ERR_CNTR1: Data miscompare error counter
16:23	ROX	FBMDMEC0_FBM_ERR_CNTR2: Data miscompare error counter
24:31	ROX	FBMDMEC0_FBM_ERR_CNTR3: Data miscompare error counter
32:39	ROX	FBMDMEC0_FBM_ERR_CNTR4: Data miscompare error counter
40:47	ROX	FBMDMEC0_FBM_ERR_CNTR5: Data miscompare error counter
48:55	ROX	FBMDMEC0_FBM_ERR_CNTR6: Data miscompare error counter
56:63	ROX	FBMDMEC0_FBM_ERR_CNTR7: Data miscompare error counter

Register Name	***FBIST Memory Data Mis Error Counter 1***
Mnemonic	FBIST.FBM.FBMDMEC1
Address	00000000030104B4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBMDMEC1_FBM_ERR_CNTR8: Data miscompare error counter
8:15	ROX	FBMDMEC1_FBM_ERR_CNTR9: Data miscompare error counter
16:23	ROX	FBMDMEC1_FBM_ERR_CNTR10: Data miscompare error counter
24:31	ROX	FBMDMEC1_FBM_ERR_CNTR11: Data miscompare error counter
32:39	ROX	FBMDMEC1_FBM_ERR_CNTR12: Data miscompare error counter
40:47	ROX	FBMDMEC1_FBM_ERR_CNTR13: Data miscompare error counter
48:55	ROX	FBMDMEC1_FBM_ERR_CNTR14: Data miscompare error counter
56:63	ROX	FBMDMEC1_FBM_ERR_CNTR15: Data miscompare error counter

Register Name	***FBIST Memory Data Mis Error Counter 2***
Mnemonic	FBIST.FBM.FBMDMEC2
Address	00000000030104B5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBMDMEC2_FBM_ERR_CNTR16: Data miscompare error counter
8:15	ROX	FBMDMEC2_FBM_ERR_CNTR17: Data miscompare error counter
16:23	ROX	FBMDMEC2_FBM_ERR_CNTR18: Data miscompare error counter
24:31	ROX	FBMDMEC2_FBM_ERR_CNTR19: Data miscompare error counter
32:39	ROX	FBMDMEC2_FBM_ERR_CNTR20: Data miscompare error counter
40:47	ROX	FBMDMEC2_FBM_ERR_CNTR21: Data miscompare error counter
48:55	ROX	FBMDMEC2_FBM_ERR_CNTR22: Data miscompare error counter
56:63	ROX	FBMDMEC2_FBM_ERR_CNTR23: Data miscompare error counter

Register Name	***FBIST Memory Data Mis Error Counter 3***
Mnemonic	FBIST.FBM.FBMDMEC3
Address	00000000030104B6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBMDMEC3_FBM_ERR_CNTR24: Data miscompare error counter
8:15	ROX	FBMDMEC3_FBM_ERR_CNTR25: Data miscompare error counter
16:23	ROX	FBMDMEC3_FBM_ERR_CNTR26: Data miscompare error counter
24:31	ROX	FBMDMEC3_FBM_ERR_CNTR27: Data miscompare error counter
32:39	ROX	FBMDMEC3_FBM_ERR_CNTR28: Data miscompare error counter
40:47	ROX	FBMDMEC3_FBM_ERR_CNTR29: Data miscompare error counter
48:55	ROX	FBMDMEC3_FBM_ERR_CNTR30: Data miscompare error counter
56:63	ROX	FBMDMEC3_FBM_ERR_CNTR31: Data miscompare error counter

Register Name	***FBIST Memory Data Compare Mask Register 0***
Mnemonic	FBIST.FBM.FBMDCM0
Address	00000000030104B8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM0_CFG_FBM_DATA_CMP_MASK0: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 1***
Mnemonic	FBIST.FBM.FBMDCM1
Address	00000000030104B9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM1_CFG_FBM_DATA_CMP_MASK1: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 2***
Mnemonic	FBIST.FBM.FBMDCM2
Address	00000000030104BA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM2_CFG_FBM_DATA_CMP_MASK2: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 3***
Mnemonic	FBIST.FBM.FBMDCM3
Address	00000000030104BB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM3_CFG_FBM_DATA_CMP_MASK3: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 4***
Mnemonic	FBIST.FBM.FBMDCM4
Address	00000000030104BC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM4_CFG_FBM_DATA_CMP_MASK4: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 5***
Mnemonic	FBIST.FBM.FBMDCM5
Address	00000000030104BD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM5_CFG_FBM_DATA_CMP_MASK5: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 6***
Mnemonic	FBIST.FBM.FBMDCM6
Address	00000000030104BE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM6_CFG_FBM_DATA_CMP_MASK6: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 7***
Mnemonic	FBIST.FBM.FBMDCM7
Address	00000000030104BF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM7_CFG_FBM_DATA_CMP_MASK7: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 8***
Mnemonic	FBIST.FBM.FBMDCM8
Address	00000000030104C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM8_CFG_FBM_DATA_CMP_MASK8: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 9***
Mnemonic	FBIST.FBM.FBMDCM9
Address	00000000030104C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM9_CFG_FBM_DATA_CMP_MASK9: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 10***
Mnemonic	FBIST.FBM.FBMDCM10
Address	00000000030104C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM10_CFG_FBM_DATA_CMP_MASK10: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 11***
Mnemonic	FBIST.FBM.FBMDCM11
Address	00000000030104C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM11_CFG_FBM_DATA_CMP_MASK11: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 12***
Mnemonic	FBIST.FBM.FBMDCM12
Address	00000000030104C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM12_CFG_FBM_DATA_CMP_MASK12: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 13***
Mnemonic	FBIST.FBM.FBMDCM13
Address	00000000030104C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM13_CFG_FBM_DATA_CMP_MASK13: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 14***
Mnemonic	FBIST.FBM.FBMDCM14
Address	00000000030104C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM14_CFG_FBM_DATA_CMP_MASK14: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Data Compare Mask Register 15***
Mnemonic	FBIST.FBM.FBMDCM15
Address	00000000030104C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	FBMDCM15_CFG_FBM_DATA_CMP_MASK15: Data compare mask register when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 0*
Mnemonic	FBIST.FBM.FBMED0
Address	00000000030104C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED0_FBM_DATA_EXP0: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 1*
Mnemonic	FBIST.FBM.FBMED1
Address	00000000030104C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED1_FBM_DATA_EXP1: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 2*
Mnemonic	FBIST.FBM.FBMED2
Address	00000000030104CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED2_FBM_DATA_EXP2: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 3*
Mnemonic	FBIST.FBM.FBMED3
Address	00000000030104CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED3_FBM_DATA_EXP3: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 4*
Mnemonic	FBIST.FBM.FBMED4
Address	00000000030104CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED4_FBM_DATA_EXP4: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 5*
Mnemonic	FBIST.FBM.FBMED5
Address	00000000030104CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED5_FBM_DATA_EXP5: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 6*
Mnemonic	FBIST.FBM.FBMED6
Address	00000000030104CE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED6_FBM_DATA_EXP6: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 7*
Mnemonic	FBIST.FBM.FBMED7
Address	00000000030104CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED7_FBM_DATA_EXP7: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 8*
Mnemonic	FBIST.FBM.FBMED8
Address	00000000030104D0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED8_FBM_DATA_EXProcessor: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 9*
Mnemonic	FBIST.FBM.FBMED9
Address	00000000030104D1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED9_FBM_DATA_EXP9: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 10*
Mnemonic	FBIST.FBM.FBMED10
Address	00000000030104D2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED10_FBM_DATA_EXP10: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Expected Data Register 11*
Mnemonic	FBIST.FBM.FBMED11
Address	00000000030104D3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED11_FBM_DATA_EXP11: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Expected Data Register 12***
Mnemonic	FBIST.FBM.FBMED12
Address	00000000030104D4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED12_FBM_DATA_EXP12: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Expected Data Register 13***
Mnemonic	FBIST.FBM.FBMED13
Address	00000000030104D5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED13_FBM_DATA_EXP13: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Expected Data Register 14***
Mnemonic	FBIST.FBM.FBMED14
Address	00000000030104D6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED14_FBM_DATA_EXP14: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Expected Data Register 15***
Mnemonic	FBIST.FBM.FBMED15
Address	00000000030104D7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMED15_FBM_DATA_EXP15: Expected Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Received Data Register 0*
Mnemonic	FBIST.FBM.FBMRD0
Address	00000000030104D8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD0_FBM_DATA_RX0: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Received Data Register 1*
Mnemonic	FBIST.FBM.FBMRD1
Address	00000000030104D9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD1_FBM_DATA_RX1: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Received Data Register 2*
Mnemonic	FBIST.FBM.FBMRD2
Address	00000000030104DA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD2_FBM_DATA_RX2: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Received Data Register 3*
Mnemonic	FBIST.FBM.FBMRD3
Address	00000000030104DB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD3_FBM_DATA_RX3: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 4***
Mnemonic	FBIST.FBM.FBMRD4
Address	00000000030104DC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD4_FBM_DATA_RX4: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 5***
Mnemonic	FBIST.FBM.FBMRD5
Address	00000000030104DD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD5_FBM_DATA_RX5: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 6***
Mnemonic	FBIST.FBM.FBMRD6
Address	00000000030104DE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD6_FBM_DATA_RX6: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 7***
Mnemonic	FBIST.FBM.FBMRD7
Address	00000000030104DF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD7_FBM_DATA_RX7: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 8***
Mnemonic	FBIST.FBM.FBMRD8
Address	00000000030104E0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD8_FBM_DATA_RX8: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 9***
Mnemonic	FBIST.FBM.FBMRD9
Address	00000000030104E1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD9_FBM_DATA_RX9: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 10***
Mnemonic	FBIST.FBM.FBMRD10
Address	00000000030104E2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD10_FBM_DATA_RX10: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 11***
Mnemonic	FBIST.FBM.FBMRD11
Address	00000000030104E3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD11_FBM_DATA_RX11: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 12***
Mnemonic	FBIST.FBM.FBMRD12
Address	00000000030104E4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD12_FBM_DATA_RX12: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 13***
Mnemonic	FBIST.FBM.FBMRD13
Address	00000000030104E5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD13_FBM_DATA_RX13: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 14***
Mnemonic	FBIST.FBM.FBMRD14
Address	00000000030104E6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD14_FBM_DATA_RX14: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	***FBIST Memory Received Data Register 15***
Mnemonic	FBIST.FBM.FBMRD15
Address	00000000030104E7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMRD15_FBM_DATA_RX15: Received Data (0:63), when all 16 regs are concatenated there are bits (0:1023)

Register Name	*FBIST Memory Error Address Register*
Mnemonic	FBIST.FBM.FBMEA
Address	00000000030104E8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	FBMEA_CFG_FBM_ERR_ADDR: Holds value of the Address associated with the first data comp error

Register Name	*FBIST Memory Error Info Register*
Mnemonic	FBIST.FBM.FBMEIR
Address	00000000030104E9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	FBMEIR_FBM_ERR_CMD_TAG: Reports the cmd tag associated with the data miscompare error. Bit 0 is not used
8:15	ROX	FBMEIR_FBM_ERR_DATA_PAT: Reports the data pattern associated with the data miscompare error. Bit 0:1 first DW of cache line with error Bit 2 RMW Commands Bit 3 Data inversion Bit 4:7 Data pattern
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	*FBIST Memory Random Data Seed Register 0*
Mnemonic	FBIST.FBM.FBMRDSR0
Address	00000000030104EC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED0: DW0 Random Data Seed, 8 bit seed used to generate 64b of data for DW0
8:15	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED1: DW1 Random Data Seed, 8 bit seed used to generate 64b of data for DW1
16:23	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED2: DW2 Random Data Seed, 8 bit seed used to generate 64b of data for DW2
24:31	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED3: DW3 Random Data Seed, 8 bit seed used to generate 64b of data for DW3
32:39	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED4: DW4 Random Data Seed, 8 bit seed used to generate 64b of data for DW4
40:47	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED5: DW5 Random Data Seed, 8 bit seed used to generate 64b of data for DW5
48:55	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED6: DW6 Random Data Seed, 8 bit seed used to generate 64b of data for DW6
56:63	RW	FBMRDSR0_CFG_FBM_DATA_RND_SEED7: DW7 Random Data Seed, 8 bit seed used to generate 64b of data for DW7

Register Name	*FBIST Memory Random Data Seed Register 1*
Mnemonic	FBIST.FBM.FBMRDSR1
Address	00000000030104ED (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEED8: DW8 Random Data Seed, 8 bit seed used to generate 64b of data for DW8
8:15	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEED9: DW9 Random Data Seed, 8 bit seed used to generate 64b of data for DW9
16:23	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEEDA: DWA Random Data Seed, 8 bit seed used to generate 64b of data for DWA
24:31	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEEDB: DWB Random Data Seed, 8 bit seed used to generate 64b of data for DWB
32:39	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEEDC: DWC Random Data Seed, 8 bit seed used to generate 64b of data for DWC
40:47	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEEDD: DWD Random Data Seed, 8 bit seed used to generate 64b of data for DWD
48:55	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEEDE: DWE Random Data Seed, 8 bit seed used to generate 64b of data for DWE
56:63	RW	FBMRDSR1_CFG_FBM_DATA_RND_SEEDF: DWF Random Data Seed, 8 bit seed used to generate 64b of data for DWF

Register Name	*FBIST Memory MISR0 Register*
Mnemonic	FBIST.FBM.FBMM0
Address	00000000030104F0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	FBMM0_FBM_DS_DATA_MISR: Downstream data MISR
12:19	ROX	FBMM0_FBM_DS_CMD_MISR: Downstream command MISR
20:55	ROX	FBMM0_FBM_DS_ADDR_MISR: Downstream Address MISR (bit20 is always 0, not used)
56:63	RO	constant=0b00000000

Register Name	*FBIST Memory MISR1 Register*
Mnemonic	FBIST.FBM.FBMM1
Address	00000000030104F1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	FBMM1_FBM_US_DATA_MISR0: Upstream data MISR 0
12:23	ROX	FBMM1_FBM_US_DATA_MISR1: Upstream data MISR 1
24:35	ROX	FBMM1_FBM_US_DATA_MISR2: Upstream data MISR 2
36:47	ROX	FBMM1_FBM_US_DATA_MISR3: Upstream data MISR 3
48:63	RO	constant=0b0000000000000000

Register Name	***MBA Fault Isolation Register (MBAFIR)***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBAFIRQ
Address	0000000003010600 (SCOM) 0000000003010601 (SCOM1) 0000000003010602 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBAFIRQ_INVALID_MAINT_CMD: Invalid Maintenance Command This bit is set when a maintenance command is started with an invalid maintenance command code entered in MBMCT
1	RWX	WOX_AND	WOX_OR	MBAFIRQ_INVALID_MAINT_ADDRESS: Invalid Maintenance Address This bit is set when a maintenance command is started when an invalid address is detected for a single or multiple address command
2	RWX	WOX_AND	WOX_OR	MBAFIRQ_MULTI_ADDRESS_MAINT_TIMEOUT: Maintenance Timeout This bit is set when a single maintenance operation (part of a milt-address maintenance op) does not complete in TBD time. (recommend > 100mS) - extra credit, implement if time allows
3	RWX	WOX_AND	WOX_OR	MBAFIRQ_INTERNAL_FSM_ERROR: Internal FSM Error A parity error occurred on an internal FSM
4	RWX	WOX_AND	WOX_OR	MBAFIRQ_MCBIST_ERROR: MCBIST Error This bit is set when MCBIST has detected an error while running its test.
5	RWX	WOX_AND	WOX_OR	MBAFIRQ_SCOM_CMD_REG_PE: SCOM Command Register Parity Errors Parity Error occurred on a scom command register
6	RWX	WOX_AND	WOX_OR	MBAFIRQ_CHANNEL_CHKSTP_ERR: Channel Checkstop Errors Errors that would lead to a channel checkstop.
7	RWX	WOX_AND	WOX_OR	MBAFIRQ_WRD_CAW2_DATA_CE_UE_ERR: UE or CE Error in WRD caw2 data latches
8:14	RWX	WOX_AND	WOX_OR	MBAFIRQ_RESERVED_8_14: RESERVED
15	RWX	WOX_AND	WOX_OR	MBAFIRQ_INTERNAL_SCOM_ERROR: Internal Scom Error
16	RWX	WOX_AND	WOX_OR	MBAFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal Som Error Clone
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000

Register Name	*MBA Fault Isolation Mask Register (MBAFIRMASK)*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBAFIRMASK
Address	0000000003010603 (SCOM) 0000000003010604 (SCOM1) 0000000003010605 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBAFIRMASK_INVALID_MAINT_CMD: Masks FIR(0)
1	RW	WO_AND	WO_OR	MBAFIRMASK_INVALID_MAINT_ADDRESS: Masks FIR(1)
2	RW	WO_AND	WO_OR	MBAFIRMASK_MULTI_ADDRESS_MAINT_TIMEOUT: Masks FIR(2)
3	RW	WO_AND	WO_OR	MBAFIRMASK_INTERNAL_FSM_ERROR: Masks FIR(3)
4	RW	WO_AND	WO_OR	MBAFIRMASK_MCBIST_ERROR: Masks FIR(4)
5	RW	WO_AND	WO_OR	MBAFIRMASK_SCOM_CMD_REG_PE: Masks FIR(5)
6	RW	WO_AND	WO_OR	MBAFIRMASK_CHANNEL_CHKSTP_ERR: Masks FIR(6)
7	RW	WO_AND	WO_OR	MBAFIRMASK_WRD_CAW2_DATA_CE_UE_ERR: Masks FIR(7)
8:14	RW	WO_AND	WO_OR	MBAFIRMASK_RESERVED_8_14: RESERVED
15	RW	WO_AND	WO_OR	MBAFIRMASK_INTERNAL_SCOM_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	MBAFIRMASK_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(16)
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBA Fault Isolation Action0 Register (MBAFIRACT0)*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBAFIRACT0
Address	0000000003010606 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAFIRACT0_INVALID_MAINT_CMD: Action 0 FIR(0)
1	RW	MBAFIRACT0_INVALID_MAINT_ADDRESS: Action 0 FIR(1)
2	RW	MBAFIRACT0_MULTI_ADDRESS_MAINT_TIMEOUT: Action 0 FIR(2)
3	RW	MBAFIRACT0_INTERNAL_FSM_ERROR: Action 0 FIR(3)
4	RW	MBAFIRACT0_MCBIST_ERROR: Action 0 FIR(4)
5	RW	MBAFIRACT0_SCOM_CMD_REG_PE: Action 0 FIR(5)
6	RW	MBAFIRACT0_CHANNEL_CHKSTP_ERR: Action 0 FIR(6)
7	RW	MBAFIRACT0_WRD_CAW2_DATA_CE_UE_ERR: Action 0 FIR(7)
8:14	RW	MBAFIRACT0_RESERVED_8_14: RESERVED
15	RW	MBAFIRACT0_INTERNAL_SCOM_ERROR: Action 0 FIR(15)
16	RW	MBAFIRACT0_INTERNAL_SCOM_ERROR_CLONE: Action 0 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	***MBA Fault Isolation Action1 Register (MBAFIRACT1)***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBAFIRACT1
Address	0000000003010607 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAFIRACT1_INVALID_MAINT_CMD: Action 1 FIR(0)
1	RW	MBAFIRACT1_INVALID_MAINT_ADDRESS: Action 1 FIR(1)
2	RW	MBAFIRACT1_MULTI_ADDRESS_MAINT_TIMEOUT: Action 1 FIR(2)
3	RW	MBAFIRACT1_INTERNAL_FSM_ERROR: Action 1 FIR(3)
4	RW	MBAFIRACT1_MCBIST_ERROR: Action 1 FIR(4)
5	RW	MBAFIRACT1_SCOM_CMD_REG_PE: Action 1 FIR(5)
6	RW	MBAFIRACT1_CHANNEL_CHKSTP_ERR: Action 1 FIR(6)
7	RW	MBAFIRACT1_WRD_CAW2_DATA_CE_UE_ERR: Action 1 FIR(7)
8:14	RW	MBAFIRACT1_RESERVED_8_14: RESERVED
15	RW	MBAFIRACT1_INTERNAL_SCOM_ERROR: Action 1 FIR(15)
16	RW	MBAFIRACT1_INTERNAL_SCOM_ERROR_CLONE: Action 1 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000

Register Name	***MBA Fault Isolation WOF Register (MBAFIRWOF)***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBAFIRWOF
Address	0000000003010608 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBAFIRWOF_INVALID_MAINT_CMD: Who's On First (WOF0) Register
1	ROX	MBAFIRWOF_INVALID_MAINT_ADDRESS: Who's On First (WOF1) Register
2	ROX	MBAFIRWOF_MULTI_ADDRESS_MAINT_TIMEOUT: Who's On First (WOF2) Register
3	ROX	MBAFIRWOF_INTERNAL_FSM_ERROR: Who's On First (WOF3) Register
4	ROX	MBAFIRWOF_MCBIST_ERROR: Who's On First (WOF4) Register
5	ROX	MBAFIRWOF_SCOM_CMD_REG_PE: Who's On First (WOF5) Register
6	ROX	MBAFIRWOF_CHANNEL_CHKSTP_ERR: Who's On First (WOF6) Register
7	ROX	MBAFIRWOF_WRD_CAW2_DATA_CE_UE_ERR: Who's On First (WOF7) Register
8:14	ROX	MBAFIRWOF_RESERVED_8_14: RESERVED
15	ROX	MBAFIRWOF_INTERNAL_SCOM_ERROR: Who's On First (WOF15) Register
16	ROX	MBAFIRWOF_INTERNAL_SCOM_ERROR_CLONE: Who's On First (WOF16) Register
17:63	RO	constant=0b00000000000000000000000000000000000000000000000

Register Name	*MBA Maintenance Command Type Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBMCTQ
Address	000000000301060A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBMCTQ_MAINT_CMD_TYPE: Maintenance Command Type Values: TIMEBASE_READ=>0b00000 TIMEBASE_SCRUB=>0b00001 TIMEBASE_STEER_CLEANUP=>0b00010 TIMEBASE_INIT=>0b00011 TIMEBASE_RANDOM_INIT=>0b00100 SUPERFAST_READ=>0b01000 SUPERFAST_INIT=>0b01001 SUPERFAST_RANDOM_INIT=>0b01010 MEMORY_DISPLAY=>0b10000 MEMORY_ALTER=>0b10001 MEMORY_ALTER_WITH_ECC_OVERRIDE=>0b10010 ATOMIC_ALTER_ERROR_INJECT=>0b10011 INCREMENT_MBMACA_ADDRESS=>0b10100
5	RW	MBMCTQ_SF_INCREMENT_MODE: Superfast Address Increment Mode (valid for all maint cmd types) 0 - non superfast addressing mode 1 - Superfast addressing mode
6	RW	MBMCTQ_BURST_WINDOW_SEL: Burst Window Select 0 - 512 Maint Clks 1 - 536870912 Maint Clks
7:8	RW	MBMCTQ_RESERVED_7_8: Reserved
9:10	RW	MBMCTQ_TIMEBASE_SEL: Time base Select Values: 1_MAINT_CLK=>0b00 8192_MAINT_CLKS=>0b01
11	RW	MBMCTQ_TIMEBASE_BURST_SEL: Time base burst select 0 - disable burst mode 1 - enable burst mode: MBMCT(12:23) = operation interval, MBMCT(24:31) = burst window length, MBMCT(32:39) = burst interval
12:23	RW	MBMCTQ_TIMEBASE_INTERVAL: Time Base interval The operation interval for Timebase operations equals the time base x MBMCT(12:23). The time base is selected by bits 9 and 10 above.
24:31	RW	MBMCTQ_BURST_WINDOW: Burst window The burst window for timebase operations with burst mode enabled equals the time base x MBMCT(24:31). The time base is selected by bits 6 above.
32:39	RW	MBMCTQ_BURST_INTERVAL: burst interval The burst interval for timebase operations with burst mode enabled equals the number of burst windows that will have no operations occurring in them.
40:63	RO	constant=0b000000000000000000000000

Register Name	*MBA Maintenance Command Control Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBMCCQ
Address	000000000301060B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMCCQ_MAINT_CMD_START: Maintenance Command Start When set, the maintenance op specified in MBMCT is started. Bit is reset by hardware.

Bits	SCOM	Field Mnemonic: Description
1	RWX	MBMCCQ_MAINT_CMD_STOP: Maintenance Command Stop When set, the maintenance op currently running is stopped. Bit is reset by hardware. The maintenance command will stop after the next memory operation.
2:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBA Maintenance Command Status Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBMSRQ
Address	000000000301060C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMSRQ_MAINT_CMD_IP: Maintenance Command in Progress (RW) Status bit, is set by hardware when maintenance command is in progress and reset by hardware when maintenance command is complete.
1:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBA Maintenance Command Address Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBMACAQ
Address	000000000301060D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBMACAQ_CMD_MASTER_RANK: Master Rank Master rank address for memory operations. For the memory buffer, Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBMACAQ_CMD_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBMACAQ_CMD_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBMACAQ_CMD_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBMACAQ_CMD_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40:46	RWX	MBMACAQ_CMD_ERR_STATUS: Error Status bits These bits are set to indicate the error conditions that occurred when a stop on error condition has been detected. The address associated with these error status bits are contained in bits 0:39 as described above. 40: NCE 41: SCE 42: MCE 43: RCE 44: MPE 45: SUE 46: UE Note: multiple error status bits may be set due to unique errors on each 64 byte pieces of read data. Note: the error status bits are only set when a stop-on-error condition is detected, and are reloaded on the next stop-on-error condition

Bits	SCOM	Field Mnemonic: Description
47:58	RWX	MBMACAQ_MRANK_SCRUBED: Master Rank Scrubbed bits These bits indicate which master ranks have been scrubbed at least 1 times. User must manually reset these bits buy writing 0's to them. Salerno Mode 0 - slot 0 master rank 0 scrubbed 1 - slot 0 master rank 1 scrubbed 2 - slot 0 master rank 2 scrubbed 3 - slot 0 master rank 3 scrubbed 4 - slot 1 master rank 0 scrubbed 5 - slot 1 master rank 1 scrubbed 6 - slot 1 master rank 2 scrubbed 7 - slot 1 master rank 3 scrubbed 8 - slot 2 master rank 0 scrubbed 9 - slot 2 master rank 1 scrubbed 10 - slot 2 master rank 2 scrubbed 11 - slot 2 master rank 3 scrubbed Memory Buffer Mode 0 - mrank 0 scrubbed 1 - mrank 1 scrubbed 2 - mrank 2 scrubbed 3 - mrank 3 scrubbed 4 - mrank 4 scrubbed 5 - mrank 5 scrubbed 6 - mrank 6 scrubbed 7 - mrank 7 scrubbed 8 - unused 9 - unused 10 -unused 11 - unused
59:63	RO	constant=0b00000

Register Name	*MBA Maintenance Command End Address Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBMEAQ
Address	000000000301060E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBMEAQ_END_MASTER_RANK: Master Rank Master rank address for memory operations. For the memory buffer, Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RW	MBMEAQ_END_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RW	MBMEAQ_END_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RW	MBMEAQ_END_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RW	MBMEAQ_END_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40:63	RO	constant=0b000000000000000000000000

Register Name	*MBA Memory Scrub/Read Control Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBASCTLQ
Address	000000000301060F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBASCTLQ_STOP_ETE_NOW: Stop on ete immediate, attention set when ete occurs When set, a scrubread op will immediately stop when an Error Threshold Equal (ETE) condition is detected.
1	RW	MBASCTLQ_STOP_ETE_RANK_END: Stop on ete end of rank When set, a scrubread op will stop at the end of the current rank, when an Error Threshold Equal condition is detected. Attention is set at the end of the rank.
2	RW	MBASCTLQ_STOP_NCE_HARD: Stop on Hard NCE ETE When set, a scrubread op will stop (immediate or end of rank) when a Hard NCE threshold equal error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.

Bits	SCOM	Field Mnemonic: Description
3	RW	MBASCTLQ_STOP_NCE_INTERMITTENT: Stop on Intermittent NCE ETE When set, a scrubread op will stop (immediate or end of rank) when an Intermittent NCE threshold equal error is detected.. Stop immediately or at end of rank is determined with bits 0 and 1.
4	RW	MBASCTLQ_STOP_NCE_SOFT: Stop on Soft NCE ETE When set, a scrubread op will stop (immediate or end of rank) when a Soft NCE threshold equal error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
5	RW	MBASCTLQ_STOP_SCE: Stop on SCE When set, a scrubread op will stop (immediate or end of rank) when a SCE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
6	RW	MBASCTLQ_STOP_MCE: Stop on MCE When set, a scrubread op will stop (immediate or end of rank) when a MCE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
7	RW	MBASCTLQ_STOP_RETRYCE: Stop on Retry CE ETE When set, a scrubread op will stop (immediate or end of rank) when a Retry CE threshold equal error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
8	RW	MBASCTLQ_STOP_MPE: Stop on MPE When set, a scrubread op will stop (immediate or end of rank) when a Mark Place Error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
9	RW	MBASCTLQ_STOP_UE: Stop on UE When set, a scrubread op will stop (immediate or end of rank) when a SD UE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
10	RW	MBASCTLQ_STOP_ON_END_ADDRESS: Stop on End Address When set, any multi-address maintenance operation will stop when the MBMACA value equals the MBMEA (end address) value. When unset, it will continue to increment pass the end address.
11	RW	MBASCTLQ_ENABLE_ATT_MAINT_CMD_DONE: When set, the Maintenance Complete Attention is set when a maintenance operation stops (immediate or end of rank)
12	RW	MBASCTLQ_STOP_SUE: Stop on SUE When set, a scrubread op will stop (immediate or end of rank) when a SUE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
13:14	RW	MBASCTLQ_CMD_TIMEOUT_SEL: Command Timeout Select - selects the time interval for a maint command to be sent out before it times out Values: 262144_CYCLES=>0b00 1048576_CYCLES=>0b01 2097152_CYCLES=>0b10 4194304_CYCLES=>0b11
15	RW	MBASCTLQ_RESET_KEEPER: Reset Keeper Writing this bit to 1 will pulse the reset of the hold latched in the MBA c_err_rpt's
16	RW	MBASCTLQ_MBSPA_BIT_0_MODE: MBSPA Bit 0 mode When unset, MBSPA(0) is set ONLY when a maintenance command completes successfully without hitting a stop-on-error condition. When set, MBSPA(0) is set when a maintenance command stops (whether from a command complete or stop-on-error condition).
17:63	RW	MBASCTLQ_RESERVED_17_63: Reserved

Register Name	***MBA Error Control Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBECTLQ
Address	0000000003010610 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBECTLQ_ATOMIC_ALT_CE_INJ: Atomic Alter CE inject Used with the Atomic Alter Error Inject command to inject a CE error. When set, MBECTL(4:10) are used to select the symbol to be modified

Bits	SCOM	Field Mnemonic: Description
1	RW	MBECTLQ_ATOMIC_ALT_CHIP_KILL_INJ: Atomic Alter Chip Kill inject Used with the Atomic Alter Error Inject command to inject a Mark Place error (MPE), or a Mark Correct Error (MCE), is a mark is already in place for the chip kill error being injected. When set, MBECTL(4:10) are used to select the mark to be modified
2	RW	MBECTLQ_ATOMIC_ALT_SD_UE_INJ: Atomic Alter UE inject Used with the Atomic Alter Error Inject command to inject a Slow Decoder UE. When set, bits 0 thru 9 of the first data beat will be inverted to create the UE
3	RW	MBECTLQ_ATOMIC_ALT_SUE_INJ: Atomic Alter Sue inject Used with the Atomic Alter Error Inject command to inject a SUE error. Turns on SUE bit in 65th byte.

Bits	SCOM	Field Mnemonic: Description
4:10	RW	MBECTLQ_ATOMIC_ALT_INJ_SYM_SEL: Atomic alter inject symbol select has 3 modes CE inject or Chip Kill (x4 mode) or Chip Kill (x8 mode) Values: INVERT_SYMBOL_0_OR_X4_OR_X8_CHIP_0_DATA_ON_WRITE=>0b0000000 INVERT_SYMBOL_1_OR_X4_OR_X8_CHIP_1_DATA_ON_WRITE=>0b0000001 INVERT_SYMBOL_2_OR_X4_OR_X8_CHIP_2_DATA_ON_WRITE=>0b0000010 INVERT_SYMBOL_3_OR_X4_OR_X8_CHIP_3_DATA_ON_WRITE=>0b0000011 INVERT_SYMBOL_4_OR_X4_OR_X8_CHIP_4_DATA_ON_WRITE=>0b0000100 INVERT_SYMBOL_5_OR_X4_OR_X8_CHIP_5_DATA_ON_WRITE=>0b0000101 INVERT_SYMBOL_6_OR_X4_OR_X8_CHIP_6_DATA_ON_WRITE=>0b0000110 INVERT_SYMBOL_7_OR_X4_OR_X8_CHIP_7_DATA_ON_WRITE=>0b0000111 INVERT_SYMBOL_8_OR_X4_OR_X8_CHIP_8_DATA_ON_WRITE=>0b0001000 INVERT_SYMBOL_9_OR_X4_OR_X8_CHIP_9_DATA_ON_WRITE=>0b0001001 INVERT_SYMBOL_10_OR_X4_OR_X8_CHIP_10_DATA_ON_WRITE=>0b0001010 INVERT_SYMBOL_11_OR_X4_OR_X8_CHIP_11_DATA_ON_WRITE=>0b0001011 INVERT_SYMBOL_12_OR_X4_OR_X8_CHIP_12_DATA_ON_WRITE=>0b0001100 INVERT_SYMBOL_13_OR_X4_OR_X8_CHIP_13_DATA_ON_WRITE=>0b0001101 INVERT_SYMBOL_14_OR_X4_OR_X8_CHIP_14_DATA_ON_WRITE=>0b0001110 INVERT_SYMBOL_15_OR_X4_OR_X8_CHIP_15_DATA_ON_WRITE=>0b0001111 INVERT_SYMBOL_16_OR_X4_OR_X8_CHIP_16_DATA_ON_WRITE=>0b0010000 INVERT_SYMBOL_17_OR_X4_OR_X8_CHIP_17_DATA_ON_WRITE=>0b0010001 INVERT_SYMBOL_18_OR_X4_CHIP_18_DATA_ON_WRITE=>0b0010010 INVERT_SYMBOL_19_OR_X4_CHIP_19_DATA_ON_WRITE=>0b0010011 INVERT_SYMBOL_20_OR_X4_CHIP_20_DATA_ON_WRITE=>0b0010100 INVERT_SYMBOL_21_OR_X4_CHIP_21_DATA_ON_WRITE=>0b0010101 INVERT_SYMBOL_22_OR_X4_CHIP_22_DATA_ON_WRITE=>0b0010110 INVERT_SYMBOL_23_OR_X4_CHIP_23_DATA_ON_WRITE=>0b0010111 INVERT_SYMBOL_24_OR_X4_CHIP_24_DATA_ON_WRITE=>0b0011000 INVERT_SYMBOL_25_OR_X4_CHIP_25_DATA_ON_WRITE=>0b0011001 INVERT_SYMBOL_26_OR_X4_CHIP_26_DATA_ON_WRITE=>0b0011010 INVERT_SYMBOL_27_OR_X4_CHIP_27_DATA_ON_WRITE=>0b0011011 INVERT_SYMBOL_28_OR_X4_CHIP_28_DATA_ON_WRITE=>0b0011100 INVERT_SYMBOL_29_OR_X4_CHIP_29_DATA_ON_WRITE=>0b0011101 INVERT_SYMBOL_30_OR_X4_CHIP_30_DATA_ON_WRITE=>0b0011110 INVERT_SYMBOL_31_OR_X4_CHIP_31_DATA_ON_WRITE=>0b0011111 INVERT_SYMBOL_32_OR_X4_CHIP_32_DATA_ON_WRITE=>0b0100000 INVERT_SYMBOL_33_OR_X4_CHIP_33_DATA_ON_WRITE=>0b0100001 INVERT_SYMBOL_34_OR_X4_CHIP_34_DATA_ON_WRITE=>0b0100010 INVERT_SYMBOL_35_OR_X4_CHIP_35_DATA_ON_WRITE=>0b0100011 INVERT_SYMBOL_36_DATA_ON_WRITE=>0b0100100 INVERT_SYMBOL_37_DATA_ON_WRITE=>0b0100101 INVERT_SYMBOL_38_DATA_ON_WRITE=>0b0100110 INVERT_SYMBOL_39_DATA_ON_WRITE=>0b0100111 INVERT_SYMBOL_40_DATA_ON_WRITE=>0b0101000 INVERT_SYMBOL_41_DATA_ON_WRITE=>0b0101001 INVERT_SYMBOL_42_DATA_ON_WRITE=>0b0101010 INVERT_SYMBOL_43_DATA_ON_WRITE=>0b0101011 INVERT_SYMBOL_44_DATA_ON_WRITE=>0b0101100 INVERT_SYMBOL_45_DATA_ON_WRITE=>0b0101101 INVERT_SYMBOL_46_DATA_ON_WRITE=>0b0101110 INVERT_SYMBOL_47_DATA_ON_WRITE=>0b0101111 INVERT_SYMBOL_48_DATA_ON_WRITE=>0b0110000 INVERT_SYMBOL_49_DATA_ON_WRITE=>0b0110001 INVERT_SYMBOL_50_DATA_ON_WRITE=>0b0110010 INVERT_SYMBOL_51_DATA_ON_WRITE=>0b0110011 INVERT_SYMBOL_52_DATA_ON_WRITE=>0b0110100 INVERT_SYMBOL_53_DATA_ON_WRITE=>0b0110101 INVERT_SYMBOL_54_DATA_ON_WRITE=>0b0110110 INVERT_SYMBOL_55_DATA_ON_WRITE=>0b0110111 INVERT_SYMBOL_56_DATA_ON_WRITE=>0b0111000 INVERT_SYMBOL_57_DATA_ON_WRITE=>0b0111001 INVERT_SYMBOL_58_DATA_ON_WRITE=>0b0111010 INVERT_SYMBOL_59_DATA_ON_WRITE=>0b0111011 INVERT_SYMBOL_60_DATA_ON_WRITE=>0b0111100 INVERT_SYMBOL_61_DATA_ON_WRITE=>0b0111101 INVERT_SYMBOL_62_DATA_ON_WRITE=>0b0111110 INVERT_SYMBOL_63_DATA_ON_WRITE=>0b0111111

Bits	SCOM	Field Mnemonic: Description
11	RW	MBECTLQ_ATOMIC_ALT_INJ_DATA_SEL: Atomic Alter Error Inject Data Select 0 - error injected in 1st 64 bytes of data 1 - error injected in 2nd 64 bytes of data
12	RW	MBECTLQ_SCOM_CMD_REG_INJ_MODE: Parity Error inject mode into the Command SCOM (MBAFIR(5)) Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
13	RW	MBECTLQ_SCOM_CMD_REG_INJ: Parity Error inject mode into the Command SCOM (MBAFIR(5))
14	RW	MBECTLQ_SCOM_CFG_DATA_REG_INJ_MODE: Parity Error inject mode into the configuration and data SCOM (MBAFIR(6)) Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
15	RW	MBECTLQ_SCOM_CFG_DATA_REG_INJ: Parity Error inject mode into the configuration and data SCOM (MBAFIR(6))
16	RW	MBECTLQ_INTERNAL_FSM_INJ_MODE: Parity Error inject mode into the configuration and data SCOM (MBAFIR(3)) Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
17	RW	MBECTLQ_INTERNAL_REG_INJ: Parity Error inject mode into the configuration and data SCOM (MBAFIR(3))
18	RW	MBECTLQ_WRD_CAW2_UE_CE_DETECT: UE and CE detection on caw2 write data latch enable When enable, ECC will be checked at caw2 write data latches and SUE inject for any CE or UE errors detected Values: DISABLE_SUE_INJECTION_FOR_CE_AND_UE_ERRORS=>0b0 ENABLE_SUE_INJECTION_FOR_CE_AND_UE_ERRORS=>0b1
19:31	RW	MBECTLQ_RESERVED_19_31: Reserved
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBA Special Attention Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBSPAQ
Address	0000000003010611 (SCOM) 0000000003010612 (SCOM1) 0000000003010613 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBSPAQ_COMMAND_COMPLETE_WO_ENA_ERR_ATTN: maintenance command complete without enabled errors Set at the completion of a maintenance op, if the maintenance command did not stop due to a stop on error threshold or stop on maintenance memory error condition. If only non-enabled stop on threshold or error events occur during the execution of a maintenance command, the Command_Complete_Attn is set when the maintenance command completes. Maintenance stop conditions are specified in MBASCTLQ.
1	RWX	WOX_AND	WOX_OR	MBSPAQ_HARD_CE_ETE_ATTN: Hard NCE ETE Set if an error threshold condition is detected
2	RWX	WOX_AND	WOX_OR	MBSPAQ_SOFT_CE_ETE_ATTN: Soft NCE ETE Set if an error threshold condition is detected

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	MBSPAQ_INTERMITTENT_ETE_ATTN: Intermittent NCE ETE Set if an error threshold condition is detected
4	RWX	WOX_AND	WOX_OR	MBSPAQ_RCE_ETE_ATTN: Retry CE ETE Set if an error threshold condition is detected
5	RWX	WOX_AND	WOX_OR	MBSPAQ_EMERGENCY_THROTTLE_ATTN: Emergency throttle action detected Set if an emergency throttle command has been detected, power controls placed in 'safe' mode
6	RWX	WOX_AND	WOX_OR	MBSPAQ_FIRMWARE_ATTN0: Firmware generated attention0
7	RWX	WOX_AND	WOX_OR	MBSPAQ_FIRMWARE_ATTN1: Firmware generated attention1
8	RWX	WOX_AND	WOX_OR	MBSPAQ_WAT_DEBUG_ATTN: WAT Debug Bus Attention This is a way for the WAT debug bus to trigger an attention
9	RWX	WOX_AND	WOX_OR	MBSPAQ_SPARE_ATTN1: Spare1
10	RWX	WOX_AND	WOX_OR	MBSPAQ_MCBIST_DONE: MCBIST Done This bit is set when MCBIST had completed its testing.
11:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000

Register Name	***MBA Special Attention Mask Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBSPAMSKQ
Address	0000000003010614 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSPAMSKQ_COMMAND_COMPLETE_WO_ENA_ERR_ATTN: Per Bit Mask for MBSPA(0)
1	RW	MBSPAMSKQ_HARD_CE_ETE_ATTN: Per Bit Mask for MBSPA(1)
2	RW	MBSPAMSKQ_SOFT_CE_ETE_ATTN: Per Bit Mask for MBSPA(2)
3	RW	MBSPAMSKQ_INTERMITTENT_ETE_ATTN: Per Bit Mask for MBSPA(3)
4	RW	MBSPAMSKQ_RCE_ETE_ATTN: Per Bit Mask for MBSPA(4)
5	RW	MBSPAMSKQ_EMERGENCY_THROTTLE_ATTN: Per Bit Mask for MBSPA(5)
6	RW	MBSPAMSKQ_FIRMWARE_ATTN0: Per Bit Mask for MBSPA(6)
7	RW	MBSPAMSKQ_FIRMWARE_ATTN1: Per Bit Mask for MBSPA(7)
8	RW	MBSPAMSKQ_WAT_DEBUG_ATTN: Per Bit Mask for MBSPA(8)
9	RW	MBSPAMSKQ_SPARE_ATTN1: Per Bit Mask for MBSPA(9)
10	RW	MBSPAMSKQ_MCBIST_DONE: Per Bit Mask for MBSPA(10)
11:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	***CCS Instruction Array 0 0***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_0
Address	0000000003010615 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_0_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_0_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_0_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_0_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_0_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_0_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_0_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_0_MA_B_CKE: Memoy Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_0_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_0_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_0_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_0_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_0_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 1***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_1
Address	0000000003010616 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_1_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_1_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_1_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_1_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_1_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_1_MA_B_CASN: DDR CAS#

Bits	SCOM	Field Mnemonic: Description
23	RW	CCS_INST_ARR0_1_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_1_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_1_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_1_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_1_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_1_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_1_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 2***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_2
Address	0000000003010617 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_2_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_2_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_2_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_2_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_2_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_2_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_2_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_2_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_2_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_2_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_2_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_2_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_2_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 3***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_3
Address	0000000003010618 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_3_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_3_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_3_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_3_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_3_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_3_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_3_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_3_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_3_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_3_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_3_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_3_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_3_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 4*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_4
Address	0000000003010619 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_4_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_4_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_4_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_4_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_4_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_4_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_4_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_4_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_4_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_4_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_4_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_4_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_4_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 5*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_5
Address	000000000301061A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_5_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_5_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_5_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_5_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_5_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_5_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_5_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_5_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_5_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_5_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_5_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_5_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_5_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 6*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_6
Address	000000000301061B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_6_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_6_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_6_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_6_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_6_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_6_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_6_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_6_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_6_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_6_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_6_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_6_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_6_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 7***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_7
Address	000000000301061C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_7_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_7_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_7_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_7_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_7_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_7_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_7_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_7_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_7_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_7_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_7_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_7_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_7_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 8***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_8
Address	000000000301061D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_8_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_8_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_8_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_8_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_8_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_8_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_8_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_8_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_8_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_8_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_8_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_8_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_8_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 9***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_9
Address	0000000003301061E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_9_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_9_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_9_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_9_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_9_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_9_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_9_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_9_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_9_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_9_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_9_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_9_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_9_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 10***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_10
Address	000000000301061F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_10_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_10_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_10_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_10_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_10_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_10_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_10_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_10_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_10_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_10_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_10_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_10_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_10_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 11*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_11
Address	0000000003010620 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_11_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_11_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_11_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_11_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_11_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_11_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_11_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_11_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_11_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_11_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_11_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_11_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_11_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 12*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_12
Address	0000000003010621 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_12_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_12_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_12_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_12_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_12_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_12_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_12_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_12_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_12_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_12_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_12_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_12_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_12_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 13***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_13
Address	0000000003010622 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_13_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_13_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_13_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_13_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_13_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_13_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_13_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_13_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_13_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_13_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_13_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_13_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_13_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 14***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_14
Address	0000000003010623 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_14_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_14_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_14_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_14_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_14_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_14_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_14_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_14_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_14_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_14_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_14_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_14_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_14_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 15***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_15
Address	0000000003010624 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_15_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_15_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_15_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_15_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_15_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_15_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_15_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_15_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_15_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_15_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_15_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_15_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_15_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 16***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_16
Address	0000000003010625 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_16_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_16_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_16_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_16_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_16_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_16_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_16_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_16_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_16_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_16_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_16_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_16_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_16_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 17*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_17
Address	0000000003010626 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_17_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_17_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_17_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_17_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_17_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_17_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_17_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_17_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_17_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_17_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_17_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_17_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_17_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 18*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_18
Address	0000000003010627 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_18_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_18_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_18_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_18_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_18_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_18_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_18_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_18_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_18_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_18_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_18_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_18_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_18_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 19***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_19
Address	0000000003010628 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_19_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_19_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_19_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_19_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_19_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_19_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_19_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_19_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_19_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_19_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_19_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_19_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_19_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 20***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_20
Address	0000000003010629 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_20_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_20_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_20_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_20_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_20_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_20_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_20_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_20_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_20_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_20_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_20_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_20_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_20_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 21***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_21
Address	0000000003301062A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_21_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_21_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_21_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_21_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_21_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_21_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_21_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_21_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_21_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_21_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_21_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_21_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_21_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 22***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_22
Address	000000000301062B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_22_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_22_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_22_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_22_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_22_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_22_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_22_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_22_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_22_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_22_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_22_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_22_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_22_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 23*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_23
Address	000000000301062C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_23_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_23_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_23_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_23_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_23_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_23_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_23_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_23_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_23_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_23_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_23_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_23_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_23_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 24*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_24
Address	000000000301062D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_24_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_24_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_24_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_24_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_24_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_24_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_24_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_24_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_24_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_24_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_24_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_24_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_24_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 25***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_25
Address	0000000003301062E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_25_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_25_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_25_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_25_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_25_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_25_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_25_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_25_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_25_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_25_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_25_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_25_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_25_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 26***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_26
Address	0000000003301062F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_26_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_26_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_26_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_26_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_26_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_26_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_26_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_26_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_26_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_26_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_26_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_26_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_26_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 27***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_27
Address	0000000003010630 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_27_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_27_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_27_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_27_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_27_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_27_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_27_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_27_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_27_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_27_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_27_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_27_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_27_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 28***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_28
Address	0000000003010631 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_28_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_28_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_28_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_28_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_28_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_28_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_28_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_28_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_28_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_28_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_28_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_28_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_28_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 29*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_29
Address	0000000003010632 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_29_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_29_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_29_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_29_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_29_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_29_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_29_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_29_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_29_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_29_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_29_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_29_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_29_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 30*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_30
Address	0000000003010633 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_30_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_30_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_30_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_30_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_30_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_30_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_30_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_30_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_30_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_30_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_30_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_30_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_30_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 31***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR0_31
Address	0000000003010634 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_31_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_31_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_31_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_31_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_31_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_31_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_31_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_31_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_31_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_31_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_31_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calibration Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_31_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_31_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 1 0***
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_0
Address	0000000003010635 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_0_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_0_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_0_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_0_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_0_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_0_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_0_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_0_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 1*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_1
Address	0000000003010636 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_1_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_1_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_1_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_1_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_1_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_1_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_1_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_1_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 2*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_2
Address	0000000003010637 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_2_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_2_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_2_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_2_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_2_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_2_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_2_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_2_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 3*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_3
Address	0000000003010638 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_3_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_3_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_3_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_3_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_3_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_3_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_3_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_3_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 4*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_4
Address	0000000003010639 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_4_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_4_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_4_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_4_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_4_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_4_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_4_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_4_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 5*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_5
Address	000000000301063A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_5_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_5_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_5_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_5_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_5_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_5_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_5_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_5_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 6*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_6
Address	000000000301063B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_6_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_6_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_6_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_6_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_6_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_6_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_6_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_6_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 7*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_7
Address	000000000301063C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_7_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_7_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_7_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_7_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_7_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_7_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_7_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_7_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 8*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_8
Address	000000000301063D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_8_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_8_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_8_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_8_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_8_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_8_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_8_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_8_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 9*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_9
Address	000000000301063E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_9_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_9_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_9_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_9_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_9_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_9_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_9_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_9_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 10*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_10
Address	000000000301063F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_10_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_10_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_10_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_10_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_10_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_10_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_10_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_10_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 11*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_11
Address	0000000003010640 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_11_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_11_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_11_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_11_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_11_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_11_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_11_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_11_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 12*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_12
Address	0000000003010641 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_12_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_12_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_12_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_12_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_12_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_12_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_12_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_12_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 13*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_13
Address	0000000003010642 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_13_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_13_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_13_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_13_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_13_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_13_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_13_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_13_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 14*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_14
Address	0000000003010643 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_14_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_14_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_14_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_14_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_14_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_14_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_14_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_14_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 15*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_15
Address	0000000003010644 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_15_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_15_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_15_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_15_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_15_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_15_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_15_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_15_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 16*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_16
Address	0000000003010645 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_16_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_16_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_16_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_16_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_16_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_16_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_16_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_16_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 17*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_17
Address	0000000003010646 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_17_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_17_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_17_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_17_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_17_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_17_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_17_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_17_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 18*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_18
Address	0000000003010647 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_18_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_18_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_18_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_18_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_18_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_18_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_18_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_18_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 19*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_19
Address	0000000003010648 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_19_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_19_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_19_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_19_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_19_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_19_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_19_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_19_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 20*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_20
Address	0000000003010649 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_20_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_20_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_20_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_20_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_20_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_20_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_20_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_20_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 21*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_21
Address	000000000301064A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_21_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_21_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_21_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_21_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_21_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_21_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_21_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_21_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 22*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_22
Address	000000000301064B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_22_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_22_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_22_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_22_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_22_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_22_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_22_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_22_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 23*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_23
Address	000000000301064C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_23_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_23_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_23_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_23_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_23_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_23_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_23_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_23_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 24*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_24
Address	000000000301064D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_24_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_24_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_24_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_24_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_24_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_24_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_24_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_24_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 25*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_25
Address	000000000301064E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_25_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_25_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_25_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_25_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_25_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_25_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_25_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_25_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 26*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_26
Address	000000000301064F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_26_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_26_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_26_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_26_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_26_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_26_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_26_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_26_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 27*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_27
Address	0000000003010650 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_27_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_27_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_27_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_27_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_27_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_27_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_27_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_27_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 28*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_28
Address	0000000003010651 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_28_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_28_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_28_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_28_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_28_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_28_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_28_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_28_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 29*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_29
Address	0000000003010652 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_29_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_29_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_29_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_29_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_29_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_29_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_29_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_29_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 30*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_30
Address	0000000003010653 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_30_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_30_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_30_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_30_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_30_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_30_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_30_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_30_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 31*
Mnemonic	MBU.MBA01.MBA_MCBIST.CCS.CCS_INST_ARR1_31
Address	0000000003010654 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_31_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_31_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_31_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_31_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_31_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_31_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_31_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_31_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*Configured Command Sequence Control Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.CCS_CNTLQ
Address	00000000030106A5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	CCS_CNTLQ_CCS_START: Start bit - Self resetting bit. Kicks off the CCS operation
1	RWX	CCS_CNTLQ_CCS_STOP: Stop bit - Self resetting bit. Stops Current CCS operation
2:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Configured Command Sequence Status Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.CCS_STATQ
Address	00000000030106A6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	CCS_STATQ_CCS_IP: IP bit - Hdw sets to a '1'b when CCS run in progress
1	RWX	CCS_STATQ_CCS_DONE: Done bit - Hdw sets to a '1'b when CCS run complete
2	RWX	CCS_STATQ_CCS_FAIL: Fail bit - Hdw sets to a '1'b when CCS run failed
3:5	RWX	CCS_STATQ_CCS_FAIL_TYPE: Fail Type - Indicates type of CCS failure: Bit 3-> Read Miscompare Bit 4 -> UE or SUE Error Bit 5 -> Calibration operation times out

Bits	SCOM	Field Mnemonic: Description
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Configured Command Sequence Mode Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.CCS_MODEQ
Address	00000000030106A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	CCS_MODEQ_CCS_STOP_ON_ERR: User sets to a '1'b to tell the Hdw to stop CCS whenever failure occurs. When a '0'b, Hdw will continue CCS even if a failure occurs.
1	RW	CCS_MODEQ_CCS_UE_DISABLE: User sets to a '1'b to force the Hdw to ignore any array ue or sue errors during CCS command fetching.
2:3	RW	CCS_MODEQ_CCS_DATA_SEL: User sets to indicate which group of the data burst to compare. Values: DDR_BURST_1_AND_2=>0b00 DDR_BURST_3_AND_4=>0b01 DDR_BURST_5_AND_6=>0b10 DDR_BURST_7_AND_8=>0b11
4:5	RW	CCS_MODEQ_MCBIST_DDR_DPHY_NCLK: DDR Phy nclk control Values: PHY_NCLK_OUTPUT_DISABLED=>0b00 PHY_NCLK_OUTPUT_ENABLED=>0b01
6:7	RW	CCS_MODEQ_MCBIST_DDR_DPHY_PCLK: DDR Phy pclk control Values: PHY_PCLK_OUTPUT_DISABLED=>0b00 PHY_PCLK_OUTPUT_ENABLED=>0b10
8:23	RW	CCS_MODEQ_DDR_CAL_TIMEOUT_CNT: DDR calibration time counter - amount of time to wait for DDR calibration to complete. This value is multiplied by the factor in bits 30:31 to get the total timeout wait time.
24	RW	CCS_MODEQ_MCBIST_DDR_RESETN: DDR Resetn Signal
25	RW	CCS_MODEQ_MCBIST_DDR_DFI_RESET_RECOVER: DDR Reset Recover Signal
26	RW	CCS_MODEQ_COPY_CKE_TO_SPARE_CKE: Copy CKE signals to CKE Spare on both ports 0 - Spare CKEs not copied with values from CKE(0:1) and CKE(4:5) 1 - Port A CKE(0:1) copied to Port A CKE(2:3), Port A CKE(4:5) copied to Port A CKE(6:7), Port B CKE(0:1) copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7)
27	RW	CCS_MODEQ_DISABLE_ECC_ARRAY_CHK: Disable ecc checking on the CCS arrays 0 - ECC checking on 1 - ECC checking off
28	RW	CCS_MODEQ_DISABLE_ECC_ARRAY_CORRECTION: Disable ecc correction on the CCS arrays 0 - ECC correction on 1 - ECC correction off
29	RW	CCS_MODEQ_CCS_ADDR_MUX_SEL: CCS Address Mux Sel - This bit should be turned on until all multiple CCS instructions are completed. 0 - selects address data from mainline logic 1 - selects address data from CCS logic
30:31	RW	CCS_MODEQ_DDR_CAL_TIMEOUT_CNT_MULT: DDR calibration time counter multiplication factor. This value is multiplied by the counter in bits 8:23 to get the total timeout wait time. Values: 1_CCS_CYCLE=>0b00 512_CCS_CYCLES=>0b01 32768_CCS_CYCLES=>0b10 1073741824_CCS_CYCLES=>0b11
32:47	RW	CCS_MODEQ_MA_B_ADDRESS_IDLE_PAT: DDR Row and Column Address Idle Pattern (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
48:50	RW	CCS_MODEQ_MA_B_BANK_IDLE_PAT: DDR Bank Address Idle Pattern For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
51	RW	CCS_MODEQ_MA_B_ACTIVATE_IDLE_PAT: DDR4 Activate Idle Pattern
52	RW	CCS_MODEQ_MA_B_RASN_IDLE_PAT: DDR RAS# Idle Pattern
53	RW	CCS_MODEQ_MA_B_CASN_IDLE_PAT: DDR CAS# Idle Pattern
54	RW	CCS_MODEQ_MA_B_WEN_IDLE_PAT: DDR Write Enable (WE#) Idle Pattern
55	RW	CCS_MODEQ_NTTM_MODE: Non Traditional Transparent Mode When set to 1, limited non-traditional read and write operations can be done.
56:59	RW	CCS_MODEQ_NTTM_RW_DATA_DLY: Non Traditional Transparent ReadWrite Delay Use to delay the Write data start pulse or Read Data capture pulse to the DDR Phys. Maximum delay of 15 cycles is possible.
60	RW	CCS_MODEQ_DDR_RESETN_ENABLE: DDR Resetn Enabled When set to 1, bit 16 of the CCS_INST_ARR0 will be driven out to DDR Resetn. When set to 0, ccs_modeq(24) will be driven out to DDR Resetn.
61	RW	CCS_MODEQ_DDR_PARITY_ENABLE: DDR Parity Enabled When set to 1, bit 60 of the CCS_INST_ARR0 will be driven out to DDR parity. When set to 0, the hardware calculates the parity.
62	RW	CCS_MODEQ_GP_BIT_3_ENABLE: GP bit 3 enable (force_mclk_low) When set to 1, the inverted value of GP(3) will be driven on the force_mclk_low signal to the DDR PHYs. When set to 0, the value of inverted value of ccs_modeq(63) will be driven on the force_mclk_low signal to the DDR PHYs
63	RW	CCS_MODEQ_FORCE_MCLK_LOW_N: force_mclk_low_n When set to 0, a '1' will be driven on the force_mclk_low signal to the DDR PHYs. When set to 1, the inverted value of ccs_modeq(63) will be driven on the force_mclk_low signal to the DDR PHYs

Register Name	***MCBIST Memory Register 0***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR0Q
Address	00000000030106A8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST00_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST00_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST00_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST00_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand

Bits	SCOM	Field Mnemonic: Description
6:7	RW	MCBIST_CFG_TEST00_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST00_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST00_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST00_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST00_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
16:18	RW	MCBIST_CFG_TEST01_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST01_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST01_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST01_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST01_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11

Bits	SCOM	Field Mnemonic: Description
24:26	RW	MCBIST_CFG_TEST01_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST01_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST01_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST01_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
32:34	RW	MCBIST_CFG_TEST02_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST02_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST02_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST02_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST02_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST02_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111

Bits	SCOM	Field Mnemonic: Description
43	RW	MCBIST_CFG_TEST02_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST02_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST02_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
48:50	RW	MCBIST_CFG_TEST03_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST03_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST03_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST03_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST03_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST03_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST03_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST03_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11

Bits	SCOM	Field Mnemonic: Description
62:63	RW	MCBIST_CFG_TEST03_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 1***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR1Q
Address	00000000030106A9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST04_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST04_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST04_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST04_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST04_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST04_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST04_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1

Bits	SCOM	Field Mnemonic: Description
12:13	RW	MCBIST_CFG_TEST04_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST04_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
16:18	RW	MCBIST_CFG_TEST05_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST05_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST05_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST05_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST05_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST05_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST05_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST05_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11

Bits	SCOM	Field Mnemonic: Description
30:31	RW	MCBIST_CFG_TEST05_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
32:34	RW	MCBIST_CFG_TEST06_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST06_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST06_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST06_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST06_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST06_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST06_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST06_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST06_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST07_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST07_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST07_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST07_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST07_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST07_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST07_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST07_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST07_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 2***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR2Q
Address	00000000030106AA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST08_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST08_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST08_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST08_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST08_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST08_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST08_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST08_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST08_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST09_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST09_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST09_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST09_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST09_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST09_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST09_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST09_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST09_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST10_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST10_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST10_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST10_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST10_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST10_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST10_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST10_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST10_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST11_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST11_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST11_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST11_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST11_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST11_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST11_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST11_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST11_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 3***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR3Q
Address	00000000030106AB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST12_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST12_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST12_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST12_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST12_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST12_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST12_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST12_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST12_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST13_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST13_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST13_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST13_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST13_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST13_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST13_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST13_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST13_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST14_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST14_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST14_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST14_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST14_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST14_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST14_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST14_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST14_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST15_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST15_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST15_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST15_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST15_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST15_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST15_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST15_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST15_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 4***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR4Q
Address	00000000030106AC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST16_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST16_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST16_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST16_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST16_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST16_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST16_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST16_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST16_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST17_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST17_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST17_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST17_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST17_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST17_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST17_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST17_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST17_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST18_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST18_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST18_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST18_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST18_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST18_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST18_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST18_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST18_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST19_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST19_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST19_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST19_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST19_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST19_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST19_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST19_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST19_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 5***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR5Q
Address	00000000030106AD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST20_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST20_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST20_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST20_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST20_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST20_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST20_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST20_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST20_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST21_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST21_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST21_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST21_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST21_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST21_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST21_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST21_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST21_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST22_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST22_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST22_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST22_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST22_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST22_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST22_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST22_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST22_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST23_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST23_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST23_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST23_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST23_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST23_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST23_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST23_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST23_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 6***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR6Q
Address	00000000030106AE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST24_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST24_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST24_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST24_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST24_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST24_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST24_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST24_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST24_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST25_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST25_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST25_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST25_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST25_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST25_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST25_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST25_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST25_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST26_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST26_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST26_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST26_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST26_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST26_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST26_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST26_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST26_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST27_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST27_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST27_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST27_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST27_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST27_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST27_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST27_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST27_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Parameter Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBPARMQ
Address	00000000030106AF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RW	MCBPARMQ_RESERVED_0_49: Not used
50:52	RW	MCBPARMQ_CFG_RANDCMD_WGT: Specifies the weighting of random commands as follows (%Read %Write): Values: 12_87=>0b000 25_75=>0b001 50_50=>0b010 75_25=>0b011 87_12=>0b100
53:59	RW	MCBPARMQ_CFG_MIN_CMD_GAP: This is the minimum number of cycles between commands when cfg_en_randcmd_gap is a 0. If cfg_en_randcmd_gap is a 1 this becomes a 7 bit seed for the LFSR that randomly generates the gap intervals between 1-127. A value of all zeros will force MCBIST to issues commands as fast as possible.
60	RW	MCBPARMQ_CFG_EN_RANDCMD_GAP: When set to a 1 random command gaps from 1-1023 cycles are enabled and cfg_min_cmd_gap is disabled and becomes a seed for a LFSR that is randomly generating 1-127 cycle gaps (there is another 8 bit LFSR that is generating a 1-8 cycle multiplier).
61:62	RW	MCBPARMQ_CFG_RANDGAP_WGT: Forces the following command gap intervals when cfg_en_randcmd_gap is a 1: 00: 1 to 1023 cycles. 01: 1 to 511 cycles. 10: 1 to 255 cycles. 11: 1 to 127 cycles.
63	RW	MCBPARMQ_CFG_BC4_EN: BC4 enable When set, it enables BC4 data mode. This configuration cannot be use in ECC data mode.

Register Name	***MCBIST Runtime Counter Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.RUNTIMECTRQ
Address	00000000030106B0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	RUNTIMECTRQ_CFG_RUNTIME_CTR: This is the runtime counter facility. This 37 bit counter will increment every 4 memory clock cycles which gives it a maximum value of 687 seconds at 800 MHz or 824 seconds at 667 MHz.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	***MCBIST Refresh Control Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRCRQ
Address	00000000030106B1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RW	MCBRCRQ_RESERVED_0_31: Not used
32	RW	MCBRCRQ_CFG_RUNTIME_MCBALL: Configures what the runtime counter counts: Values: JUST_ONE_SUBTEST=>0b0 FULL_MCBIST_RUN=>0b1
33:37	RW	MCBRCRQ_CFG_RUNTIME_SUBTEST: If bit 32 is a 0, these bits represent the subtest number that should be counted.

Bits	SCOM	Field Mnemonic: Description
38	RW	MCBRCRQ_CFG_RUNTIME_OVERHEAD: If bit 32 is a 1, this bit configures the starting point of the runtime counter: Values: WITHOUT_OVERHEAD_WAIT_UNTIL_SUBTEST_0_IS_STARTED=>0b0 WITH_OVERHEAD_AS_SOON_AS_MCBIST_LEAVES_THE_IDLE_STATE=>0b1
39	RW	MCBRCRQ_RESERVED_39: Not used
40:63	RO	constant=0b00000000000000000000000

Register Name	***Random Data Seed 0 Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS0Q
Address	00000000030106B2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS0Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS0Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS0Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS0Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS0Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS0Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS0Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS0Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***Random Data Seed 1 Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS1Q
Address	00000000030106B3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS1Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS1Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS1Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS1Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS1Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS1Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS1Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS1Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 2 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS2Q
Address	00000000030106B4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS2Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS2Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS2Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS2Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS2Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS2Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS2Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS2Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 3 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS3Q
Address	00000000030106B5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS3Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS3Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS3Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS3Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS3Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS3Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS3Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS3Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 4 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS4Q
Address	00000000030106B6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS4Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS4Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MCBRDS4Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS4Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS4Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS4Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS4Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS4Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***Random Data Seed 5 Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS5Q
Address	00000000030106B7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS5Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS5Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS5Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS5Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS5Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS5Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS5Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS5Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***Random Data Seed 6 Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS6Q
Address	00000000030106B8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS6Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS6Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS6Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS6Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS6Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS6Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS6Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS6Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 7 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS7Q
Address	00000000030106B9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS7Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS7Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS7Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS7Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS7Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS7Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS7Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS7Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 8 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDS8Q
Address	00000000030106BA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS8Q_DGEN_RNDD_SEED0: DQ(8) Burst 1 Random Data Seed
8:15	RW	MCBRDS8Q_DGEN_RNDD_SEED1: DQ(8) Burst 2 Random Data Seed
16:23	RW	MCBRDS8Q_DGEN_RNDD_SEED2: DQ(8) Burst 3 Random Data Seed
24:31	RW	MCBRDS8Q_DGEN_RNDD_SEED3: DQ(8) Burst 4 Random Data Seed
32:39	RW	MCBRDS8Q_DGEN_RNDD_SEED4: DQ(8) Burst 5 Random Data Seed
40:47	RW	MCBRDS8Q_DGEN_RNDD_SEED5: DQ(8) Burst 6 Random Data Seed
48:55	RW	MCBRDS8Q_DGEN_RNDD_SEED6: DQ(8) Burst 7 Random Data Seed
56:63	RW	MCBRDS8Q_DGEN_RNDD_SEED7: DQ(8) Burst 8 Random Data Seed

Register Name	*Random Data Seed Spare Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRDSSPQ
Address	00000000030106BB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDSSPQ_DGEN_RNDD_SEED0: DQ(9) Burst 1 Random Data Seed
8:15	RW	MCBRDSSPQ_DGEN_RNDD_SEED1: DQ(9) Burst 2 Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MCBRDSSPQ_DGEN_RNDD_SEED2: DQ(9) Burst 3 Random Data Seed
24:31	RW	MCBRDSSPQ_DGEN_RNDD_SEED3: DQ(9) Burst 4 Random Data Seed
32:39	RW	MCBRDSSPQ_DGEN_RNDD_SEED4: DQ(9) Burst 5 Random Data Seed
40:47	RW	MCBRDSSPQ_DGEN_RNDD_SEED5: DQ(9) Burst 6 Random Data Seed
48:55	RW	MCBRDSSPQ_DGEN_RNDD_SEED6: DQ(9) Burst 7 Random Data Seed
56:63	RW	MCBRDSSPQ_DGEN_RNDD_SEED7: DQ(9) Burst 8 Random Data Seed

Register Name	***Data Rotate Seed Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBDRSRQ
Address	00000000030106BC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBDRSRQ_CFG_DATA_ROT_SEED: Bits 0:63 of the Data Rotate Seed

Register Name	***Data Rotate Configuration Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBDRCRQ
Address	00000000030106BD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBDRCRQ_CFG_DATA_ROT: Bits to shift: Values: ROTATE_1_BIT=>0b0001 ROTATE_2_BITS=>0b0010 ROTATE_3_BITS=>0b0011 ROTATE_4_BITS=>0b0100 ROTATE_5_BITS=>0b0101 ROTATE_6_BITS=>0b0110 ROTATE_7_BITS=>0b0111 ROTATE_8_BITS=>0b1000 ROTATE_9_BITS=>0b1001 ROTATE_10_BITS=>0b1010 ROTATE_11_BITS=>0b1011 ROTATE_12_BITS=>0b1100 ROTATE_13_BITS=>0b1101 ROTATE_14_BITS=>0b1110 ROTATE_15_BITS=>0b1111
4:19	RW	MCBDRCRQ_CFG_DATA_ROT_SEED: Bits 64:79 of the Data Rotate Seed
20	RW	MCBDRCRQ_CFG_INVERT_DATA: These bits control the final inversion of data over to the write data flow. Bit 20 = Invert MA Data
21:63	RW	MCBDRCRQ_RESERVED_21_63: Not used

Register Name	*Fixed Data Seed Burst 0 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD0Q
Address	00000000030106BE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD0Q_CFG_FIXED_SEED: Fixed Data Seed(0:63)

Register Name	*Fixed Data Seed Burst 1 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD1Q
Address	00000000030106BF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD1Q_CFG_FIXED_SEED: Fixed Data Seed(72:135)

Register Name	*Fixed Data Seed Burst 2 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD2Q
Address	00000000030106C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD2Q_CFG_FIXED_SEED: Fixed Data Seed(144:207)

Register Name	*Fixed Data Seed Burst 3 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD3Q
Address	00000000030106C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD3Q_CFG_FIXED_SEED: Fixed Data Seed(216:279)

Register Name	*Fixed Data Seed Burst 4 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD4Q
Address	00000000030106C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD4Q_CFG_FIXED_SEED: Fixed Data Seed(288:351)

Register Name	*Fixed Data Seed Burst 5 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD5Q
Address	00000000030106C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD5Q_CFG_FIXED_SEED: Fixed Data Seed(360:423)

Register Name	*Fixed Data Seed Burst 6 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD6Q
Address	00000000030106C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD6Q_CFG_FIXED_SEED: Fixed Data Seed(432:495)

Register Name	*Fixed Data Seed Burst 7 Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFD7Q
Address	00000000030106C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD7Q_CFG_FIXED_SEED: Fixed Data Seed(504:567)

Register Name	*Fixed Data Seed Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFDQ
Address	00000000030106C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBFDQ_CFG_FIXED_SEED1: DQ(8) Burst 1 Fixed Data Seed(64:71)
8:15	RW	MCBFDQ_CFG_FIXED_SEED2: DQ(8) Burst 2 Fixed Data Seed(136:143)
16:23	RW	MCBFDQ_CFG_FIXED_SEED3: DQ(8) Burst 3 Fixed Data Seed(208:215)
24:31	RW	MCBFDQ_CFG_FIXED_SEED4: DQ(8) Burst 4 Fixed Data Seed(280:287)
32:39	RW	MCBFDQ_CFG_FIXED_SEED5: DQ(8) Burst 5 Fixed Data Seed(352:359)
40:47	RW	MCBFDQ_CFG_FIXED_SEED6: DQ(8) Burst 6 Fixed Data Seed(424:431)
48:55	RW	MCBFDQ_CFG_FIXED_SEED7: DQ(8) Burst 7 Fixed Data Seed(496:503)
56:63	RW	MCBFDQ_CFG_FIXED_SEED8: DQ(8) Burst 8 Fixed Data Seed(568:575)

Register Name	*Fixed Data Seed Spare Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBFDSPQ
Address	00000000030106C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBFDSPQ_CFG_FIXED_SEED1: DQ(9) Burst 1 Fixed Data Seed(576:583)
8:15	RW	MCBFDSPQ_CFG_FIXED_SEED2: DQ(9) Burst 2 Fixed Data Seed(584:591)
16:23	RW	MCBFDSPQ_CFG_FIXED_SEED3: DQ(9) Burst 3 Fixed Data Seed(592:599)
24:31	RW	MCBFDSPQ_CFG_FIXED_SEED4: DQ(9) Burst 4 Fixed Data Seed(600:607)
32:39	RW	MCBFDSPQ_CFG_FIXED_SEED5: DQ(9) Burst 5 Fixed Data Seed(608:615)
40:47	RW	MCBFDSPQ_CFG_FIXED_SEED6: DQ(9) Burst 6 Fixed Data Seed(616:623)
48:55	RW	MCBFDSPQ_CFG_FIXED_SEED7: DQ(9) Burst 7 Fixed Data Seed(624:631)
56:63	RW	MCBFDSPQ_CFG_FIXED_SEED8: DQ(9) Burst 8 Fixed Data Seed(632:639)

Register Name	*Port A Socket 0 Address Map Register 0*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR0A0Q
Address	00000000030106C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK0: Master Rank Bit 0 (MSB)
6:11	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK1: Master Rank Bit 1

Bits	SCOM	Field Mnemonic: Description
12:17	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK2: Master Rank Rank Bit 2
18:23	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK3: Master Rank Rank Bit 3
24:29	RW	MCBAMR0A0Q_CFG_A0MAP_SRANK0: Slave Rank Bit 0 (MSB)
30:35	RW	MCBAMR0A0Q_CFG_A0MAP_SRANK1: Slave Rank Bit 1
36:41	RW	MCBAMR0A0Q_CFG_A0MAP_SRANK2: Slave Rank Rank Bit 2
42:47	RW	MCBAMR0A0Q_CFG_A0MAP_BANK3: DRAM Bank Address Bit 3 (MSB)
48:53	RW	MCBAMR0A0Q_CFG_A0MAP_BANK2: DRAM Bank Address Bit 2 (MSB)
54:59	RW	MCBAMR0A0Q_CFG_A0MAP_BANK1: DRAM Bank Address Bit 1
60:63	RW	MCBAMR0A0Q_RESERVED_60_63: Reserved

Register Name	***Port A Socket 0 Address Map Register 1***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR1A0Q
Address	00000000030106C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A0Q_CFG_A0MAP_BANK0: DRAM Bank Address Bit 0
6:11	RW	MCBAMR1A0Q_CFG_A0MAP_ROW16: DRAM Row Address Bit16 (MSB)
12:17	RW	MCBAMR1A0Q_CFG_A0MAP_ROW15: DRAM Row Address Bit15
18:23	RW	MCBAMR1A0Q_CFG_A0MAP_ROW14: DRAM Row Address Bit 14
24:29	RW	MCBAMR1A0Q_CFG_A0MAP_ROW13: DRAM Row Address Bit 13
30:35	RW	MCBAMR1A0Q_CFG_A0MAP_ROW12: DRAM Row Address Bit 12
36:41	RW	MCBAMR1A0Q_CFG_A0MAP_ROW11: DRAM Row Address Bit 11
42:47	RW	MCBAMR1A0Q_CFG_A0MAP_ROW10: DRAM Row Address Bit 10
48:53	RW	MCBAMR1A0Q_CFG_A0MAP_ROW9: DRAM Row Address Bit 9
54:59	RW	MCBAMR1A0Q_CFG_A0MAP_ROW8: DRAM Row Address Bit 8
60:63	RW	MCBAMR1A0Q_RESERVED_60_63: Not used

Register Name	***Port A Socket 0 Address Map Register 2***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR2A0Q
Address	00000000030106CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A0Q_CFG_A0MAP_ROW7: DRAM Row Address Bit 7
6:11	RW	MCBAMR2A0Q_CFG_A0MAP_ROW6: DRAM Row Address Bit 6
12:17	RW	MCBAMR2A0Q_CFG_A0MAP_ROW5: DRAM Row Address Bit 5
18:23	RW	MCBAMR2A0Q_CFG_A0MAP_ROW4: DRAM Row Address Bit 4

Bits	SCOM	Field Mnemonic: Description
24:29	RW	MCBAMR2A0Q_CFG_A0MAP_ROW3: DRAM Row Address Bit 3
30:35	RW	MCBAMR2A0Q_CFG_A0MAP_ROW2: DRAM Row Address Bit 2
36:41	RW	MCBAMR2A0Q_CFG_A0MAP_ROW1: DRAM Row Address Bit 1
42:47	RW	MCBAMR2A0Q_CFG_A0MAP_ROW0: DRAM Row Address Bit 0
48:53	RW	MCBAMR2A0Q_CFG_A0MAP_COL13: DRAM Column Address Bit 13 (MSB)
54:59	RW	MCBAMR2A0Q_CFG_A0MAP_COL11: DRAM Column Address Bit 11
60:63	RW	MCBAMR2A0Q_RESERVED_60_63: Not used

Register Name	***Port A Socket 0 Address Map Register 3***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR3A0Q
Address	00000000030106CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A0Q_CFG_A0MAP_COL9: DRAM Column Address Bit 9
6:11	RW	MCBAMR3A0Q_CFG_A0MAP_COL8: DRAM Column Address Bit 8
12:17	RW	MCBAMR3A0Q_CFG_A0MAP_COL7: DRAM Column Address Bit 7
18:23	RW	MCBAMR3A0Q_CFG_A0MAP_COL6: DRAM Column Address Bit 6
24:29	RW	MCBAMR3A0Q_CFG_A0MAP_COL5: DRAM Column Address Bit 5
30:35	RW	MCBAMR3A0Q_CFG_A0MAP_COL4: DRAM Column Address Bit 4
36:41	RW	MCBAMR3A0Q_CFG_A0MAP_COL3: DRAM Column Address Bit 3
42:47	RW	MCBAMR3A0Q_CFG_A0MAP_COL2: DRAM Column Address Bit 2 - Map to an Unused Address bit if NOT fixed BL= 4
48:63	RW	MCBAMR3A0Q_RESERVED_48_63: Not Used

Register Name	***Port A0 Random Start Address Configuration Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRSARA0Q
Address	00000000030106CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBRSARA0Q_CFG_RAND_START_ADDR_A0: Socket A0 Starting Address when addressing is random forward Ending Address when addressing is random reverse
38:63	RW	MCBRSARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Random Start Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBRSARA1Q
Address	00000000030106CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBRSARA1Q_CFG_RAND_START_ADDR_A1: Socket A1 Starting Address when addressing is random forward Ending Address when addressing is random reverse
38:63	RW	MCBRSARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Random End Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBREARA0Q
Address	00000000030106CE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBREARA0Q_CFG_RAND_END_ADDR_A0: Socket A0 Ending Address when addressing is random forward Starting Address when addressing is random reverse
38:63	RW	MCBREARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Random End Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBREARA1Q
Address	00000000030106CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBREARA1Q_CFG_RAND_END_ADDR_A1: Socket A1 Ending Address when addressing is random forward Starting Address when addressing is random reverse
38:63	RW	MCBREARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Sequential Start Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBSSARA0Q
Address	00000000030106D0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSSARA0Q_CFG_SEQ_START_ADDR_A0: Socket A0 Starting Address when addressing is sequential forward Ending Address when addressing is sequential reverse
38:63	RW	MCBSSARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Sequential Start Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBSSARA1Q
Address	00000000030106D1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSSARA1Q_CFG_SEQ_START_ADDR_A1: Socket A1 Starting Address when addressing is sequential forward Ending Address when addressing is sequential reverse
38:63	RW	MCBSSARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Sequential End Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBSEARA0Q
Address	00000000030106D2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSEARA0Q_CFG_SEQ_END_ADDR_A0: Socket A0 Ending Address when addressing is sequential forward Starting Address when addressing is sequential reverse
38:63	RW	MCBSEARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Sequential End Address Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBSEARA1Q
Address	00000000030106D3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSEARA1Q_CFG_SEQ_END_ADDR_A1: Socket A1 Ending Address when addressing is sequential forward Starting Address when addressing is sequential reverse
38:63	RW	MCBSEARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Address LFSR Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBLFSRA0Q
Address	00000000030106D4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBLFSRA0Q_CFG_LFSR_MASK_A0: Socket A0 Default configuration is for a 25 bit LFSR MASK Master Rank 0:3, Slave Rank 0:2, Bank(3:0), Row(16:15) fixed Row(14:0), Col(13,11,9:2) variable

Bits	SCOM	Field Mnemonic: Description
38:63	RW	MCBLFSRA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Address LFSR Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBLFSRA1Q
Address	00000000030106D5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBLFSRA1Q_CFG_LFSR_MASK_A1: Socket A1 Default configuration is for a 25 bit LFSR MASK Master Rank 0:3, Slave Rank 0:2, Bank(3:0), Row(16:15) fixed Row(14:0), Col(13,11,9:2) variable
38:63	RW	MCBLFSRA1Q_RESERVED_38_63: Not Used

Register Name	*Port A Address Generator Configuration Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAGRAQ
Address	00000000030106D6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAGRAQ_CFG_FIXED_WIDTH_A0: Sets the number of fixed slots in the address generator for Port A, socket A0. This will cause the bits from (MSB to MSB+cfg_fixed_width_a0-1) to not be included in the address generation. Used in conjunction with the configurable address map registers. Example: Fixed Rank, Fixed Bank, Fixed Row = 3 + 3 + 16 = 22 Program 0x16 Defaulted to a fixed Rank setting - Don needs to check this
6:11	RW	MCBAGRAQ_CFG_FIXED_WIDTH_A1: Sets the number of fixed slots in the address generator for Port A, socket A1. This will cause the bits from (MSB to MSB+cfg_fixed_width_a1-1) to not be included in the address generation. Used in conjunction with the configurable address map registers. Example: Fixed Rank, Fixed Bank, Fixed Row = 3 + 3 + 16 = 22 Program 0x16 Defaulted to a fixed Rank setting - Don needs to check this
12:15	RW	MCBAGRAQ_CFG_PORTA0_RATIO: Programs how often Port A, socket A0 addresses need to be generated relative to Port A, socket A1 addresses. Ratios can be set anywhere from [1-15] : [1-15]. Used for Deterministic address weighting.
16:19	RW	MCBAGRAQ_CFG_PORTA1_RATIO: Programs how often Port A, socket A1 addresses need to be generated relative to Port A, socket A0 addresses. Ratios can be set anywhere from [1-15] : [1-15]. Used for Deterministic address weighting.
20:22	RW	MCBAGRAQ_CFG_RANDPORT_WGT_A: Specify the weighting of A0A1 port accesses. A B 000 - 12.5 87.5 001 - 25 75 010 - 50 50 011 - 75 25 100 - 87.5 12.5
23	RW	MCBAGRAQ_CFG_DET_RAND_WGT_A: 0 - Use deterministic ratio to switch between socket A0 and socket A1 1 - Use random weighted ratio to switch between socket A0 and socket A1
24:25	RW	MCBAGRAQ_CFG_PORTA_SCKT_PPLTD: Socket Populated Values: SOCKET_A0_AND_SOCKET_A1_ARE_NOT_POPULATED=>0b00 ONLY_SOCKET_A1_IS_POPULATED=>0b01 ONLY_SOCKET_A0_IS_POPULATED=>0b10 SOCKET_A0_AND_SOCKET_A1_ARE_BOTH_POPULATED=>0b11
26:31	RW	MCBAGRAQ_RESERVED_26_31: Not used
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	*Port A Socket 1 Address Map Register 0*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR0A1Q
Address	00000000030106D7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK0: Master Rank Bit 0 (MSB)
6:11	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK1: Master Rank Bit 1
12:17	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK2: Master Rank Rank Bit 2
18:23	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK3: Master Rank Rank Bit 3
24:29	RW	MCBAMR0A1Q_CFG_A1MAP_SRANK0: Slave Rank Bit 0 (MSB)
30:35	RW	MCBAMR0A1Q_CFG_A1MAP_SRANK1: Slave Rank Bit 1
36:41	RW	MCBAMR0A1Q_CFG_A1MAP_SRANK2: Slave Rank Rank Bit 2
42:47	RW	MCBAMR0A1Q_CFG_A1MAP_BANK3: DRAM Bank Address Bit 3 (MSB)
48:53	RW	MCBAMR0A1Q_CFG_A1MAP_BANK2: DRAM Bank Address Bit 2 (MSB)
54:59	RW	MCBAMR0A1Q_CFG_A1MAP_BANK1: DRAM Bank Address Bit 1
60:63	RW	MCBAMR0A1Q_RESERVED_60_63: Reserved

Register Name	*Port A Socket 1 Address Map Register 1*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR1A1Q
Address	00000000030106D8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A1Q_CFG_A1MAP_BANK0: DRAM Bank Address Bit 0
6:11	RW	MCBAMR1A1Q_CFG_A1MAP_ROW16: DRAM Row Address Bit16 (MSB)
12:17	RW	MCBAMR1A1Q_CFG_A1MAP_ROW15: DRAM Row Address Bit15
18:23	RW	MCBAMR1A1Q_CFG_A1MAP_ROW14: DRAM Row Address Bit 14
24:29	RW	MCBAMR1A1Q_CFG_A1MAP_ROW13: DRAM Row Address Bit 13
30:35	RW	MCBAMR1A1Q_CFG_A1MAP_ROW12: DRAM Row Address Bit 12
36:41	RW	MCBAMR1A1Q_CFG_A1MAP_ROW11: DRAM Row Address Bit 11
42:47	RW	MCBAMR1A1Q_CFG_A1MAP_ROW10: DRAM Row Address Bit 10
48:53	RW	MCBAMR1A1Q_CFG_A1MAP_ROW9: DRAM Row Address Bit 9
54:59	RW	MCBAMR1A1Q_CFG_A1MAP_ROW8: DRAM Row Address Bit 8
60:63	RW	MCBAMR1A1Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 1 Address Map Register 2*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR2A1Q
Address	00000000030106D9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A1Q_CFG_A1MAP_ROW7: DRAM Row Address Bit 7
6:11	RW	MCBAMR2A1Q_CFG_A1MAP_ROW6: DRAM Row Address Bit 6
12:17	RW	MCBAMR2A1Q_CFG_A1MAP_ROW5: DRAM Row Address Bit 5
18:23	RW	MCBAMR2A1Q_CFG_A1MAP_ROW4: DRAM Row Address Bit 4
24:29	RW	MCBAMR2A1Q_CFG_A1MAP_ROW3: DRAM Row Address Bit 3
30:35	RW	MCBAMR2A1Q_CFG_A1MAP_ROW2: DRAM Row Address Bit 2
36:41	RW	MCBAMR2A1Q_CFG_A1MAP_ROW1: DRAM Row Address Bit 1
42:47	RW	MCBAMR2A1Q_CFG_A1MAP_ROW0: DRAM Row Address Bit 0
48:53	RW	MCBAMR2A1Q_CFG_A1MAP_COL13: DRAM Column Address Bit 13 (MSB)
54:59	RW	MCBAMR2A1Q_CFG_A1MAP_COL11: DRAM Column Address Bit 11
60:63	RW	MCBAMR2A1Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 1 Address Map Register 3*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR3A1Q
Address	00000000030106DA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A1Q_CFG_A1MAP_COL9: DRAM Column Address Bit 9
6:11	RW	MCBAMR3A1Q_CFG_A1MAP_COL8: DRAM Column Address Bit 8
12:17	RW	MCBAMR3A1Q_CFG_A1MAP_COL7: DRAM Column Address Bit 7
18:23	RW	MCBAMR3A1Q_CFG_A1MAP_COL6: DRAM Column Address Bit 6
24:29	RW	MCBAMR3A1Q_CFG_A1MAP_COL5: DRAM Column Address Bit 5
30:35	RW	MCBAMR3A1Q_CFG_A1MAP_COL4: DRAM Column Address Bit 4
36:41	RW	MCBAMR3A1Q_CFG_A1MAP_COL3: DRAM Column Address Bit 3
42:47	RW	MCBAMR3A1Q_CFG_A1MAP_COL2: DRAM Column Address Bit 2 - Map to an Unused Address bit if NOT fixed BL= 4
48:63	RW	MCBAMR3A1Q_RESERVED_48_63: Not Implemented

Register Name	*MCBIST Control Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCB_CNTLQ
Address	00000000030106DB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCB_CNTLQ_MCB_START: Start bit - Self resetting bit. Kicks off the MCBIST operation
1	RWX	MCB_CNTLQ_MCB_STOP: Stop bit - Self resetting bit. Stops after Current MCBIST subtest is done.
2:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Configured Command Sequence Status Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCB_CNTLSTATQ
Address	00000000030106DC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCB_CNTLSTATQ_MCB_IP: IP bit - Hdw sets to a '1'b when MCBIST run in progress
1	RWX	MCB_CNTLSTATQ_MCB_DONE: Done bit - Hdw sets to a '1'b when MCBIST run complete
2	RWX	MCB_CNTLSTATQ_MCB_FAIL: Fail bit - Hdw sets to a '1'b when MCBIST run failed
3:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*RCD/LRDIMM Control Words 0 - 15*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.RCD_LRDIM_CNTL_WORD0_15Q
Address	00000000030106DD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD0: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
4:7	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD1: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
8:11	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD2: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
12:15	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD3: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
16:19	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD4: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
20:23	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD5: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
24:27	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD6: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)

Bits	SCOM	Field Mnemonic: Description
28:31	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD7: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
32:35	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD8: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
36:39	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD9: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
40:43	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD10: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
44:47	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD11: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
48:51	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD12: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
52:55	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD13: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
56:59	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD14: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
60:63	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD15: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)

Register Name	***CCS Array Error Injection Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.CCSARRERRINJQ
Address	00000000030106DE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	CCSARRERRINJQ_CCS_ARRAY_CE_ERR_INJ_MODE: CE Error inject mode into the ccs array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
1	RW	CCSARRERRINJQ_CCS_ARRAY_CE_ERR_INJ: CE Error inject into the ccs array
2	RW	CCSARRERRINJQ_CCS_ARRAY_UE_ERR_INJ_MODE: UE Error inject mode into the ccs array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	CCSARRERRINJQ_CCS_ARRAY_UE_ERR_INJ: UE Error inject into the ccs array
4	RW	CCSARRERRINJQ_CS_CHIP_ID_2N_MODE: CS_n(2), CS_n(3), CS_n(6), and CS_n(7) used for CHIP IDs for 2N mode Values: CHIP_SELECTS_WILL_BE_ASSERTED_FOR_1_CYCLE_IN_2N_MODE=>0b0 CHIP_SELECTS_BE_ASSERTED_FOR_2_CYCLES_IN_2N_MODE=>0b1
5	RW	CCSARRERRINJQ_DISABLE_2N_MODE: Disable 2N mode Values: ENABLED_2N_MODE_WHEN_THE_CHIP_IS_IN_2N_MODE=>0b0 DISABLES_2N_MODE_WHEN_THE_CHIP_IS_IN_2N_MODE=>0b1
6:63	RW	CCSARRERRINJQ_RESERVED_6_63: RESERVED

Register Name	***MCBIST Memory Register 7***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBMR7Q
Address	00000000030106DF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST28_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST28_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST28_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST28_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST28_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST28_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST28_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST28_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST28_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST29_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST29_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST29_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST29_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST29_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST29_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST29_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST29_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST29_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST30_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST30_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST30_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST30_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST30_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST30_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST30_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST30_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST30_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST31_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST31_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST31_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST31_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST31_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST31_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST31_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST31_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST31_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Configuration Register***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBCFGQ
Address	00000000030106E0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:41	RW	MCBCFGQ_RESERVED_0_41: Not used
42:55	RW	MCBIST_CFG_REF_WAIT_TIME: This is the refresh wait time in memory clock cycles. When doing the Refresh only subtest, MCBIST will wait time amount of time before it goes on to the next subtest.
56:59	RW	MCBCFGQ_RESERVED_56_59: Not used
60	RW	MCBIST_CFG_RESET_ERROR_DATA: Reset error log RA, error counters, Status Reg and error map. Note SRB buffer cannot be reset all the time since the data path is not accessible by MCBIST. Rising edge triggered. Must be a 0 and then set to a 1 to force a reset: Values: RESET_INACTIVE=>0b0 RESET_ERROR_LOGS=>0b1
61	RW	MCBIST_CFG_BREAK_ON_SUBTEST: Break on subtest Values: DO_NOT_BREAK_WHEN_SUBTEST_COMPLETES=>0b0 BREAK_WHEN_CURRENT_SUBTEST_COMPLETES_IS_USED_TO_STOP_A_LOOPING_RUN_OF_REFRESH_ONLY=>0b1
62	RW	MCBIST_CFG_STOP_ON_ERR: Stop on error. MCBCMABQ[36] will determine if the stop on error occurs after 1 error is seen or after 8 errors is seen. Values: DO_NOT_STOP_ON_ERROR=>0b0 STOP_ON_ERROR_AFTER_SUBTEST_COMPLETES=>0b1
63	RW	MCBCFGQ_RESERVED_63: Not used

Register Name	***Port A Socket 2 Address Map Register 0***
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR0A2Q
Address	00000000030106E1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK0: Master Rank Bit 0 (MSB)
6:11	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK1: Master Rank Bit 1
12:17	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK2: Master Rank Rank Bit 2
18:23	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK3: Master Rank Rank Bit 3
24:29	RW	MCBAMR0A2Q_CFG_A2MAP_SRANK0: Slave Rank Bit 0 (MSB)
30:35	RW	MCBAMR0A2Q_CFG_A2MAP_SRANK1: Slave Rank Bit 1
36:41	RW	MCBAMR0A2Q_CFG_A2MAP_SRANK2: Slave Rank Rank Bit 2
42:47	RW	MCBAMR0A2Q_CFG_A2MAP_BANK3: DRAM Bank Address Bit 3 (MSB)
48:53	RW	MCBAMR0A2Q_CFG_A2MAP_BANK2: DRAM Bank Address Bit 2 (MSB)
54:59	RW	MCBAMR0A2Q_CFG_A2MAP_BANK1: DRAM Bank Address Bit 1
60:63	RW	MCBAMR0A2Q_RESERVED_60_63: Reserved

Register Name	*Port A Socket 2 Address Map Register 1*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR1A2Q
Address	00000000030106E2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A2Q_CFG_A2MAP_BANK0: DRAM Bank Address Bit 0
6:11	RW	MCBAMR1A2Q_CFG_A2MAP_ROW16: DRAM Row Address Bit16 (MSB)
12:17	RW	MCBAMR1A2Q_CFG_A2MAP_ROW15: DRAM Row Address Bit15
18:23	RW	MCBAMR1A2Q_CFG_A2MAP_ROW14: DRAM Row Address Bit 14
24:29	RW	MCBAMR1A2Q_CFG_A2MAP_ROW13: DRAM Row Address Bit 13
30:35	RW	MCBAMR1A2Q_CFG_A2MAP_ROW12: DRAM Row Address Bit 12
36:41	RW	MCBAMR1A2Q_CFG_A2MAP_ROW11: DRAM Row Address Bit 11
42:47	RW	MCBAMR1A2Q_CFG_A2MAP_ROW10: DRAM Row Address Bit 10
48:53	RW	MCBAMR1A2Q_CFG_A2MAP_ROW9: DRAM Row Address Bit 9
54:59	RW	MCBAMR1A2Q_CFG_A2MAP_ROW8: DRAM Row Address Bit 8
60:63	RW	MCBAMR1A2Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 2 Address Map Register 2*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR2A2Q
Address	00000000030106E3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A2Q_CFG_A2MAP_ROW7: DRAM Row Address Bit 7
6:11	RW	MCBAMR2A2Q_CFG_A2MAP_ROW6: DRAM Row Address Bit 6
12:17	RW	MCBAMR2A2Q_CFG_A2MAP_ROW5: DRAM Row Address Bit 5
18:23	RW	MCBAMR2A2Q_CFG_A2MAP_ROW4: DRAM Row Address Bit 4
24:29	RW	MCBAMR2A2Q_CFG_A2MAP_ROW3: DRAM Row Address Bit 3
30:35	RW	MCBAMR2A2Q_CFG_A2MAP_ROW2: DRAM Row Address Bit 2
36:41	RW	MCBAMR2A2Q_CFG_A2MAP_ROW1: DRAM Row Address Bit 1
42:47	RW	MCBAMR2A2Q_CFG_A2MAP_ROW0: DRAM Row Address Bit 0
48:53	RW	MCBAMR2A2Q_CFG_A2MAP_COL13: DRAM Column Address Bit 13 (MSB)
54:59	RW	MCBAMR2A2Q_CFG_A2MAP_COL11: DRAM Column Address Bit 11
60:63	RW	MCBAMR2A2Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 2 Address Map Register 3*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MCBAMR3A2Q
Address	00000000030106E4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A2Q_CFG_A2MAP_COL9: DRAM Column Address Bit 9
6:11	RW	MCBAMR3A2Q_CFG_A2MAP_COL8: DRAM Column Address Bit 8
12:17	RW	MCBAMR3A2Q_CFG_A2MAP_COL7: DRAM Column Address Bit 7
18:23	RW	MCBAMR3A2Q_CFG_A2MAP_COL6: DRAM Column Address Bit 6
24:29	RW	MCBAMR3A2Q_CFG_A2MAP_COL5: DRAM Column Address Bit 5
30:35	RW	MCBAMR3A2Q_CFG_A2MAP_COL4: DRAM Column Address Bit 4
36:41	RW	MCBAMR3A2Q_CFG_A2MAP_COL3: DRAM Column Address Bit 3
42:47	RW	MCBAMR3A2Q_CFG_A2MAP_COL2: DRAM Column Address Bit 2 - Map to an Unused Address bit if NOT fixed BL= 4
48:63	RW	MCBAMR3A2Q_RESERVED_48_63: Not Implemented

Register Name	*CCS Fixed Data Register 0*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.CCS_FIXED_DATA0Q
Address	00000000030106E5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CCS_FIXED_DATA0Q_FIXED_DATA_0_63: Fixed data from Non traditional Transparent Mode

Register Name	*CCS Fixed Data Register 1*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.CCS_FIXED_DATA1Q
Address	00000000030106E6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_FIXED_DATA1Q_FIXED_DATA_64_79: Fixed data from Non traditional Transparent Mode
16:63	RW	CCS_FIXED_DATA1Q_RESERVED_16_63: RESERVED

Register Name	*MBA Error Report Register*
Mnemonic	MBU.MBA01.MBA_MCBIST.SCOMFIR.MBA_MCBERRPTQ
Address	00000000030106E7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_MCBERRPTQ_MAINT_START_ADDR_ERR: Maint Start Address Error on linked to MBAFIR bit 1
1	ROX	MBA_MCBERRPTQ_MAINT_END_ADDR_ERR: Maint End Address Error on linked to MBAFIR bit 1
2	ROX	MBA_MCBERRPTQ_MCB_FIR_CCS_ERR: CCS FSM Parity Error on linked to MBAFIR bit 3
3	ROX	MBA_MCBERRPTQ_MAINT_1HOT_ST_ERROR: Maint FSM Parity Error on linked to MBAFIR bit 6
4	ROX	MBA_MCBERRPTQ_MCB_FIR_MCBAGEN_ERR: MCBIST Address Generation FSM Parity Error on linked to MBAFIR bit 3
5	ROX	MBA_MCBERRPTQ_MCB_FIR_MCBFSM_ERR: MCBIST Control FSM Parity Error on linked to MBAFIR bit 3
6	ROX	MBA_MCBERRPTQ_MBMCCQ_PE: SCOM Register Parity Error on mbmccq linked to MBAFIR bit 5
7	ROX	MBA_MCBERRPTQ_CCS_CNTLQ_PE: SCOM Register Parity Error on ccs_cntlq linked to MBAFIR bit 6
8	ROX	MBA_MCBERRPTQ_MCB_CNTLQ_PE: SCOM Register Parity Error on mcb_cntlq linked to MBAFIR bit 6
9	ROX	MBA_MCBERRPTQ_MBSPAQ_PE: SCOM Register Parity Error on mbspaq linked to MBAFIR bit 5
10	ROX	MBA_MCBERRPTQ_MAINT_CCS_PE: SCOM Register Parity Error on maint and ccs register linked to MBAFIR bit 5
11	ROX	MBA_MCBERRPTQ_MCBAGEN_PE: SCOM Register Parity Error linked on mcbist address generation registers to MBAFIR bit 5
12	ROX	MBA_MCBERRPTQ_MCBDGEN_PE: SCOM Register Parity Error linked on mcbist data generation registers to MBAFIR bit 5
13	ROX	MBA_MCBERRPTQ_MCB_CONTROLLER_PE: SCOM Register Parity Error linked on mcbist controller configuration registers to MBAFIR bit 5
14	ROX	MBA_MCBERRPTQ_MBABS0_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
15	ROX	MBA_MCBERRPTQ_MBABS1_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
16	ROX	MBA_MCBERRPTQ_MBABS2_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
17	ROX	MBA_MCBERRPTQ_MBABS3_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
18	ROX	MBA_MCBERRPTQ_MBABS4_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
19	ROX	MBA_MCBERRPTQ_MBABS5_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
20	ROX	MBA_MCBERRPTQ_MBABS6_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
21	ROX	MBA_MCBERRPTQ_MBABS7_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
22	ROX	MBA_MCBERRPTQ_MBA_INJQ_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
23	ROX	MBA_MCBERRPTQ_MBA_WRD_MODE_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 6
24	ROX	MBA_MCBERRPTQ_MBMACAQ_PE: Maint Address SCOM Register Parity Error linked to MBAFIR bit 6
25	ROX	MBA_MCBERRPTQ_MBMCTQ_PE: Maint Command Type SCOM Register Parity Error linked to MBAFIR bit 6
26:63	ROX	MBA_MCBERRPTQ_RESERVED_26_63: RESERVED

Register Name	*Trace Array High Data Register*
Mnemonic	TCM.TRA.MBA01TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000003010880 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	*Trace Array Low Data Register*
Mnemonic	TCM.TRA.MBA01TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000003010881 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	*MBA CAL FIR Register (MBACALFIR)*
Mnemonic	MBU.MBA23.MBA_SRQ.MBACALFIRQ
Address	0000000003010C00 (SCOM) 0000000003010C01 (SCOM1) 0000000003010C02 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_RECOVERABLE_ERROR: When set, a MBA recoverable error has occurred. These include cal[0:3]_cfg, rrq, wrq and power control parity errors
1	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_NONRECOVERABLE_ERROR: When set, a MBA nonrecoverable error has occurred. These include dsm, tmr, farb and SIR parity errors
2	RWX	WOX_AND	WOX_OR	MBACALFIRQ_REFRESH_OVERRUN: When set, nine (9) refreshes have been enqueued to any single rank.
3	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WAT__ERROR: When set, an error has been detected in the MBA debug WAT logic
4	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR_0: When set, a RCD parity error has been detected on DDR port 0

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR0_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr0
6	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR1_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr1
7	RWX	WOX_AND	WOX_OR	MBACALFIRQ_RCD_PARITY_ERROR_1: When set, a RCD parity error has been detected on DDR port 1
8	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBX_TO_MBA_PAR_ERROR: When set, indicates a rdcmd_par, rdcmd_par_rc, rdcmd_par rd1, rdcmd_par_rc rd1, wrcmd_par, wrcmd_par_rc or a wrd_idx_par error has been detected.
9	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_WRD_UE: When set, indicates that a mba_wrd ue has been detected
10	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_WRD_CE: When set, indicates that a mba_wrd ce has been detected
11	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_MAINT_UE: When set, indicates that a mba_maint ue has been detected
12	RWX	WOX_AND	WOX_OR	MBACALFIRQ_MBA_MAINT_CE: When set, indicates that a mba_maint ce has been detected
13	RWX	WOX_AND	WOX_OR	MBACALFIRQ_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR phy(s) did not clear a pending calibration update request.
14	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_DATA_CE: When set, indicates that a ce detected on the wrq data buffer data.
15	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_DATA_UE: When set, indicates that a ue detected on the wrq data buffer data.
16	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_DATA_SUE: When set, indicates that a sue detected on the wrq data buffer data.
17	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
18	RWX	WOX_AND	WOX_OR	MBACALFIRQ_SM_1HOT_ERR: When set, indicates a state machine one hot error.
19	RWX	WOX_AND	WOX_OR	MBACALFIRQ_WRD_SCOM_ERROR: When set indicates the WRD_MAC scom satellite detected an internal error.
20	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred
21	RWX	WOX_AND	WOX_OR	MBACALFIRQ_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error
22:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000

Register Name	***MBA CAL FIR Mask Register (MBACALFIR_MASK)***
Mnemonic	MBU.MBA23.MBA_SRQ.MBACALFIR_MASK
Address	0000000003010C03 (SCOM) 0000000003010C04 (SCOM1) 0000000003010C05 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_RECOVERABLE_ERROR: When set, a MBA recoverable error has occurred. These include cal[0:3]_cfg, rrq, wrq and power control parity errors
1	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_NONRECOVERABLE_ERROR: When set, a MBA nonrecoverable error has occurred. These include dsm, tmr, farb and SIR parity errors
2	RW	WO_AND	WO_OR	MBACALFIR_MASK_REFRESH_OVERRUN: When set, a refresh request was detected to a rank that is in high-priority refresh state, indicating that the high-priority refresh was not serviced before another refresh request is received.
3	RW	WO_AND	WO_OR	MBACALFIR_MASK_WAT__ERROR: When set, an error has been detected in the MBA debug WAT logic
4	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR_0: When set, a RCD parity error has been detected on DDR port 0
5	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR0_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr0
6	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR1_CAL_TIMEOUT_ERR: When set, a calibration complete indication was not received in the calibration timeout time for ddr1
7	RW	WO_AND	WO_OR	MBACALFIR_MASK_RCD_PARITY_ERROR_1: When set, a RCD parity error has been detected on DDR port 1
8	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBX_TO_MBA_PAR_ERROR: When set, indicates a rdcmd_par, rdcmd_par_rc, rdcmd_par rd1, rdcmd_par_rc rd1, wrcmd_par, wrcmd_par_rc or a wrd_idx_par error has been detected.
9	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_WRD_UE: When set, indicates that a mba_wrd ue has been detected
10	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_WRD_CE: When set, indicates that a mba_wrd ce has been detected
11	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_MAINT_UE: When set, indicates that a mba_maint ue has been detected
12	RW	WO_AND	WO_OR	MBACALFIR_MASK_MBA_MAINT_CE: When set, indicates that a mba_maint ce has been detected
13	RW	WO_AND	WO_OR	MBACALFIR_MASK_DDR_CAL_RESET_TIMEOUT: When set, indicates that a soft reset issued to the DDR phy(s) did not clear a pending calibration update request.
14	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_DATA_CE: When set, indicates that a ce detected on the wrq data buffer data.
15	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_DATA_UE: When set, indicates that a ue detected on the wrq data buffer data.
16	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_DATA_SUE: When set, indicates that a sue detected on the wrq data buffer data.
17	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRQ_RRQ_HANG_ERR: When set, indicates that the WRQ or RRQ is in a hung state.
18	RW	WO_AND	WO_OR	MBACALFIR_MASK_SM_1HOT_ERR: When set, indicates a state machine one hot error.
19	RW	WO_AND	WO_OR	MBACALFIR_MASK_WRD_SCOM_ERROR: When set indicates the WRD_MAC scom satellite detected an internal error.
20	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR: When set, and internal SCOM error has occurred
21	RW	WO_AND	WO_OR	MBACALFIR_MASK_INTERNAL_SCOM_ERROR_COPY: Copy of internal scom error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22:63	RO	N/A	N/A	constant=0b0000000000000000000000000000000000000000000000

Register Name	*MBA CAL FIR Action 0 Register (MBACALFIR_ACTION0)*
Mnemonic	MBU.MBA23.MBA_SRQ.MBACALFIR_ACTION0
Address	0000000003010C06 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:21	RW	MBACALFIR_ACTION0_FIR_ACTION0: MBA action0 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
22:63	RO	constant=0b0000000000000000000000000000000000000000000000

Register Name	*MBA CAL FIR Action 1 Register (MBACALFIR_ACTION1)*
Mnemonic	MBU.MBA23.MBA_SRQ.MBACALFIR_ACTION1
Address	0000000003010C07 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:21	RW	MBACALFIR_ACTION1_FIR_ACTION1: MBA action1 select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
22:63	RO	constant=0b0000000000000000000000000000000000000000000000

Register Name	*Data State Machine Configurations*
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_DSM0Q
Address	0000000003010C0A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_DSM0Q_CFG_RODT_START_DLY: Delay from read command to ODT turn on
6:11	RW	MBA_DSM0Q_CFG_RODT_END_DLY: Delay from read command to ODT turn off
12:17	RW	MBA_DSM0Q_CFG_WODT_START_DLY: Delay from write command to ODT turn on
18:23	RW	MBA_DSM0Q_CFG_WODT_END_DLY: Delay from write command to ODT turn off
24:29	RW	MBA_DSM0Q_CFG_WRDONE_DLY: Delay from write command to write done to MBS
30:35	RW	MBA_DSM0Q_CFG_WRDATA_DLY: Delay from write command to stating the write data flow
36:41	RW	MBA_DSM0Q_CFG_RDTAG_DLY: Delay from read command to rd data valid back to MBS
42	RW	MBA_DSM0Q_CFG_RDTAG_MBX_CYCLE: Determines the mem clock 1/2 cycle that the rdtag entry is released from the dsm queue. 0 = release when mbx clock is low 1= release when mbx clock is high

Bits	SCOM	Field Mnemonic: Description
43:48	RW	MBA_DSM0Q_CFG_RODT_BC4_END_DLY: Delay from read command to ODT turn off for BC4 command
49:54	RW	MBA_DSM0Q_CFG_WODT_BC4_END_DLY: Delay from write command to ODT turn off for BC4 command
55	RW	MBA_DSM0Q_CFG_SYNC_RDTAG_ENABLE: Enable synchronous rdtag interface between MBA and MBS
56:57	RW	MBA_DSM0Q_CFG_GOLDEN_DELAY_MODE: Programmable delay to apply to synchronization pulse between MBS and MBA for synchronous rdtag mode
58:63	RW	MBA_DSM0Q_RESERVED_58_63: Reserved

Register Name	***DDR Data Bus Timing Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_TMR0Q
Address	0000000003010C0B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBA_TMR0Q_RRSMSR_DLY: Read to Read same mastersame rank
4:7	RW	MBA_TMR0Q_RRSMDR_DLY: Read to Read same masterdifferent rank
8:11	RW	MBA_TMR0Q_RRDM_DLY: Read to Read to different master
12:15	RW	MBA_TMR0Q_RWSMSR_DLY: Read to Write same mastersame rank
16:19	RW	MBA_TMR0Q_RWSMDR_DLY: Read to Write same masterdifferent rank
20:23	RW	MBA_TMR0Q_RWDM_DLY: Read to Write different master
24:29	RW	MBA_TMR0Q_WRSMSR_DLY: Write to read same mastersame rank
30:35	RW	MBA_TMR0Q_WRSMDR_DLY: Write to read same masterdifferent rank
36:39	RW	MBA_TMR0Q_WRDM_DLY: Write to Read different master
40:43	RW	MBA_TMR0Q_WWSMSR_DLY: Write to Write same mastersame rank
44:47	RW	MBA_TMR0Q_WWSMDR_DLY: Write to Write same masterdifferent rank
48:51	RW	MBA_TMR0Q_WWDM_DLY: Write to Write different master
52:55	RW	MBA_TMR0Q_RROP_DLY: Read open page to read delay
56:59	RW	MBA_TMR0Q_WWOP_DLY: Write open page to write delay
60:63	RW	MBA_TMR0Q_TRRD: Activate to activate delay

Register Name	***DDR Bank Busy Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_TMR1Q
Address	0000000003010C0C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RW	MBA_TMR1Q_CFG_TRAP: Read with auto precharge total time(max)
7:13	RW	MBA_TMR1Q_CFG_TWAP: Write with auto precharge total time
14:19	RW	MBA_TMR1Q_CFG_TFAW: Four activate window time

Bits	SCOM	Field Mnemonic: Description
20:23	RW	MBA_TMR1Q_RRSBG_DLY: (DDR4) Ras to Ras same bank group(Trrd_l)
24:28	RW	MBA_TMR1Q_WRSBG_DLY: (DDR4) write to read same bank group(twtr_l)
29	RW	MBA_TMR1Q_CFG_DDR4_CL_INTL_DIS: Disable bank group interleaving for DDR4.
30:63	RW	MBA_TMR1Q_RESERVED_30_63: Reserved

Register Name	***DDR Write Command Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_WRQ0Q
Address	0000000003010C0D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBA_WRQ0Q_CFG_WRITE_HW_MARK: Write highwater mark(force writes HPenables writes)
5	RW	MBA_WRQ0Q_CFG_WRQ_FIFO_MODE: Prevent reordering in the WRQ(only entry0 can be selected) HP Cleaner writes will not get selected till they are in entry 0.
6	RW	MBA_WRQ0Q_CFG_DISABLE_WR_PG_MODE: Disable page commands for WRQ
7:18	RW	MBA_WRQ0Q_CFG_WRQ_ENTRY0_HP_DLY: Time for entry0 of the WRQ before it forces HP setting this dial to a 0, will disable entry0 HP
19	RW	MBA_WRQ0Q_CFG_WRQ_FLUSH_WR_RANK: When one write is issued to a rank, try to force more writes to that rank to avoid multiple write to read same rank penalties.
20	RW	MBA_WRQ0Q_CFG_WRQ_ENABLE_NON_HP_WR: Allow writes when they do not meet a condition like entry0_flush, or rd_idle_allow_wr, etc
21:32	RW	MBA_WRQ0Q_CFG_ENTRY0_MIN_FOR_RRQ_IDLE_WR: This is an added condition to allowing writes when the RRQ is idle. This addition allows for multiple writes to stack up in the WRQ before starting the write burst.
33:37	RW	MBA_WRQ0Q_CFG_RRQ_IDLE_LOW_WATERMARK: RRQ idle will also allow writes if the above condition is met of the wrq meets the cfg_rrq_idle_low_watermark condition. For example if this dial is set to 8, and there are more then 8 entries in the wrq then the condition will allow writes when the rrq_idle period is met.
38:43	RW	MBA_WRQ0Q_CFG_WRQ_SKIP_LIMIT: The number of times entry0 of the WRQ can be skipped before entry0 prevents older writes from being issued until entry0 is sent.
44	RW	MBA_WRQ0Q_CFG_WRQ_CLN_HP_ENABLE: Set to 1 to enable cleaner_hp_flush event. When the cleaner is backed up, it will tell the MBA wrq to flush writes to a specific rank. Set to 0, this input into MBA is ignored.
45:52	RW	MBA_WRQ0Q_CFG_WRQ_HANG_THRESHOLD: Hang detection for entry0 of WRQ. Incrememnts every mcbist_srq_hang_pulse(2048 phase hold cycles), and will set a fir when the count=threshold and another pulse is received. Since this checks for count=threshold, a value of 0 is not valid.
53:60	RW	MBA_WRQ0Q_CFG_RRQ_HANG_THRESHOLD: Hang detection for entry0 of RRQ. Incrememnts every mcbist_srq_hang_pulse(2048 phase hold cycles), and will set a fir when the count=threshold and another pulse is received. Since this checks for count=threshold, a value of 0 is not valid.
61:63	RW	MBA_WRQ0Q_RESERVED_61_63: Reserved

Register Name	***DDR Read Command Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_RRQ0Q
Address	0000000003010C0E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_RRQ0Q_CFG_RRQ_SKIP_LIMIT: Number of times the bottom entry in the RRQ can be skipped before preventing the entry from being skipped
6:10	RW	MBA_RRQ0Q_CFG_RRQ_REORDER_DEPTH: RRQ reordering depth, 0x10 use all 16 entries 0x0F use bottom 15 entries ... 0x00 use bottom entry(fifo mode)
11	RW	MBA_RRQ0Q_CFG_DISABLE_RD_PG_MODE: Disable page commands for RRQ
12	RW	MBA_RRQ0Q_CFG_DISABLE_FAST_PATH: Disable MBA RRQ fastpath
13:23	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR0: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=000
24:34	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR1: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=001
35:45	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR2: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=011
46:56	RW	MBA_RRQ0Q_CFG_RD_IDLE_ALLOW_WR3: Time with a empty RRQ before writes will be enabled Use this value when mbx_mba_cln_dv_bklog_q=111
57:63	RW	MBA_RRQ0Q_RESERVED_57_63: Reserved

Register Name	***DDR Calibration Registers***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_CAL0Q
Address	0000000003010C0F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL0Q_CFG_CAL_INTERVAL_TMR0_ENABLE: Enable interval tmr0
1:2	RW	MBA_CAL0Q_CFG_TIME_BASE_TMR0: Time base for interval tmr0 counter Values: 1_CYCLE=>0b00 256_CYCLES=>0b01 16384_CYCLE=>0b10 16777216_CYCLES=>0b11
3:11	RW	MBA_CAL0Q_CFG_INTERVAL_COUNTER_TMR0: Interval timer based on time_base(time_base*interval_counter)
12	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops, should always be 1 if the timer is enabled
13:16	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
17	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1
18	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops

Bits	SCOM	Field Mnemonic: Description
19:22	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
23	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2
24	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops
25:28	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_TYPE: 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
29	RW	MBA_CAL0Q_CFG_CAL_TMR0_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3
30:38	RW	MBA_CAL0Q_CFG_CAL_TMR0_Z_SYNC: The timer value will be set to this value during z sync.
39:46	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR: Wait time for DDR soft reset upon calibration timeout fail.
47:48	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_TMR_TB: Timebase interval for ddr_reset_tmr Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
49	RW	MBA_CAL0Q_CFG_CAL_TMR0_DDR_RESET_ENABLE: Enable DDR soft reset upon calibration timeout fail. 0 Do not issue soft DDR reset upon calibration timeout. 1 Issue DDR soft reset upon calibration timeout.
50	RW	MBA_CAL0Q_CFG_CAL_TMR0_SINGLE_RANK: Enable single-rank mode for timer0 calibrations. Calibrations programmed in tmr0 will run on 1 rank at a time per timer expiration. 0 Issue calibrations for all enabled ranks per timer expiration. 1 Issue calibrations for 1 rank at a time per timer expiration.
51	RW	MBA_CAL0Q_INJECT_CAL0_PAR_ERROR: Setting to 1 will inject one parity error, must be set to 0 and then 1 again to inject another error 0 No error inject 1 Inject one parity error
52	RW	MBA_CAL0Q_INJECT_1HOT_SM_ERROR: Setting to 1 will inject one 1hot sm error, must be set to 0 and then 1 again to inject another error 0 No error inject 1 Inject one 1hot sm error
53:55	RW	MBA_CAL0Q_CFG_CAL_SINGLE_PORT_MODE: Single port mode config, default is both ports are calibrated at the same time, options are single port calibrated at a time with both ports powered up single port calibrated at a time with one port powered up single port calibrated at a time with one port powered up and only the rank requested by the DDR PHY powered up, only to be used in single rank mode Values: DEFAULT=>0b000 SINGLE_PORT_CAL_BOTH_PORT_PUP=>0b100 SINGLE_PORT_CAL_ONE_PORT_PUP=>0b110 SINGLE_PORT_CAL_ONE_PORT_ONE_RANK_PUP=>0b111
56:63	RW	MBA_CAL0Q_RESERVED_56_63: Reserved

Register Name	***DDR Calibration Registers***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_CAL1Q
Address	0000000003010C10 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL1Q_CFG_CAL_INTERVAL_TMR1_ENABLE: Enable interval tmr1

Bits	SCOM	Field Mnemonic: Description
1:2	RW	MBA_CAL1Q_CFG_TIME_BASE_TMR1: Time base for interval tmr1 counter Values: 1_CYCLE=>0b00 256_CYCLES=>0b01 16384_CYCLE=>0b10 16777216_CYCLES=>0b11
3:11	RW	MBA_CAL1Q_CFG_INTERVAL_COUNTER_TMR1: Interval timer based on time_base(time_base*interval_counter)
12	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops, should always be 1 if the timer is enabled
13:16	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
17	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1
18	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops
19:22	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
23	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2
24	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops
25:28	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_TYPE: 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
29	RW	MBA_CAL1Q_CFG_CAL_TMR1_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3
30:38	RW	MBA_CAL1Q_CFG_CAL_TMR1_Z_SYNC: The timer value will be set to this value during z sync.
39	RW	MBA_CAL1Q_CFG_CAL_TMR1_SINGLE_RANK: Enable single-rank mode for timer1 calibrations. Calibrations programmed in tmr1 will run on 1 rank at a time per timer expiration. 0 Issue calibrations for all enabled ranks per timer expiration. 1 Issue calibrations for 1 rank at a time per timer expiration.
40:63	RW	MBA_CAL1Q_RESERVED_40_63: Reserved

Register Name	***DDR Calibration Registers***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_CAL2Q
Address	0000000003010C11 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_CAL2Q_CFG_CAL_INTERVAL_TMR2_ENABLE: Enable interval tmr2
1:2	RW	MBA_CAL2Q_CFG_TIME_BASE_TMR2: Time base for interval tmr2 counter Values: 1_CYCLE=>0b00 256_CYCLES=>0b01 16384_CYCLE=>0b10 16777216_CYCLES=>0b11
3:11	RW	MBA_CAL2Q_CFG_INTERVAL_COUNTER_TMR2: Interval timer based on time_base(time_base*interval_counter)

Bits	SCOM	Field Mnemonic: Description
12	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_ENABLE: Enable bit for first calibration to perform when timer pops, should always be 1 if the timer is enabled
13:16	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
17	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL1_DDR_DONE: Use the complete signal from the DDR for cal1
18	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_ENABLE: Enable bit for second calibration to perform when timer pops
19:22	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_TYPE: 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
23	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL2_DDR_DONE: Use the complete signal from the DDR for cal2
24	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_ENABLE: Enable bit for third calibration to perform when timer pops
25:28	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_TYPE: 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step 0011 Periodic Calibration: Run SysClk, DQS and Read Eye all in parallel (default behavior).
29	RW	MBA_CAL2Q_CFG_CAL_TMR2_CAL3_DDR_DONE: Use the complete signal from the DDR for cal3
30:38	RW	MBA_CAL2Q_CFG_CAL_TMR2_Z_SYNC: The timer value will be set to this value during z sync
39	RW	MBA_CAL2Q_CFG_CAL_TMR2_SINGLE_RANK: Enable single-rank mode for timer2 calibrations. Calibrations programmed in tmr2 will run on 1 rank at a time per timer expiration. 0 Issue calibrations for all enabled ranks per timer expiration. 1 Issue calibrations for 1 rank at a time per timer expiration.
40:63	RW	MBA_CAL2Q_RESERVED_40_63: Reserved

Register Name	***DDR Calibration Length Registers***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_CAL3Q
Address	0000000003010C12 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_TB: Internal ZQ time base Time base for internal ZQ cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
2:9	RW	MBA_CAL3Q_CFG_INTERNAL_ZQ_LENGTH: Number of internal ZQ time bases required to meet max internal zq length
10:11	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_TB: External ZQ time base Time base for external ZQ cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
12:19	RW	MBA_CAL3Q_CFG_EXTERNAL_ZQ_LENGTH: Number of external ZQ time bases required to meet max external zq length

Bits	SCOM	Field Mnemonic: Description
20:21	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_TB: ReadclkSysclk time base Time base for readclksysclk cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
22:29	RW	MBA_CAL3Q_CFG_RDCLK_SYSCLK_LENGTH: Number of Readclksysclk time bases required to meet max rdclk length
30:31	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_TB: Dqs alignment time base Time base for DQS alignment cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
32:39	RW	MBA_CAL3Q_CFG_DQS_ALIGNMENT_LENGTH: Number of Dqs alignment time bases required to meet max dqs alignment length
40:41	RW	MBA_CAL3Q_CFG_MPR_READEYE_TB: Readeye time base Time base for readeye cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
42:49	RW	MBA_CAL3Q_CFG_MPR_READEYE_LENGTH: Number of readeye time bases required to meet max external zq length
50:51	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_TB: All Periodics time base Time base for all periodic cal counter Values: 1_CYCLE=>0b00 64_CYCLES=>0b01 512_CYCLE=>0b10 8192_CYCLES=>0b11
52:59	RW	MBA_CAL3Q_CFG_ALL_PERIODIC_LENGTH: Number of all_periodic time bases required to meet max calibration length for all periodic calibration (in parallel)
60:63	RW	MBA_CAL3Q_RESERVED_60_63: Reserved

Register Name	***Final Arb Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_FARB0Q
Address	0000000003010C13 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:10	RW	Reserved.
11:23	RW	Reserved.
24:30	RW	MBA_FARB0Q_CFG_MAX_READS_IN_A_ROW: Limits the max number of reads in a row, before forcing a write. There must be a write in the WRQ for the counting to start. 0x00 Disabled 0x01 1 read before allowing a write 0x7F 127 reads before forcing a write
31:37	RW	MBA_FARB0Q_CFG_MAX_WRITES_IN_A_ROW: Limits the max number of writes in a row, before forcing a read. There must be a read in the RRQ for the counting to start. 0x00 Disabled 0x01 1 write before allowing a read 0x7F 127 write before forcing a read

Bits	SCOM	Field Mnemonic: Description
38	RW	MBA_FARB0Q_CFG_PARITY_AFTER_CMD: Determines when parity will be driven 0b0 parity driven same cycle as the command 0b1parity driven the cycle after the command (also turns on OE for the parity cycle)
39	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_RAS0: Inject a parity error on next RAS on port 0 according to inject type selected in bit 59
40	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CAS0: Inject a parity error on next CAS on port 0 according to inject type selected in bit 59
41	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_RAS1: Inject a parity error on next RAS on port 1 according to inject type selected in bit 59
42	RWX	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CAS1: Inject a parity error on next CAS on port 1 according to inject type selected in bit 59
43:47	RW	MBA_FARB0Q_CFG_PARITY_DETECT_TIME: Measures the time from an injected error till when the error is detected back at the MBA
48:53	RW	MBA_FARB0Q_CFG_RCD_PROTECTION_TIME: Time interval in which commands were sent out before a rcd parity error occurrence that should be re-issued. Should be set >= to cfg_parity_detect_time
54	RW	MBA_FARB0Q_CFG_DISABLE_RCD_RECOVERY: Disable the rcd recovery procedure.
55	RW	MBA_FARB0Q_CFG_OE_ALWAYS_ON: Force DDR OE to always be on(never tristate the ddr addr drivers)
56	RW	MBA_FARB0Q_CFG_FLIP_PORT1_ADDR: Set to 1 to enable port 1 Address bit flipping. Address bits that will be flipped: bank(0:2), Addr(3:9, 11, 13-15)
57	RW	MBA_FARB0Q_CFG_DISABLE_REFRESH_DURING_NOISE_WDW: Default 0, allows refreshes during a noise window. Set to 1, to disable refreshes during a noise window.
58	RW	MBA_FARB0Q_CFG_NM_PER_SLOT_ENABLED: Reserved.
59	RW	MBA_FARB0Q_CFG_INJECT_PARITY_ERR_CONSTANT: If set, parity errors are injected continuously; otherwise, parity errors are injected only once
60	RW	MBA_FARB0Q_CFG_IGNORE_RCD_PARITY_ERR: If set, rcd parity errors are not logged and recovery is not started. When this is set, cfg_disable_rcd_recovery becomes irrelevant because recovery is never started.
61:63	RW	MBA_FARB0Q_RESERVED_61_63: Reserved

Register Name	***Final Arb Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_FARB1Q
Address	0000000003010C14 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_FARB1Q_CFG_M0S0_CS: Chip selects for M0S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
6:11	RW	MBA_FARB1Q_CFG_M0S1_CS: Chip selects for M0S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
12:17	RW	MBA_FARB1Q_CFG_M0S2_CS: Chip selects for M0S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
18:23	RW	MBA_FARB1Q_CFG_M0S3_CS: Chip selects for M0S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
24:29	RW	MBA_FARB1Q_CFG_M0S4_CS: Chip selects for M0S4 OR M2S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
30:35	RW	MBA_FARB1Q_CFG_M0S5_CS: Chip selects for M0S5 OR M2S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
36:41	RW	MBA_FARB1Q_CFG_M0S6_CS: Chip selects for M0S6 or M2S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
42:47	RW	MBA_FARB1Q_CFG_M0S7_CS: Chip selects for M0S7 or M2S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14

Bits	SCOM	Field Mnemonic: Description
48:51	RW	MBA_FARB1Q_CFG_CS_S0_MASK: Mask bits for the chip select. This mask register masks the actual chip select bits while allowing chip_id bits to go out for 2N mode. Set by cs_mapping gdial.
52	RW	MBA_FARB1Q_CFG_S0_DIS_SMDR: Set to 1 if using a 5D config in slot 0, This will using the different master parms instead of the SMDR.
53:63	RW	MBA_FARB1Q_CFG_S0_RSV0: Reserved

Register Name	***Final Arb Parameters***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_FARB2Q
Address	0000000003010C15 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MBA_FARB2Q_CFG_M1S0_CS: Chip selects for M1S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
6:11	RW	MBA_FARB2Q_CFG_M1S1_CS: Chip selects for M1S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
12:17	RW	MBA_FARB2Q_CFG_M1S2_CS: Chip selects for M1S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
18:23	RW	MBA_FARB2Q_CFG_M1S3_CS: Chip selects for M1S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
24:29	RW	MBA_FARB2Q_CFG_M1S4_CS: Chip selects for M1S4 or M3S0, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
30:35	RW	MBA_FARB2Q_CFG_M1S5_CS: Chip selects for M1S5 or M3S1, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
36:41	RW	MBA_FARB2Q_CFG_M1S6_CS: Chip selects for M1S6 or M3S2, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
42:47	RW	MBA_FARB2Q_CFG_M1S7_CS: Chip selects for M1S7 or M3S3, slot 0 0:3 =cs(0 to 3) 4= ODT cs 5=A14
48:63	RW	MBA_FARB2Q_CFG_S0_RSV1: Reserved

Register Name	***N/M Throttling Control***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_FARB3Q
Address	0000000003010C16 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:14	RW	MBA_FARB3Q_CFG_NM_N_PER_MBA: The N value for the NM throttling across a single MBA. The max command count that can occur over a time interval M.
15:30	RW	MBA_FARB3Q_CFG_NM_N_PER_CHIP: The N value for the NM throttling across both MBAs. The max command count that can occur over a time interval M.
31:44	RW	MBA_FARB3Q_CFG_NM_M: The M value for the NM throttling. This counts DRAM clock cycles.
45:47	RW	MBA_FARB3Q_CFG_NM_RAS_WEIGHT: The increment to be added to the N count each time a RAS is sent.
48:50	RW	MBA_FARB3Q_CFG_NM_CAS_WEIGHT: The increment to be added to the N count each time a CAS is sent.
51	RW	MBA_FARB3Q_CFG_NM_PER_SLOT_ENABLED: Default 0, NM events counted per MBA. Set to 1 to count NM events per slot.
52	RW	MBA_FARB3Q_CFG_NM_COUNT_OTHER_MBA_DIS: Set to 1 to turn Counter 2 into a per-MBA counter, disregarding any incrementing from the other MBA (NOTE: also set this to a '1' if you want to fence the other MBA).

Bits	SCOM	Field Mnemonic: Description
53:63	RW	MBA_FARB3Q_RESERVED_53_63: Reserved

Register Name	*MBA Error Report Register*
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_ERR_REPORTQ
Address	0000000003010C1A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_ERR: Rdcmd parity error from MBX MBACALFIR Bit 8
1	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_RC_ERR: Rdcmd RC parity error from MBX MBACALFIR Bit 8
2	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_RD1_ERR: Rdcmd RD1 parity error from MBX MBACALFIR Bit 8
3	ROX	MBA_ERR_REPORTQ_MBA_RDCMD_PAR_RC_RD1_ERR: Rdcmd RC RD1 parity error from MBX MBACALFIR Bit 8
4	ROX	MBA_ERR_REPORTQ_MBA_WRCMD_PAR_ERR: Wrcmd parity error from MBX MBACALFIR Bit 8
5	ROX	MBA_ERR_REPORTQ_MBA_WRCMD_PAR_RC_ERR: Wrcmd RC parity error from MBX MBACALFIR Bit 8
6	ROX	MBA_ERR_REPORTQ_MBA_WRD_IDX_PAR_ERR: WRD index parity error from MBX MBACALFIR Bit 8
7	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_7: reserved
8	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_8: reserved
9	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_9: reserved
10	ROX	MBA_ERR_REPORTQ_WRQ_HANG_ERR: WRQ hang error MBACALFIR Bit 17
11	ROX	MBA_ERR_REPORTQ_RRQ_HANG_ERR: RRQ hang error MBACALFIR Bit 17
12	ROX	MBA_ERR_REPORTQ_DSM_PE_ERR: Parity error in DSM config reg(s) MBACALFIR Bit 1
13	ROX	MBA_ERR_REPORTQ_TMR_PE_ERR: Parity error in TMR config reg(s) MBACALFIR Bit 1
14	ROX	MBA_ERR_REPORTQ_RRQ_PE_ERR: Parity error in RRQ config reg(s) MBACALFIR Bit 1
15	ROX	MBA_ERR_REPORTQ_WRQ_PE_ERR: Parity error in WRQ config reg(s) MBACALFIR Bit 1
16	ROX	MBA_ERR_REPORTQ_FARB_PE_ERR: Parity error in FARB config reg(s) MBACALFIR Bit 1
17	ROX	MBA_ERR_REPORTQ_PC_PE_ERR: Parity error in PC config reg(s) MBACALFIR Bit 1
18	ROX	MBA_ERR_REPORTQ_CAL0_PE_ERR: Parity error in Cal0 config reg MBACALFIR Bit 0
19	ROX	MBA_ERR_REPORTQ_CAL1_PE_ERR: Parity error in Cal1 config reg MBACALFIR Bit 0
20	ROX	MBA_ERR_REPORTQ_CAL2_PE_ERR: Parity error in Cal2 config reg MBACALFIR Bit 0
21	ROX	MBA_ERR_REPORTQ_CAL3_PE_ERR: Parity error in Cal3 config reg MBACALFIR Bit 0
22	ROX	MBA_ERR_REPORTQ_DDR_IF_SM_1HOT_ERR: DDR state machine one hot error MBACALFIR Bit 18
23	ROX	MBA_ERR_REPORTQ_CAL_SM_1HOT_ERR: Calibration state machine one hot error MBACALFIR Bit 18
24	ROX	MBA_ERR_REPORTQ_RANK_SM_1HOT_ERR: Rank state machine one hot error MBACALFIR Bit 18
25	ROX	MBA_ERR_REPORTQ_PC_CAL_REFFSM_1HOT_ERR: Refresh state machine one hot error MBACALFIR Bit 18
26	ROX	MBA_ERR_REPORTQ_PC_CAL_PCFSM_1HOT_ERR: Power Control state machine one hot error MBACALFIR Bit 18

Bits	SCOM	Field Mnemonic: Description
27	ROX	MBA_ERR_REPORTQ_FARB_CAL_RECVFSM_1HOT_ERR: Recovery state machine one hot error MBACALFIR Bit 18
28	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_28: reserved
29	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_29: reserved
30	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_30: reserved
31	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_31: reserved
32	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_32: reserved
33	ROX	MBA_ERR_REPORTQ_SIR_CERR: SIR error MBACALFIR Bit 1
34	ROX	MBA_ERR_REPORTQ_RDCMD_RDCHECK_ERR: Read cmd index check error from MBX MBACALFIR Bit 8
35	ROX	MBA_ERR_REPORTQ_WRD_RDCHECK_ERR: Write cmd index check error from MBX MBACALFIR Bit 8
36	ROX	MBA_ERR_REPORTQ_CAL0_INVALID_ACCESS: Cal0 invalid access MBASECUREFIR Bit 0
37	ROX	MBA_ERR_REPORTQ_CAL1_INVALID_ACCESS: Cal1 invalid access MBASECUREFIR Bit 1
38	ROX	MBA_ERR_REPORTQ_CAL2_INVALID_ACCESS: Cal2 invalid access MBASECUREFIR Bit 2
39	ROX	MBA_ERR_REPORTQ_CAL3_INVALID_ACCESS: Cal3 invalid access MBASECUREFIR Bit 3
40	ROX	MBA_ERR_REPORTQ_DDR_INVALID_ACCESS: DDR invalid access MBASECUREFIR Bit 4
41	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_41: reserved
42	ROX	MBA_ERR_REPORTQ_RESERVED_CERR_42: reserved
43:63	RO	constant=0b00000000000000000000

Register Name	***MBA Secure Fault Isolation Register (MCASFIR)***
Mnemonic	MBU.MBA23.MBA_SRQ.MBASIRQ
Address	0000000003010C1B (SCOM) 0000000003010C1C (SCOM1) 0000000003010C1D (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL0Q_ACCESS: If set, a non-inband write access to MBA_CALQ0 was detected with protection_en active
1	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL1Q_ACCESS: If set, a non-inband write access to MBA_CALQ1 was detected with protection_en active
2	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL2Q_ACCESS: If set, a non-inband write access to MBA_CAL2Q was detected with protection_en active
3	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_MBA_CAL3Q_ACCESS: If set, a non-inband write access to MBA_CAL3Q was detected with protection_en active
4	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_DDR_CONFIG_REG_ACCESS: If set, a non-inband write access to a DDR configuration register was detected with protection_en active
5	RWX	WOX_AND	WOX_OR	MBASIRQ_INVALID_SIR_MASK_OR_ACTION_REGISTER_ACCESS: If set, a non-inband write access to the MBSSIR mask or action registers was detected with protection_en active
6:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBA Secure Fault Isolation Mask Register (MBASIRMASK)*
Mnemonic	MBU.MBA23.MBA_SRQ.MBASIRMASK
Address	0000000003010C1E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBASIRMASK_SIR_MASK: Masks SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBA Secure Fault Isolation Action0 Register (MBASIRACT0)*
Mnemonic	MBU.MBA23.MBA_SRQ.MBASIRACT0
Address	0000000003010C21 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBASIRACT0_ACTION_0: Action 0 for SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBA Secure Fault Isolation Action0 Register (MBASIRACT1)*
Mnemonic	MBU.MBA23.MBA_SRQ.MBASIRACT1
Address	0000000003010C22 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RO	MBASIRACT1_ACTION_1: Action 1 for SIR(0:5)
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Refresh Register 0*
Mnemonic	MBU.MBA23.MBA_SRQ.PC.MBAREF0Q
Address	0000000003010C32 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREF0Q_CFG_REFRESH_ENABLE: Refresh enable

Bits	SCOM	Field Mnemonic: Description
1:2	RW	MBAREF0Q_CFG_REFRESH_INTERVAL_TIMEBASE_SELECT: NOTE: Settings 10 and 11 are for characterizationstess testing only. Values: USE_DEFAULT_REFRESH_INTERVAL=>0b00 USE_A_1_IN_8K_PULSE_AS_A_REFRESH_INTERVAL_TIMEBASE=>0b10 USE_A_1_IN_2_22_PULSE_AS_A_REFRESH_INTERVAL_TIMEBASE=>0b11
3	RW	MBAREF0Q_RESERVED_3: Reserved
4:7	RW	MBAREF0Q_CFG_REFRESH_PRIORITY_THRESHOLD: Once the number of queued refreshes to a rank reaches this threshold, that rank's refreshes become high priority. Values greater than 0x8 can potentially lead to a refresh interval-DRAM spec violation. A value of 0xf is illegal.
8:18	RW	MBAREF0Q_CFG_REFRESH_INTERVAL: For example, for a system with two master ranks and 4 slaves per master (8 ranks total), a desired refresh interval of 7.8us, and DDR-1600 memory, cfg_refresh_interval=7.881.25.008=97 (round down)
19:29	RW	MBAREF0Q_CFG_REFRESH_RESET_INTERVAL: NOTE: refresh reset interval should be set to a value less than the refresh interval
30:39	RW	MBAREF0Q_CFG_TRFC: Refresh to activate rank protection timer
40:49	RW	MBAREF0Q_CFG_REFR_TSV_STACK: Refresh to Refresh spacing within the same TSV stack timer
50:60	RW	MBAREF0Q_CFG_REFR_CHECK_INTERVAL: For example, if using DDR-1600 memory and expecting a refresh to occur every 7.8us: cfg_refr_check_interval=7.81.25.008=780=0x30C If using DDR-1600 memory and expecting a refresh every 3.9us: cfg_refr_check_interval=3.91.25.008=390=0x186
61:63	RW	MBAREF0Q_RESERVED_61_63: Reserved

Register Name	***Rank-to-primary-CKE Mapping Table***
Mnemonic	MBU.MBA23.MBA_SRQ.PC.MBAREF1Q
Address	0000000003010C33 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBAREF1Q_CFG_MRNK0_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
4:7	RW	MBAREF1Q_CFG_MRNK1_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
8:11	RW	MBAREF1Q_CFG_MRNK2_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011

Bits	SCOM	Field Mnemonic: Description
12:15	RW	MBAREF1Q_CFG_MRNK3_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
16:19	RW	MBAREF1Q_CFG_MRNK4_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
20:23	RW	MBAREF1Q_CFG_MRNK5_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
24:27	RW	MBAREF1Q_CFG_MRNK6_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
28:31	RW	MBAREF1Q_CFG_MRNK7_PRIM_CKE: Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011
32:63	RO	constant=0b00000000000000000000000000000000 Values: MA0_CNTL_CKE0=>0b1000 MA0_CNTL_CKE1=>0b0100 MA0_CNTL_CKE01=>0b1100 MA1_CNTL_CKE0=>0b0010 MA1_CNTL_CKE1=>0b0001 MA1_CNTL_CKE01=>0b0011

Register Name	***Power Control Register 0***
Mnemonic	MBU.MBA23.MBA_SRQ.PC.MBARPC0Q
Address	0000000003010C34 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBARPC0Q_CFG_LP2_ENTRY_REQ: Setreset by firmware. When set, MBA powers down all ranks and sets cfg_lp2_state=1. Set by firmware during LP2 entry procedure, after all traffic and refresh has been stopped. Cleared by firmware during LP2 exit procedure.
1	ROX	MBARPC0Q_CFG_LP2_STATE: Read only status bit; set by hardware when cfg_lp2_entry_req is active AND all ranks are powered down; reset by hardware when cfg_lp2_entry_req is reset
2	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS_ENABLE: This is an overall enable for power domain control. If power control is disabled, the CKEs will always be set to a '1'.
3:5	RW	MBARPC0Q_CFG_MIN_MAX_DOMAINS: Maxall_minall means power control will not limit the number of domains accessible at a given time. Power domains will not be powered down even if they go idle, unless min_domain_reduction is enabled. Maxall_minx will permit idle power down to reduce the number of domains powered up once a domain has gone idle, but it won't restrict the maximum domains powered up. Max1_minx restricts the number of domains that can be powered up at a given time to 1. Values: MAXALL_MINALL=>0b000 MAXALL_MIN1=>0b001 MAXALL_MIN0=>0b010 MAX1_MIN1=>0b011 MAX1_MIN0=>0b100
6:10	RW	MBARPC0Q_CFG_PUP_AVAIL: Specifies how many DRAM command clocks for power control to wait from CKE going high to activate
11:15	RW	MBARPC0Q_CFG_PDN_PUP: Specifies how many DRAM command clocks for power control to wait from CKE going low to high again (enforces minimum time in power down)
16:20	RW	MBARPC0Q_CFG_PUP_PDN: Specifies how many DRAM command clocks for power control to wait from CKE going high to low again (enforces minimum time powered up)
21	RW	MBARPC0Q_RESERVED_21: Reserved
22	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_ENABLE: This allows a dynamic reduction of the minimum domains to 0 when no memory traffic has been seen over the specified cfg_min_domain_reduction_time; min domains will be restored once traffic is seen; the adjusted min domains won't be reflected in or over-write the cfg_min_max_domains setting (adjustment made internal to logic).
23:32	RW	MBARPC0Q_CFG_MIN_DOMAIN_REDUCTION_TIME: Specifies how many DRAM command clocks the MBA must be idle before min_cke is reduced to 0.
33	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_ENABLE: Once a configurable time has been met since the last activate, a subsequent domain can be powered up, even if the powering-down domain has not been powered down yet.
34:41	RW	MBARPC0Q_CFG_PUP_AFTER_ACTIVATE_WAIT_TIME: Specifies how many DRAM command clocks the MBA must be idle before minimum domains is reduced to 0.
42	RW	MBARPC0Q_CFG_FORCE_SPARE_PUP: Forces all spare CKEs to couple with their respective primary CKEs. This bit should not be toggled during runtime or when calibration is enabled.
43:63	RW	MBARPC0Q_RESERVED_43_63: Reserved

Register Name	***Rank-to-CKE Power Domain Mapping Table***
Mnemonic	MBU.MBA23.MBA_SRQ.PC.MBARPC1Q
Address	0000000003010C35 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBARPC1Q_CFG_MRNK0_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1

Bits	SCOM	Field Mnemonic: Description
4:7	RW	MBARPC1Q_CFG_MRNK1_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
8:11	RW	MBARPC1Q_CFG_MRNK2_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
12:15	RW	MBARPC1Q_CFG_MRNK3_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
16:19	RW	MBARPC1Q_CFG_MRNK4_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
20:23	RW	MBARPC1Q_CFG_MRNK5_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
24:27	RW	MBARPC1Q_CFG_MRNK6_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
28:31	RW	MBARPC1Q_CFG_MRNK7_RD_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
32:35	RW	MBARPC1Q_CFG_MRNK0_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
36:39	RW	MBARPC1Q_CFG_MRNK1_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
40:43	RW	MBARPC1Q_CFG_MRNK2_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
44:47	RW	MBARPC1Q_CFG_MRNK3_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
48:51	RW	MBARPC1Q_CFG_MRNK4_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
52:55	RW	MBARPC1Q_CFG_MRNK5_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
56:59	RW	MBARPC1Q_CFG_MRNK6_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1
60:63	RW	MBARPC1Q_CFG_MRNK7_WR_CKE: Bit0 is ma0_cntl_cke0 Bit1 is ma0_cntl_cke1 Bit2 is ma1_cntl_cke0 Bit3 is ma1_cntl_cke1

Register Name	***Refresh Avoidance Control Register***
Mnemonic	MBU.MBA23.MBA_SRQ.PC.MBAREFAQ
Address	0000000003010C36 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAREFAQ_CFG_REFRESH_LP_DYN_WAIT_ENABLE: When enabled, a low priority refresh wait function takes into account the power state of the rank, how long the rank has been idle and the rank's refresh backlog queue count when scheduling a low priority refresh. If disabled, a low priority refresh is scheduled once the read reorder queue has been idle for a programmable number of cycles.
1	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BIAS_ENABLE: When enabled, the refresh logic sends a signal to bias the prefetch and final arbitration logic ahead of issuing a high priority refresh.
2	RW	MBAREFAQ_CFG_REFRESH_HP_RANK_BLOCK_ENABLE: When enabled, the refresh logic sends a block signal when issuing a high priority refresh. The block signal prevents new demand requests to the refreshing rank from overwhelming the read reorder queue.
3	RW	MBAREFAQ_RESERVED_3: Reserved

Bits	SCOM	Field Mnemonic: Description
4:7	RW	MBAREFAQ_CFG_REFRESH_PUP_THRESHOLD: If cfg_refresh_lp_dyn_wait_enable=1, then the logic waits until the refresh backlog queue reaches this threshold before powering up to service a low priority refresh. If power control is disabled (rank never powered down), this setting becomes irrelevant as the rank will always be powered up, and the refresh will still be gated until the appropriate idle time has been met. This setting should not be set greater than cfg_priority_threshold (the refresh high priority threshold).
8:10	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ1_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
11:13	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ2_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
14:16	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ3_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
17:19	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ4_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
20:22	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ5_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111

Bits	SCOM	Field Mnemonic: Description
23:25	RW	MBAREFAQ_CFG_REFRESH_BLQ_EQ6_COEF: Values: 0=>0b000 0_125=>0b001 0_25=>0b010 0_5=>0b011 0_75=>0b100 1_0=>0b101 1_5=>0b110 2_0=>0b111
26:31	RW	MBAREFAQ_CFG_RRQ_REF_HINT_DLY: Programmable timer that determines the delay from the refresh pending backlog = HP threshold to the assertion of a scheduling hint to the read reorder queue to accommodate the impending high priority refresh. (B) NOTE: This delay counts in multiples of 4 DDR clocks (per default hp ref sub counter setting)
32:37	RW	MBAREFAQ_CFG_ASSERT_REFRESH_BLOCK_DLY: Programmable timer that determines the delay from the refresh pending backlog = HP threshold to where subsequent commands from MBS to the refresh rank are blocked. This must be greater than cfg_rrq_ref_hint_dly. (C) NOTE: This delay counts in multiples of 4 DDR clocks (per default hp ref sub counter setting)
38:43	RW	MBAREFAQ_CFG_FORCE_HP_REF_REQ_DLY: Programmable timer that determines the delay from the refresh pending backlog = HP threshold to where the refresh must be serviced by the final command arbiter. This must be greater than cfg_assert_refresh_block_dly. (D) NOTE: This delay counts in multiples of 4 DDR clocks (per default hp ref sub counter setting)
44:49	RW	MBAREFAQ_CFG_REF_BLOCK_STOP_DLY: Programmable setting which is subtracted from the tRFC timer. The result is used to determine when the block signal can be deasserted leading up to the end of a tRFC period. This allows new commands targeting the refresh domain being refreshed to progress to the rrq so that they are ready to go as soon as tRFC ends. (N)
50:63	RW	MBAREFAQ_RESERVED_50_63: Reserved

Register Name	***Performance Monitor Counts0***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU0Q
Address	0000000003010C37 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU0Q_READ_COUNT: Read count, increments every read, wraps
32:63	ROX	MBA_PMU0Q_WRITE_COUNT: Write count, increments every write, wraps

Register Name	***Performance Monitor Counts1***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU1Q
Address	0000000003010C38 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU1Q_ACTIVATE_COUNT: Bank activate count, increments for every activate , wraps
32:63	ROX	MBA_PMU1Q_PU_COUNTS: Counts the number of rising edges for a CKE, wraps

Register Name	***Performance Monitor Counts2***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU2Q
Address	0000000003010C39 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU2Q_FRAME_COUNT: Frame count, increments every dram clock(2:1) clock
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***Performance Monitor Counts4***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU3Q
Address	0000000003010C3A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	MBA_PMU3Q_LOW_IDLE_THRESHOLD: Each time the low idle (no reads or writes queued) threshold is met, the low idle count will increment; between periods of command activity, there may be multiple low-idle-threshold-width windows of command inactivity. For each of these windows, the low idle count will be incremented. (counts 2:1Dram addr frequency) counts MBA idle cycles
16:31	RW	MBA_PMU3Q_MED_IDLE_THRESHOLD: Each time the med idle (no reads or writes queued) threshold is met, the med idle count will increment; between periods of command activity, there may be multiple med-idle-threshold-width windows of command inactivity. For each of these windows, the med idle count will be incremented.
32:63	RW	MBA_PMU3Q_HIGH_IDLE_THRESHOLD: Each time the high idle (no reads or writes queued) threshold is met, the high idle count will increment; between periods of command activity, there may be multiple high-idle-threshold-width windows of command inactivity. For each of these windows, the high idle count will be incremented.

Register Name	***Performance Monitor Counts***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU4Q
Address	0000000003010C3B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU4Q_BASE_IDLE_COUNT: Increments every MBA idle cycle (counts 2:1Dram addr frequency)
32:63	ROX	MBA_PMU4Q_LOW_IDLE_COUNT: Counts the number of times the low idle threshold was met (counts 2:1Dram addr frequency)

Register Name	***Performance Monitor Counts***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU5Q
Address	0000000003010C3C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MBA_PMU5Q_MED_IDLE_COUNT: Counts the number of times the med idle threshold was met (counts 2:1Dram addr frequency)
32:63	ROX	MBA_PMU5Q_HIGH_IDLE_COUNT: Counts the number of times the high idle threshold was met (counts 2:1Dram addr frequency)

Register Name	***Performance Monitor Counts***
Mnemonic	MBU.MBA23.MBA_SRQ.MBA_PMU6Q
Address	0000000003010C3D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:17	RWX_WCLRPART	MBA_PMU6Q_TOTAL_GAP_COUNTS: Increments by 1 for any gap that is greater than or equal to the gap programmed by the gap length field (see bits 36-38 for info)
18:35	RWX_WCLRPART	MBA_PMU6Q_SPECIFIC_GAP_COUNT: Total number of gaps greater than or equal to gap length caused by reason specified in field 39:42.
36:38	RW	MBA_PMU6Q_GAP_LENGTH_ADDER: The gap length is this field +4. So a value of 0 will count gaps that occur every 4 cycles.
39:42	RW	MBA_PMU6Q_SPECIFIC_GAP_CONDITION: This field chooses the condition for the specific gap counter(18:35) refresh_busy => 0b0001; bank_busy => 0b0010; power_down_busy => 0b0011; high_priority_write => 0b0100; entry_0_HP => 0b0101; NM_busy => 0b0110; read_queue_empty => 0b0111; write_queue_empty => 0b1000; read_and_write_queue_empty => 0b1001; bg_busy => 0b1010; data_bus_busy => 0b1011; out_of_timers => 0b1100; Values: TFAW_BUSY=>0b0000 REFRESH_BUSY=>0b0001 BANK_BUSY=>0b0010 POWER_DOWN_BUSY=>0b0011 HIGH_PRIORITY_WRITE=>0b0100 ENTRY_0_HP=>0b0101 NM_BUSY=>0b0110 READ_QUEUE_EMPTY=>0b0111 WRITE_QUEUE_EMPTY=>0b1000 READ_AND_WRITE_QUEUE_EMPTY=>0b1001 BG_BUSY=>0b1010 DATA_BUS_BUSY=>0b1011 OUT_OF_TIMERS=>0b1100
43:60	RWX_WCLRPART	MBA_PMU6Q_CMD_TO_CMD_COUNT: Count the number of times the following command pattern occurs that is specified in bits 61:63.

Bits	SCOM	Field Mnemonic: Description
61:63	RW	MBA_PMU6Q_COMMAND_PATTERN_TO_COUNT: Type of command pattern for counter in bits 43:60 should count. Values: RWSM_READ_TO_WRITE_SAME_MASTER=>0b000 RWDM_READ_TO_WRITE_DIFFERENT_MASTER=>0b001 RWXX_READ_TO_WRITE=>0b010 WRSM_WRITE_TO_READ_SAME_MASTER=>0b011 WRDM_WRITE_TO_READ_DIFFERENT_MASTER=>0b100 WRXX_WRITE_TO_READ=>0b101 RRDM_READ_TO_READ_DIFFERENT_MASTER=>0b110 WWDM_WRITE_TO_WRITE_DIFFERENT_MASTER=>0b111

Register Name	***MBA Bit Steer Control Register 0***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS0
Address	0000000003010C40 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS0_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010

Bits	SCOM	Field Mnemonic: Description
5:9	RW	MBABS0_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001
10:15	RW	MBABS0_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9___X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8___X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7___X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6___X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5___X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4___X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3___X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2___X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1___X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 1***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS1
Address	0000000003010C41 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS1_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS1_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS1_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 2***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS2
Address	0000000003010C42 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS2_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS2_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS2_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 3***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS3
Address	0000000003010C43 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS3_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS3_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS3_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 4***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS4
Address	0000000003010C44 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS4_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS4_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS4_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 5***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS5
Address	0000000003010C45 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS5_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS5_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS5_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 6***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS6
Address	0000000003010C46 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS6_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS6_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS6_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Bit Steer Control Register 7***
Mnemonic	MBU.MBA23.MBA_WRD.MBABS7
Address	0000000003010C47 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBABS7_WRITE_BIT_STEER_MUX_SELECT_0: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP0=>0b00000 DRAM_17__X8___35__X4__READ_DATA_REPLACED_WITH_SP0=>0b00001 DRAM_16__X8___34__X4__READ_DATA_REPLACED_WITH_SP0=>0b00010 DRAM_15__X8___33__X4__READ_DATA_REPLACED_WITH_SP0=>0b00011 DRAM_14__X8___32__X4__READ_DATA_REPLACED_WITH_SP0=>0b00100 DRAM_13__X8___31__X4__READ_DATA_REPLACED_WITH_SP0=>0b00101 DRAM_12__X8___30__X4__READ_DATA_REPLACED_WITH_SP0=>0b00110 DRAM_11__X8___29__X4__READ_DATA_REPLACED_WITH_SP0=>0b00111 DRAM_10__X8___28__X4__READ_DATA_REPLACED_WITH_SP0=>0b01000 DRAM_1____X8___27__X4__READ_DATA_REPLACED_WITH_SP0=>0b01001 DRAM_26__X4__READ_DATA_REPLACED_WITH_SP0=>0b01010 DRAM_25__X4__READ_DATA_REPLACED_WITH_SP0=>0b01011 DRAM_24__X4__READ_DATA_REPLACED_WITH_SP0=>0b01100 DRAM_23__X4__READ_DATA_REPLACED_WITH_SP0=>0b01101 DRAM_22__X4__READ_DATA_REPLACED_WITH_SP0=>0b01110 DRAM_21__X4__READ_DATA_REPLACED_WITH_SP0=>0b01111 DRAM_20__X4__READ_DATA_REPLACED_WITH_SP0=>0b10000 DRAM_3____X4__READ_DATA_REPLACED_WITH_SP0=>0b10001 DRAM_2____X4__READ_DATA_REPLACED_WITH_SP0=>0b10010
5:9	RW	MBABS7_WRITE_BIT_STEER_MUX_SELECT_1: x4 x8 DRAM mode: Values: NO_SPARING_USING_SP1=>0b00000 DRAM_9__X8___19__X4__READ_DATA_REPLACED_WITH_SP1=>0b00001 DRAM_8__X8___18__X4__READ_DATA_REPLACED_WITH_SP1=>0b00010 DRAM_7__X8___17__X4__READ_DATA_REPLACED_WITH_SP1=>0b00011 DRAM_6__X8___16__X4__READ_DATA_REPLACED_WITH_SP1=>0b00100 DRAM_5__X8___15__X4__READ_DATA_REPLACED_WITH_SP1=>0b00101 DRAM_4__X8___14__X4__READ_DATA_REPLACED_WITH_SP1=>0b00110 DRAM_3__X8___13__X4__READ_DATA_REPLACED_WITH_SP1=>0b00111 DRAM_2__X8___12__X4__READ_DATA_REPLACED_WITH_SP1=>0b01000 DRAM_0____X8___11__X4__READ_DATA_REPLACED_WITH_SP1=>0b01001 DRAM_10__X4__READ_DATA_REPLACED_WITH_SP1=>0b01010 DRAM_9__X4__READ_DATA_REPLACED_WITH_SP1=>0b01011 DRAM_8__X4__READ_DATA_REPLACED_WITH_SP1=>0b01100 DRAM_7__X4__READ_DATA_REPLACED_WITH_SP1=>0b01101 DRAM_6__X4__READ_DATA_REPLACED_WITH_SP1=>0b01110 DRAM_5__X4__READ_DATA_REPLACED_WITH_SP1=>0b01111 DRAM_4__X4__READ_DATA_REPLACED_WITH_SP1=>0b10000 DRAM_1__X4__READ_DATA_REPLACED_WITH_SP1=>0b10001

Bits	SCOM	Field Mnemonic: Description
10:15	RW	MBABS7_WRITE_BIT_STEER_MUX_SELECT_2: x4 DRAM mode: Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Bits	SCOM	Field Mnemonic: Description
16:63	RO	constant=0b00000000000000000000000000000000000000000000000000 Values: NO_SPARING_USING_SP=>0b000000 DRAM_35__X4__DATA_REPLACED_WITH_SP=>0b000001 DRAM_34__X4__DATA_REPLACED_WITH_SP=>0b000010 DRAM_33__X4__DATA_REPLACED_WITH_SP=>0b000011 DRAM_32__X4__DATA_REPLACED_WITH_SP=>0b000100 DRAM_31__X4__DATA_REPLACED_WITH_SP=>0b000101 DRAM_30__X4__DATA_REPLACED_WITH_SP=>0b000110 DRAM_29__X4__DATA_REPLACED_WITH_SP=>0b000111 DRAM_28__X4__DATA_REPLACED_WITH_SP=>0b001000 DRAM_27__X4__DATA_REPLACED_WITH_SP=>0b001001 DRAM_26__X4__DATA_REPLACED_WITH_SP=>0b001010 DRAM_25__X4__DATA_REPLACED_WITH_SP=>0b001011 DRAM_24__X4__DATA_REPLACED_WITH_SP=>0b001100 DRAM_23__X4__DATA_REPLACED_WITH_SP=>0b001101 DRAM_22__X4__DATA_REPLACED_WITH_SP=>0b001110 DRAM_21__X4__DATA_REPLACED_WITH_SP=>0b001111 DRAM_20__X4__DATA_REPLACED_WITH_SP=>0b010000 DRAM_19__X4__DATA_REPLACED_WITH_SP=>0b010001 DRAM_18__X4__DATA_REPLACED_WITH_SP=>0b010010 DRAM_17__X4__DATA_REPLACED_WITH_SP=>0b010011 DRAM_16__X4__DATA_REPLACED_WITH_SP=>0b010100 DRAM_15__X4__DATA_REPLACED_WITH_SP=>0b010101 DRAM_14__X4__DATA_REPLACED_WITH_SP=>0b010110 DRAM_13__X4__DATA_REPLACED_WITH_SP=>0b010111 DRAM_12__X4__DATA_REPLACED_WITH_SP=>0b011000 DRAM_11__X4__DATA_REPLACED_WITH_SP=>0b011001 DRAM_10__X4__DATA_REPLACED_WITH_SP=>0b011010 DRAM__9__X4__DATA_REPLACED_WITH_SP=>0b011011 DRAM__8__X4__DATA_REPLACED_WITH_SP=>0b011100 DRAM__7__X4__DATA_REPLACED_WITH_SP=>0b011101 DRAM__6__X4__DATA_REPLACED_WITH_SP=>0b011110 DRAM__5__X4__DATA_REPLACED_WITH_SP=>0b011111 DRAM__4__X4__DATA_REPLACED_WITH_SP=>0b100000 DRAM__3__X4__DATA_REPLACED_WITH_SP=>0b100001 DRAM__2__X4__DATA_REPLACED_WITH_SP=>0b100010 DRAM__1__X4__DATA_REPLACED_WITH_SP=>0b100011

Register Name	***MBA Error Injection***
Mnemonic	MBU.MBA23.MBA_WRD.MBA_INJQ
Address	0000000003010C48 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBA_INJQ_CFG_RDTAG_ERR_INJ: Self resetting bit. Writing a one will send a rdtag error inject pulse. After the pulse is sent it will be reset to 0
1	RWX	MBA_INJQ_CFG_RRQ_POP_ERR_INJ: Self resetting bit. Writing a one will send a rrq pop error inject pulse. After the pulse is sent it will be reset to 0
2	RW	MBA_INJQ_CFG_WR_ECC_INJ_MODE: Inject mode for write data ECC injection. Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	MBA_INJQ_CFG_WR_ECC_ERR_INJ: Inject enable. The write inject type (CE, UE, etc..) and specific write data bit(s) corrupted are indicated by the MBA Error Control Register. For single shot mode, bit must be cleared and re-set to enable another error inject. For continuous mode, error injection will occur on valid operations until bit is cleared.

Bits	SCOM	Field Mnemonic: Description
4	RW	MBA_INJQ_CFG_WRD_BUFF_INJ_MODE: Inject mode for write re-order data buffer ECC Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
5	RW	MBA_INJQ_CFG_WRD_BUFFER_CE_INJ: Inject CE error into write reorder data buffer. For single shot mode, but must be cleared and reset to enable another error inject. For continuous mode, error injection will occur on valid operations until bit is cleared. Values: NO_CE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER=>0b0 CE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER_BASED_ON_INJ_MODE=>0b1
6	RW	MBA_INJQ_CFG_WRD_BUFFER_UE_INJ: Inject UE error into write reorder data buffer. For single shot mode, but must be cleared and reset to enable another error inject. For continuous mode, error injection will occur on valid operations until bit is cleared. Values: NO_UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER=>0b0 UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER_BASED_ON_INJ_MODE=>0b1
7:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000 Values: NO_UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER=>0b0 UE_ECC_INJECT_INTO_WRITE_REORDER_DATA_BUFFER_BASED_ON_INJ_MODE=>0b1

Register Name	***MBA WRD Mode***
Mnemonic	MBU.MBA23.MBA_WRD.MBA_WRD_MODE
Address	0000000003010C49 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBA_WRD_MODE_CFG_WRD_ECC_CHK_DISABLE: Set to disable 8B ECC checking on WRD data bus.
1	RW	MBA_WRD_MODE_CFG_WRD_ECC_COR_DISABLE: Set to disable 8B ECC correction on WRD data bus.
2:4	RW	MBA_WRD_MODE_ECC_METADATA_MODE: Number of metadata in 65th byte. Values: 0_METADATA_8_CHECKBITS=>0b000 1_METADATA_7_CHECKBITS=>0b100 2_METADATA_6_CHECKBITS=>0b010 6_METADATA_2_CHECKBITS___DEFAULT_FOR_VENICE__CENTAUR__=>0b011
5	RW	MBA_WRD_MODE_CFG_MAINT_ECC_CHK_DISABLE: Set to disable 8B ECC checking on maintenance buffer output.
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Fault Isolation Register (MBAFIR)***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBAFIRQ
Address	0000000003010E00 (SCOM) 0000000003010E01 (SCOM1) 0000000003010E02 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBAFIRQ_INVALID_MAINT_CMD: Invalid Maintenance Command This bit is set when a maintenance command is started with an invalid maintenance command code entered in MBMCT
1	RWX	WOX_AND	WOX_OR	MBAFIRQ_INVALID_MAINT_ADDRESS: Invalid Maintenance Address This bit is set when a maintenance command is started when an invalid address is detected for a single or multiple address command
2	RWX	WOX_AND	WOX_OR	MBAFIRQ_MULTI_ADDRESS_MAINT_TIMEOUT: Maintenance Timeout This bit is set when a single maintenance operation (part of a mult-address maintenance op) does not complete in TBD time. (recommend > 100mS) - extra credit, implement if time allows
3	RWX	WOX_AND	WOX_OR	MBAFIRQ_INTERNAL_FSM_ERROR: Internal FSM Error A parity error occurred on an internal FSM
4	RWX	WOX_AND	WOX_OR	MBAFIRQ_MCBIST_ERROR: MCBIST Error This bit is set when MCBIST has detected an error while running its test.
5	RWX	WOX_AND	WOX_OR	MBAFIRQ_SCOM_CMD_REG_PE: SCOM Command Register Parity Errors Parity Error occurred on a scom command register
6	RWX	WOX_AND	WOX_OR	MBAFIRQ_CHANNEL_CHKSTP_ERR: Channel Checkstop Errors Errors that would lead to a channel checkstop.
7	RWX	WOX_AND	WOX_OR	MBAFIRQ_WRD_CAW2_DATA_CE_UE_ERR: UE or CE Error in WRD caw2 data latches
8:14	RWX	WOX_AND	WOX_OR	MBAFIRQ_RESERVED_8_14: RESERVED
15	RWX	WOX_AND	WOX_OR	MBAFIRQ_INTERNAL_SCOM_ERROR: Internal Scom Error
16	RWX	WOX_AND	WOX_OR	MBAFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal Som Error Clone
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBA Fault Isolation Mask Register (MBAFIRMASK)*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBAFIRMASK
Address	0000000003010E03 (SCOM) 0000000003010E04 (SCOM1) 0000000003010E05 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MBAFIRMASK_INVALID_MAINT_CMD: Masks FIR(0)
1	RW	WO_AND	WO_OR	MBAFIRMASK_INVALID_MAINT_ADDRESS: Masks FIR(1)
2	RW	WO_AND	WO_OR	MBAFIRMASK_MULTI_ADDRESS_MAINT_TIMEOUT: Masks FIR(2)
3	RW	WO_AND	WO_OR	MBAFIRMASK_INTERNAL_FSM_ERROR: Masks FIR(3)
4	RW	WO_AND	WO_OR	MBAFIRMASK_MCBIST_ERROR: Masks FIR(4)
5	RW	WO_AND	WO_OR	MBAFIRMASK_SCOM_CMD_REG_PE: Masks FIR(5)
6	RW	WO_AND	WO_OR	MBAFIRMASK_CHANNEL_CHKSTP_ERR: Masks FIR(6)
7	RW	WO_AND	WO_OR	MBAFIRMASK_WRD_CAW2_DATA_CE_UE_ERR: Masks FIR(7)
8:14	RW	WO_AND	WO_OR	MBAFIRMASK_RESERVED_8_14: RESERVED
15	RW	WO_AND	WO_OR	MBAFIRMASK_INTERNAL_SCOM_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	MBAFIRMASK_INTERNAL_SCOM_ERROR_CLONE: Masks FIR(16)

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
17:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBA Fault Isolation Action0 Register (MBAFIRACT0)*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBAFIRACT0
Address	0000000003010E06 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAFIRACT0_INVALID_MAINT_CMD: Action 0 FIR(0)
1	RW	MBAFIRACT0_INVALID_MAINT_ADDRESS: Action 0 FIR(1)
2	RW	MBAFIRACT0_MULTI_ADDRESS_MAINT_TIMEOUT: Action 0 FIR(2)
3	RW	MBAFIRACT0_INTERNAL_FSM_ERROR: Action 0 FIR(3)
4	RW	MBAFIRACT0_MCBIST_ERROR: Action 0 FIR(4)
5	RW	MBAFIRACT0_SCOM_CMD_REG_PE: Action 0 FIR(5)
6	RW	MBAFIRACT0_CHANNEL_CHKSTP_ERR: Action 0 FIR(6)
7	RW	MBAFIRACT0_WRD_CAW2_DATA_CE_UE_ERR: Action 0 FIR(7)
8:14	RW	MBAFIRACT0_RESERVED_8_14: RESERVED
15	RW	MBAFIRACT0_INTERNAL_SCOM_ERROR: Action 0 FIR(15)
16	RW	MBAFIRACT0_INTERNAL_SCOM_ERROR_CLONE: Action 0 FIR(16)
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBA Fault Isolation Action1 Register (MBAFIRACT1)*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBAFIRACT1
Address	0000000003010E07 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBAFIRACT1_INVALID_MAINT_CMD: Action 1 FIR(0)
1	RW	MBAFIRACT1_INVALID_MAINT_ADDRESS: Action 1 FIR(1)
2	RW	MBAFIRACT1_MULTI_ADDRESS_MAINT_TIMEOUT: Action 1 FIR(2)
3	RW	MBAFIRACT1_INTERNAL_FSM_ERROR: Action 1 FIR(3)
4	RW	MBAFIRACT1_MCBIST_ERROR: Action 1 FIR(4)
5	RW	MBAFIRACT1_SCOM_CMD_REG_PE: Action 1 FIR(5)
6	RW	MBAFIRACT1_CHANNEL_CHKSTP_ERR: Action 1 FIR(6)
7	RW	MBAFIRACT1_WRD_CAW2_DATA_CE_UE_ERR: Action 1 FIR(7)
8:14	RW	MBAFIRACT1_RESERVED_8_14: RESERVED
15	RW	MBAFIRACT1_INTERNAL_SCOM_ERROR: Action 1 FIR(15)
16	RW	MBAFIRACT1_INTERNAL_SCOM_ERROR_CLONE: Action 1 FIR(16)

Bits	SCOM	Field Mnemonic: Description
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBA Fault Isolation WOF Register (MBAFIRWOF)*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBAFIRWOF
Address	0000000003010E08 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBAFIRWOF_INVALID_MAINT_CMD: Who's On First (WOF0) Register
1	ROX	MBAFIRWOF_INVALID_MAINT_ADDRESS: Who's On First (WOF1) Register
2	ROX	MBAFIRWOF_MULTI_ADDRESS_MAINT_TIMEOUT: Who's On First (WOF2) Register
3	ROX	MBAFIRWOF_INTERNAL_FSM_ERROR: Who's On First (WOF3) Register
4	ROX	MBAFIRWOF_MCBIST_ERROR: Who's On First (WOF4) Register
5	ROX	MBAFIRWOF_SCOM_CMD_REG_PE: Who's On First (WOF5) Register
6	ROX	MBAFIRWOF_CHANNEL_CHKSTP_ERR: Who's On First (WOF6) Register
7	ROX	MBAFIRWOF_WRD_CAW2_DATA_CE_UE_ERR: Who's On First (WOF7) Register
8:14	ROX	MBAFIRWOF_RESERVED_8_14: RESERVED
15	ROX	MBAFIRWOF_INTERNAL_SCOM_ERROR: Who's On First (WOF15) Register
16	ROX	MBAFIRWOF_INTERNAL_SCOM_ERROR_CLONE: Who's On First (WOF16) Register
17:63	RO	constant=0b00000000000000000000000000000000000000000000000000000

Register Name	*MBA Maintenance Command Type Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBMCTQ
Address	0000000003010E0A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	MBMCTQ_MAINT_CMD_TYPE: Maintenance Command Type Values: TIMEBASE_READ=>0b00000 TIMEBASE_SCRUB=>0b00001 TIMEBASE_STEER_CLEANUP=>0b00010 TIMEBASE_INIT=>0b00011 TIMEBASE_RANDOM_INIT=>0b00100 SUPERFAST_READ=>0b01000 SUPERFAST_INIT=>0b01001 SUPERFAST_RANDOM_INIT=>0b01010 MEMORY_DISPLAY=>0b10000 MEMORY_ALTER=>0b10001 MEMORY_ALTER_WITH_ECC_OVERRIDE=>0b10010 ATOMIC_ALTER_ERROR_INJECT=>0b10011 INCREMENT_MBMACA_ADDRESS=>0b10100
5	RW	MBMCTQ_SF_INCREMENT_MODE: Superfast Address Increment Mode (valid for all maint cmd types) 0 - non superfast addressing mode 1 - Superfast addressing mode

Bits	SCOM	Field Mnemonic: Description
6	RW	MBMCTQ_BURST_WINDOW_SEL: Burst Window Select 0 - 512 Maint Clks 1 - 536870912 Maint Clks
7:8	RW	MBMCTQ_RESERVED_7_8: Reserved
9:10	RW	MBMCTQ_TIMEBASE_SEL: Time base Select Values: 1_MAINT_CLK=>0b00 8192_MAINT_CLKS=>0b01
11	RW	MBMCTQ_TIMEBASE_BURST_SEL: Time base burst select 0 - disable burst mode 1 - enable burst mode: MBMCT(12:23) = operation interval, MBMCT(24:31) = burst window length, MBMCT(32:39) = burst interval
12:23	RW	MBMCTQ_TIMEBASE_INTERVAL: Time Base interval The operation interval for Timebase operations equals the time base x MBMCT(12:23). The time base is selected by bits 9 and 10 above.
24:31	RW	MBMCTQ_BURST_WINDOW: Burst window The burst window for timebase operations with burst mode enabled equals the time base x MBMCT(24:31). The time base is selected by bits 6 above.
32:39	RW	MBMCTQ_BURST_INTERVAL: burst interval The burst interval for timebase operations with burst mode enabled equals the number of burst windows that will have no operations occurring in them.
40:63	RO	constant=0b000000000000000000000000

Register Name	***MBA Maintenance Command Control Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBMCCQ
Address	0000000003010E0B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMCCQ_MAINT_CMD_START: Maintenance Command Start When set, the maintenance op specified in MBMCT is started. Bit is reset by hardware.
1	RWX	MBMCCQ_MAINT_CMD_STOP: Maintenance Command Stop When set, the maintenance op currently running is stopped. Bit is reset by hardware. The maintenance command will stop after the next memory operation.
2:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Maintenance Command Status Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBMSRQ
Address	0000000003010E0C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MBMSRQ_MAINT_CMD_IP: Maintenance Command in Progress (RW) Status bit, is set by hardware when maintenance command is in progress and reset by hardware when maintenance command is complete.
1:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*MBA Maintenance Command Address Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBMACAQ
Address	0000000003010E0D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	MBMACAQ_CMD_MASTER_RANK: Master Rank Master rank address for memory operations. For Memory Buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RWX	MBMACAQ_CMD_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RWX	MBMACAQ_CMD_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0
11:27	RWX	MBMACAQ_CMD_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RWX	MBMACAQ_CMD_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40:46	RWX	MBMACAQ_CMD_ERR_STATUS: Error Status bits These bits are set to indicate the error conditions that occurred when a stop on error condition has been detected. The address associated with these error status bits are contained in bits 0:39 as described above. 40: NCE 41: SCE 42: MCE 43: RCE 44: MPE 45: SUE 46: UE Note: multiple error status bits may be set due to unique errors on each 64 byte pieces of read data. Note: the error status bits are only set when a stop-on-error condition is detected, and are reloaded on the next stop-on-error condition
47:58	RWX	MBMACAQ_MRANK_SCRUBED: Master Rank Scrubbed bits These bits indicate which master ranks have been scrubbed at least 1 times. User must manually reset these bits buy writing 0's to them. Salerno Mode 0 - slot 0 master rank 0 scrubbed 1 - slot 0 master rank 1 scrubbed 2 - slot 0 master rank 2 scrubbed 3 - slot 0 master rank 3 scrubbed 4 - slot 1 master rank 0 scrubbed 5 - slot 1 master rank 1 scrubbed 6 - slot 1 master rank 2 scrubbed 7 - slot 1 master rank 3 scrubbed 8 - slot 2 master rank 0 scrubbed 9 - slot 2 master rank 1 scrubbed 10 - slot 2 master rank 2 scrubbed 11 - slot 2 master rank 3 scrubbed Memory Buffer Mode 0 - mrank 0 scrubbed 1 - mrank 1 scrubbed 2 - mrank 2 scrubbed 3 - mrank 3 scrubbed 4 - mrank 4 scrubbed 5 - mrank 5 scrubbed 6 - mrank 6 scrubbed 7 - mrank 7 scrubbed 8 - unused 9 - unused 10 -unused 11 - unused
59:63	RO	constant=0b00000

Register Name	*MBA Maintenance Command End Address Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBMEAQ
Address	0000000003010E0E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MBMEAQ_END_MASTER_RANK: Master Rank Master rank address for memory operations. For Memory Buffer Master_rank(0) is a don't care Master_rank(1:3) is the master rank addr For Salerno Master_rank(0:1) is the slot number Master_rank(2:3) is the master rank addr
4:6	RW	MBMEAQ_END_SLAVE_RANK: Slave Rank Slave rank address for memory operations.
7:10	RW	MBMEAQ_END_BANK: Bank bank address for memory operations. For DDR3: Bank(7) is a don;t care and Bank(8:10) maps to DRAM bank address b2,b1,b0. For DDR4: Bank(7:8) maps to DRAM bank group address bg1,bg0 and Bank(9:10) maps to DRAM bank address b1,b0

Bits	SCOM	Field Mnemonic: Description
11:27	RW	MBMEAQ_END_ROW: Row row address for memory operations. ROW(11:26) maps to DRAM row address r16 - r0.
28:39	RW	MBMEAQ_END_COL: Col Note for DDR3 write burst order must be sequential so low order bits are tied to 0 in hardware. COL(28 - 39) maps to DRAM column address (c13,c11,c9 - c3) (c2, c1, and c0 are tied to 0).
40:63	RO	constant=0b000000000000000000000000

Register Name	***MBA Memory Scrub/Read Control Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBASCTLQ
Address	0000000003010E0F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBASCTLQ_STOP_ETE_NOW: Stop on ete immediate, attention set when ete occurs When set, a scrubread op will immediately stop when an Error Threshold Equal (ETE) condition is detected.
1	RW	MBASCTLQ_STOP_ETE_RANK_END: Stop on ete end of rank When set, a scrubread op will stop at the end of the current rank, when an Error Threshold Equal condition is detected. Attention is set at the end of the rank.
2	RW	MBASCTLQ_STOP_NCE_HARD: Stop on Hard NCE ETE When set, a scrubread op will stop (immediate or end of rank) when a Hard NCE threshold equal error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
3	RW	MBASCTLQ_STOP_NCE_INTERMITTENT: Stop on Intermittent NCE ETE When set, a scrubread op will stop (immediate or end of rank) when an Intermittent NCE threshold equal error is detected.. Stop immediately or at end of rank is determined with bits 0 and 1.
4	RW	MBASCTLQ_STOP_NCE_SOFT: Stop on Soft NCE ETE When set, a scrubread op will stop (immediate or end of rank) when a Soft NCE threshold equal error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
5	RW	MBASCTLQ_STOP_SCE: Stop on SCE When set, a scrubread op will stop (immediate or end of rank) when a SCE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
6	RW	MBASCTLQ_STOP_MCE: Stop on MCE When set, a scrubread op will stop (immediate or end of rank) when a MCE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
7	RW	MBASCTLQ_STOP_RETRYCE: Stop on Retry CE ETE When set, a scrubread op will stop (immediate or end of rank) when a Retry CE threshold equal error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
8	RW	MBASCTLQ_STOP_MPE: Stop on MPE When set, a scrubread op will stop (immediate or end of rank) when a Mark Place Error is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
9	RW	MBASCTLQ_STOP_UE: Stop on UE When set, a scrubread op will stop (immediate or end of rank) when a SD UE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.
10	RW	MBASCTLQ_STOP_ON_END_ADDRESS: Stop on End Address When set, any multi-address maintenance operation will stop when the MBMACA value equals the MBMEA (end address) value. When unset, it will continue to increment pass the end address.
11	RW	MBASCTLQ_ENABLE_ATT_MAINT_CMD_DONE: When set, the Maintenance Complete Attention is set when a maintenance operation stops (immediate or end of rank)
12	RW	MBASCTLQ_STOP_SUE: Stop on SUE When set, a scrubread op will stop (immediate or end of rank) when a SUE is detected. Stop immediately or at end of rank is determined with bits 0 and 1.

Bits	SCOM	Field Mnemonic: Description
13:14	RW	MBASCTLQ_CMD_TIMEOUT_SEL: Command Timeout Select - selects the time interval for a maint command to be sent out before it times out Values: 262144_CYCLES=>0b00 1048576_CYCLES=>0b01 2097152_CYCLES=>0b10 4194304_CYCLES=>0b11
15	RW	MBASCTLQ_RESET_KEEPER: Reset Keeper Writing this bit to 1 will pulse the reset of the hold latched in the MBA c_err_rpt's
16	RW	MBASCTLQ_MBSPA_BIT_0_MODE: MBSPA Bit 0 mode When unset, MBSPA(0) is set ONLY when a maintenance command completes successfully without hitting a stop-on-error condition. When set, MBSPA(0) is set when a maintenance command stops (whether from a command complete or stop-on-error condition).
17:63	RW	MBASCTLQ_RESERVED_17_63: Reserved

Register Name	***MBA Error Control Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBECTLQ
Address	0000000003010E10 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBECTLQ_ATOMIC_ALT_CE_INJ: Atomic Alter CE inject Used with the Atomic Alter Error Inject command to inject a CE error. When set, MBECTL(4:10) are used to select the symbol to be modified
1	RW	MBECTLQ_ATOMIC_ALT_CHIP_KILL_INJ: Atomic Alter Chip Kill inject Used with the Atomic Alter Error Inject command to inject a Mark Place error (MPE), or a Mark Correct Error (MCE), is a mark is already in place for the chip kill error being injected. When set, MBECTL(4:10) are used to select the mark to be modified
2	RW	MBECTLQ_ATOMIC_ALT_SD_UE_INJ: Atomic Alter UE inject Used with the Atomic Alter Error Inject command to inject a Slow Decoder UE. When set, bits 0 thru 9 of the first data beat will be inverted to create the UE
3	RW	MBECTLQ_ATOMIC_ALT_SUE_INJ: Atomic Alter Sue inject Used with the Atomic Alter Error Inject command to inject a SUE error. Turns on SUE bit in 65th byte.

Bits	SCOM	Field Mnemonic: Description
4:10	RW	MBECTLQ_ATOMIC_ALT_INJ_SYM_SEL: Atomic alter inject symbol select has 3 modes CE inject or Chip Kill (x4 mode) or Chip Kill (x8 mode) Values: INVERT_SYMBOL_0_OR_X4_OR_X8_CHIP_0_DATA_ON_WRITE=>0b0000000 INVERT_SYMBOL_1_OR_X4_OR_X8_CHIP_1_DATA_ON_WRITE=>0b0000001 INVERT_SYMBOL_2_OR_X4_OR_X8_CHIP_2_DATA_ON_WRITE=>0b0000010 INVERT_SYMBOL_3_OR_X4_OR_X8_CHIP_3_DATA_ON_WRITE=>0b0000011 INVERT_SYMBOL_4_OR_X4_OR_X8_CHIP_4_DATA_ON_WRITE=>0b0000100 INVERT_SYMBOL_5_OR_X4_OR_X8_CHIP_5_DATA_ON_WRITE=>0b0000101 INVERT_SYMBOL_6_OR_X4_OR_X8_CHIP_6_DATA_ON_WRITE=>0b0000110 INVERT_SYMBOL_7_OR_X4_OR_X8_CHIP_7_DATA_ON_WRITE=>0b0000111 INVERT_SYMBOL_8_OR_X4_OR_X8_CHIP_8_DATA_ON_WRITE=>0b0001000 INVERT_SYMBOL_9_OR_X4_OR_X8_CHIP_9_DATA_ON_WRITE=>0b0001001 INVERT_SYMBOL_10_OR_X4_OR_X8_CHIP_10_DATA_ON_WRITE=>0b0001010 INVERT_SYMBOL_11_OR_X4_OR_X8_CHIP_11_DATA_ON_WRITE=>0b0001011 INVERT_SYMBOL_12_OR_X4_OR_X8_CHIP_12_DATA_ON_WRITE=>0b0001100 INVERT_SYMBOL_13_OR_X4_OR_X8_CHIP_13_DATA_ON_WRITE=>0b0001101 INVERT_SYMBOL_14_OR_X4_OR_X8_CHIP_14_DATA_ON_WRITE=>0b0001110 INVERT_SYMBOL_15_OR_X4_OR_X8_CHIP_15_DATA_ON_WRITE=>0b0001111 INVERT_SYMBOL_16_OR_X4_OR_X8_CHIP_16_DATA_ON_WRITE=>0b0010000 INVERT_SYMBOL_17_OR_X4_OR_X8_CHIP_17_DATA_ON_WRITE=>0b0010001 INVERT_SYMBOL_18_OR_X4_CHIP_18_DATA_ON_WRITE=>0b0010010 INVERT_SYMBOL_19_OR_X4_CHIP_19_DATA_ON_WRITE=>0b0010011 INVERT_SYMBOL_20_OR_X4_CHIP_20_DATA_ON_WRITE=>0b0010100 INVERT_SYMBOL_21_OR_X4_CHIP_21_DATA_ON_WRITE=>0b0010101 INVERT_SYMBOL_22_OR_X4_CHIP_22_DATA_ON_WRITE=>0b0010110 INVERT_SYMBOL_23_OR_X4_CHIP_23_DATA_ON_WRITE=>0b0010111 INVERT_SYMBOL_24_OR_X4_CHIP_24_DATA_ON_WRITE=>0b0011000 INVERT_SYMBOL_25_OR_X4_CHIP_25_DATA_ON_WRITE=>0b0011001 INVERT_SYMBOL_26_OR_X4_CHIP_26_DATA_ON_WRITE=>0b0011010 INVERT_SYMBOL_27_OR_X4_CHIP_27_DATA_ON_WRITE=>0b0011011 INVERT_SYMBOL_28_OR_X4_CHIP_28_DATA_ON_WRITE=>0b0011100 INVERT_SYMBOL_29_OR_X4_CHIP_29_DATA_ON_WRITE=>0b0011101 INVERT_SYMBOL_30_OR_X4_CHIP_30_DATA_ON_WRITE=>0b0011110 INVERT_SYMBOL_31_OR_X4_CHIP_31_DATA_ON_WRITE=>0b0011111 INVERT_SYMBOL_32_OR_X4_CHIP_32_DATA_ON_WRITE=>0b0100000 INVERT_SYMBOL_33_OR_X4_CHIP_33_DATA_ON_WRITE=>0b0100001 INVERT_SYMBOL_34_OR_X4_CHIP_34_DATA_ON_WRITE=>0b0100010 INVERT_SYMBOL_35_OR_X4_CHIP_35_DATA_ON_WRITE=>0b0100011 INVERT_SYMBOL_36_DATA_ON_WRITE=>0b0100100 INVERT_SYMBOL_37_DATA_ON_WRITE=>0b0100101 INVERT_SYMBOL_38_DATA_ON_WRITE=>0b0100110 INVERT_SYMBOL_39_DATA_ON_WRITE=>0b0100111 INVERT_SYMBOL_40_DATA_ON_WRITE=>0b0101000 INVERT_SYMBOL_41_DATA_ON_WRITE=>0b0101001 INVERT_SYMBOL_42_DATA_ON_WRITE=>0b0101010 INVERT_SYMBOL_43_DATA_ON_WRITE=>0b0101011 INVERT_SYMBOL_44_DATA_ON_WRITE=>0b0101100 INVERT_SYMBOL_45_DATA_ON_WRITE=>0b0101101 INVERT_SYMBOL_46_DATA_ON_WRITE=>0b0101110 INVERT_SYMBOL_47_DATA_ON_WRITE=>0b0101111 INVERT_SYMBOL_48_DATA_ON_WRITE=>0b0110000 INVERT_SYMBOL_49_DATA_ON_WRITE=>0b0110001 INVERT_SYMBOL_50_DATA_ON_WRITE=>0b0110010 INVERT_SYMBOL_51_DATA_ON_WRITE=>0b0110011 INVERT_SYMBOL_52_DATA_ON_WRITE=>0b0110100 INVERT_SYMBOL_53_DATA_ON_WRITE=>0b0110101 INVERT_SYMBOL_54_DATA_ON_WRITE=>0b0110110 INVERT_SYMBOL_55_DATA_ON_WRITE=>0b0110111 INVERT_SYMBOL_56_DATA_ON_WRITE=>0b0111000 INVERT_SYMBOL_57_DATA_ON_WRITE=>0b0111001 INVERT_SYMBOL_58_DATA_ON_WRITE=>0b0111010 INVERT_SYMBOL_59_DATA_ON_WRITE=>0b0111011 INVERT_SYMBOL_60_DATA_ON_WRITE=>0b0111100 INVERT_SYMBOL_61_DATA_ON_WRITE=>0b0111101 INVERT_SYMBOL_62_DATA_ON_WRITE=>0b0111110 INVERT_SYMBOL_63_DATA_ON_WRITE=>0b0111111

Bits	SCOM	Field Mnemonic: Description
11	RW	MBECTLQ_ATOMIC_ALT_INJ_DATA_SEL: Atomic Alter Error Inject Data Select 0 - error injected in 1st 64 bytes of data 1 - error injected in 2nd 64 bytes of data
12	RW	MBECTLQ_SCOM_CMD_REG_INJ_MODE: Parity Error inject mode into the Command SCOM (MBAFIR(5)) Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
13	RW	MBECTLQ_SCOM_CMD_REG_INJ: Parity Error inject mode into the Command SCOM (MBAFIR(5))
14	RW	MBECTLQ_SCOM_CFG_DATA_REG_INJ_MODE: Parity Error inject mode into the configuration and data SCOM (MBAFIR(6)) Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
15	RW	MBECTLQ_SCOM_CFG_DATA_REG_INJ: Parity Error inject mode into the configuration and data SCOM (MBAFIR(6))
16	RW	MBECTLQ_INTERNAL_FSM_INJ_MODE: Parity Error inject mode into the configuration and data SCOM (MBAFIR(3)) Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
17	RW	MBECTLQ_INTERNAL_REG_INJ: Parity Error inject mode into the configuration and data SCOM (MBAFIR(3))
18	RW	MBECTLQ_WRD_CAW2_UE_CE_DETECT: UE and CE detection on caw2 write data latch enable When enable, ECC will be checked at caw2 write data latches and SUE inject for any CE or UE errors detected Values: DISABLE_SUE_INJECTION_FOR_CE_AND_UE_ERRORS=>0b0 ENABLE_SUE_INJECTION_FOR_CE_AND_UE_ERRORS=>0b1
19:31	RW	MBECTLQ_RESERVED_19_31: Reserved
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***MBA Special Attention Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBSPAQ
Address	0000000003010E11 (SCOM) 0000000003010E12 (SCOM1) 0000000003010E13 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MBSPAQ_COMMAND_COMPLETE_WO_ENA_ERR_ATTN: maintenance command complete without enabled errors Set at the completion of a maintenance op, if the maintenance command did not stop due to a stop on error threshold or stop on maintenance memory error condition. If only non-enabled stop on threshold or error events occur during the execution of a maintenance command, the Command_Complete_Attn is set when the maintenance command completes. Maintenance stop conditions are specified in MBASCTLQ.
1	RWX	WOX_AND	WOX_OR	MBSPAQ_HARD_CE_ETE_ATTN: Hard NCE ETE Set if an error threshold condition is detected
2	RWX	WOX_AND	WOX_OR	MBSPAQ_SOFT_CE_ETE_ATTN: Soft NCE ETE Set if an error threshold condition is detected

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	MBSPAQ_INTERMITTENT_ETE_ATTN: Intermittent NCE ETE Set if an error threshold condition is detected
4	RWX	WOX_AND	WOX_OR	MBSPAQ_RCE_ETE_ATTN: Retry CE ETE Set if an error threshold condition is detected
5	RWX	WOX_AND	WOX_OR	MBSPAQ_EMERGENCY_THROTTLE_ATTN: Emergency throttle action detected Set if an emergency throttle command has been detected, power controls placed in 'safe' mode
6	RWX	WOX_AND	WOX_OR	MBSPAQ_FIRMWARE_ATTN0: Firmware generated attention0
7	RWX	WOX_AND	WOX_OR	MBSPAQ_FIRMWARE_ATTN1: Firmware generated attention1
8	RWX	WOX_AND	WOX_OR	MBSPAQ_WAT_DEBUG_ATTN: WAT Debug Bus Attention This is a way for the WAT debug bus to trigger an attention
9	RWX	WOX_AND	WOX_OR	MBSPAQ_SPARE_ATTN1: Spare1
10	RWX	WOX_AND	WOX_OR	MBSPAQ_MCBIST_DONE: MCBIST Done This bit is set when MCBIST had completed its testing.
11:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	***MBA Special Attention Mask Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBSPAMSKQ
Address	0000000003010E14 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MBSPAMSKQ_COMMAND_COMPLETE_WO_ENA_ERR_ATTN: Per Bit Mask for MBSPA(0)
1	RW	MBSPAMSKQ_HARD_CE_ETE_ATTN: Per Bit Mask for MBSPA(1)
2	RW	MBSPAMSKQ_SOFT_CE_ETE_ATTN: Per Bit Mask for MBSPA(2)
3	RW	MBSPAMSKQ_INTERMITTENT_ETE_ATTN: Per Bit Mask for MBSPA(3)
4	RW	MBSPAMSKQ_RCE_ETE_ATTN: Per Bit Mask for MBSPA(4)
5	RW	MBSPAMSKQ_EMERGENCY_THROTTLE_ATTN: Per Bit Mask for MBSPA(5)
6	RW	MBSPAMSKQ_FIRMWARE_ATTN0: Per Bit Mask for MBSPA(6)
7	RW	MBSPAMSKQ_FIRMWARE_ATTN1: Per Bit Mask for MBSPA(7)
8	RW	MBSPAMSKQ_WAT_DEBUG_ATTN: Per Bit Mask for MBSPA(8)
9	RW	MBSPAMSKQ_SPARE_ATTN1: Per Bit Mask for MBSPA(9)
10	RW	MBSPAMSKQ_MCBIST_DONE: Per Bit Mask for MBSPA(10)
11:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000

Register Name	***CCS Instruction Array 0 0***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_0
Address	0000000003010E15 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_0_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_0_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_0_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_0_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_0_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_0_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_0_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_0_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_0_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_0_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_0_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_0_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_0_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 1***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_1
Address	0000000003010E16 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_1_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_1_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_1_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_1_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_1_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_1_MA_B_CASN: DDR CAS#

Bits	SCOM	Field Mnemonic: Description
23	RW	CCS_INST_ARR0_1_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_1_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_1_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_1_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_1_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_1_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_1_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 2***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_2
Address	0000000003010E17 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_2_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_2_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_2_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_2_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_2_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_2_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_2_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_2_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_2_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_2_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_2_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_2_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_2_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 3***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_3
Address	0000000003010E18 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_3_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_3_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_3_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_3_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_3_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_3_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_3_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_3_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_3_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_3_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_3_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_3_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_3_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 4***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_4
Address	0000000003010E19 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_4_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_4_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_4_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_4_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_4_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_4_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_4_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_4_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_4_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_4_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_4_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_4_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_4_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 5*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_5
Address	0000000003010E1A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_5_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_5_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_5_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_5_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_5_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_5_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_5_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_5_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_5_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_5_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_5_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_5_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_5_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 6*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_6
Address	0000000003010E1B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_6_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_6_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_6_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_6_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_6_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_6_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_6_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_6_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_6_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_6_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_6_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_6_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_6_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 7***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_7
Address	0000000003010E1C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_7_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_7_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_7_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_7_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_7_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_7_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_7_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_7_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_7_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_7_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_7_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_7_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_7_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 8***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_8
Address	0000000003010E1D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_8_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_8_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_8_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_8_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_8_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_8_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_8_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_8_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_8_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_8_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_8_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_8_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_8_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 9***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_9
Address	0000000003010E1E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_9_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_9_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_9_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_9_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_9_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_9_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_9_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_9_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_9_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_9_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_9_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_9_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_9_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 10***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_10
Address	0000000003010E1F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_10_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_10_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_10_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_10_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_10_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_10_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_10_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_10_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_10_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_10_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_10_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_10_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_10_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 11*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_11
Address	0000000003010E20 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_11_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_11_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_11_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_11_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_11_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_11_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_11_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_11_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_11_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_11_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_11_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_11_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_11_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 12*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_12
Address	0000000003010E21 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_12_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_12_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_12_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_12_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_12_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_12_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_12_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_12_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_12_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_12_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_12_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_12_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_12_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 13***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_13
Address	0000000003010E22 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_13_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_13_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_13_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_13_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_13_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_13_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_13_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_13_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_13_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_13_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_13_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_13_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_13_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 14***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_14
Address	0000000003010E23 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_14_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_14_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_14_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_14_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_14_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_14_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_14_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_14_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_14_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_14_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_14_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_14_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_14_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 15***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_15
Address	0000000003010E24 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_15_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_15_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_15_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_15_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_15_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_15_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_15_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_15_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_15_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_15_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_15_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_15_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_15_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 16***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_16
Address	0000000003010E25 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_16_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_16_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_16_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_16_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_16_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_16_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_16_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_16_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_16_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_16_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_16_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_16_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_16_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 17*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_17
Address	0000000003010E26 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_17_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_17_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_17_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_17_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_17_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_17_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_17_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_17_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_17_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_17_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_17_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_17_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_17_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 18*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_18
Address	0000000003010E27 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_18_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_18_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_18_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_18_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_18_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_18_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_18_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_18_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_18_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_18_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_18_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_18_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_18_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 19***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_19
Address	0000000003010E28 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_19_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_19_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_19_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_19_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_19_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_19_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_19_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_19_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_19_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_19_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_19_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_19_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_19_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 20***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_20
Address	0000000003010E29 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_20_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_20_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_20_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_20_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_20_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_20_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_20_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_20_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_20_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_20_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_20_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_20_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_20_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 21***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_21
Address	0000000003010E2A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_21_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_21_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_21_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_21_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_21_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_21_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_21_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_21_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_21_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_21_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_21_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_21_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_21_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 22***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_22
Address	0000000003010E2B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_22_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_22_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_22_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_22_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_22_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_22_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_22_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_22_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_22_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_22_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_22_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_22_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_22_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 23*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_23
Address	0000000003010E2C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_23_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_23_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_23_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_23_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_23_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_23_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_23_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_23_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_23_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_23_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_23_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_23_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_23_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 24*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_24
Address	0000000003010E2D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_24_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_24_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_24_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_24_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_24_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_24_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_24_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_24_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_24_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_24_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_24_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_24_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_24_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 25***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_25
Address	0000000003010E2E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_25_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_25_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_25_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_25_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_25_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_25_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_25_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_25_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_25_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_25_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_25_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_25_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_25_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 26***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_26
Address	0000000003010E2F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_26_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_26_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_26_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_26_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_26_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_26_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_26_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_26_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_26_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares

Bits	SCOM	Field Mnemonic: Description
48:55	RW	CCS_INST_ARR0_26_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_26_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_26_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_26_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 27***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_27
Address	0000000003010E30 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_27_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_27_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_27_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_27_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_27_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_27_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_27_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_27_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_27_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_27_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_27_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step

Bits	SCOM	Field Mnemonic: Description
60	RW	CCS_INST_ARR0_27_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_27_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 28***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_28
Address	0000000003010E31 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_28_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_28_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_28_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_28_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_28_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_28_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_28_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_28_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_28_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_28_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_28_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_28_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_28_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 29*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_29
Address	0000000003010E32 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_29_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_29_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_29_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_29_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_29_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_29_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_29_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_29_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_29_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_29_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_29_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_29_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_29_RESERVED_61_63: Reserved

Register Name	*CCS Instruction Array 0 30*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_30
Address	0000000003010E33 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_30_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
16	RW	CCS_INST_ARR0_30_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_30_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_30_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_30_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_30_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_30_MA_B_WEN: DDR Write Enable (WE#)
24:31	RW	CCS_INST_ARR0_30_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_30_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_30_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_30_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_30_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_30_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 0 31***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR0_31
Address	0000000003010E34 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR0_31_MA_B_ADDRESS: DDR Row and Column Address (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1
16	RW	CCS_INST_ARR0_31_DDR_RESETN: DDR Resetn Only valid when bit 60 of the ccs_modeq is set to 1. Otherwise, ccs_modeq(24) will control the value of DDR Resetn.
17:19	RW	CCS_INST_ARR0_31_MA_B_BANK: DDR Bank Address For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
20	RW	CCS_INST_ARR0_31_MA_B_ACTIVATE: DDR4 Activate
21	RW	CCS_INST_ARR0_31_MA_B_RASN: DDR RAS#
22	RW	CCS_INST_ARR0_31_MA_B_CASN: DDR CAS#
23	RW	CCS_INST_ARR0_31_MA_B_WEN: DDR Write Enable (WE#)

Bits	SCOM	Field Mnemonic: Description
24:31	RW	CCS_INST_ARR0_31_MA_B_CKE: Memory Buffer Mode Port A DDR CKE(0:1) (ma0_cntl_cke(0:1), CKE(4:5) (ma1_cntl_cke(0:1), Port B DDR CKE(0:1) (mb0_cntl_cke(0:1), CKE(4:5) (mb1_cntl_cke(0:1) Note that Port A CKE(0:1) is copied to Port A CKE(2:3), Port A CKE(4:5) is copied to Port A CKE(6:7), Port B CKE(0:1) is copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7) when bit 26 of CCS_MODEQ is set. Salerno Mode CKE(0:1) is slot 0 CKE(2:3) is slot 1 CKE(4:5) is slot 2 CKE(6:7) are spares
32:47	RW	CCS_INST_ARR0_31_MA_B_CSN: Memory Buffer Mode Port A DDR CSN(0:3) ma0_cntl_csn(0:3) CSN(4:7) ma1_cntl_csn(0:3) Port B DDR CSN(0:3) mb0_cntl_csn(0:3) CSN(4:7) mb1_cntl_csn(0:3) Salerno Mode CSN(0:3) is slot 0 CSN(4:7) is slot 1 CSN(8:11) is slot 2 CSN(12:15) are spares
48:55	RW	CCS_INST_ARR0_31_MA_B_ODT: Memory Buffer Mode Port A ODT ODT(0:1) ma0_cntl_odt(0:1) ODT(0:1) ma1_cntl_odt(0:1) Port B ODT ODT(0:1) mb0_cntl_odt(0:1) ODT(0:1) mb1_cntl_odt(0:1) Salerno Mode ODT(0:1) is slot 0 ODT(2:3) is slot 1 ODT(4:5) is slot 2 ODT(6:7) are spares
56:59	RW	CCS_INST_ARR0_31_DDR_CALIBRATION_TYPE: Bits 0:1 define the calibration type. Bits 2:3 define the sub-type 0123 11xx Initial Calibration. Performs all of the following steps that are enabled via configuration register: SysclkRdclk alignment, DQS alignment, Read Eye MPR Centering, Write leveling, Write centering, Coarse rdwr alignment, Read Eye Custom Pattern Centering. 10xx Internal ZQ calibration (cal_rank ignored) 01xx External ZQ calbration. Requested rank is ZQ Cal'd 0000 Periodic Calibration. SysClkRdClk alignment Step 0001 Periodic Calibration: DQS alignment Step 0010 Periodic Calibration: Read Eye MPR Centering Step
60	RW	CCS_INST_ARR0_31_DDR_PARITY: DDR Parity Only valid when bit 61 of the ccs_modeq is set to 1. Otherwise, parity is calculated by the hardware.
61:63	RW	CCS_INST_ARR0_31_RESERVED_61_63: Reserved

Register Name	***CCS Instruction Array 1 0***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_0
Address	0000000003010E35 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_0_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_0_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_0_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_0_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_0_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_0_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_0_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_0_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 1*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_1
Address	0000000003010E36 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_1_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_1_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_1_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_1_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_1_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_1_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_1_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_1_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 2*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_2
Address	0000000003010E37 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_2_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_2_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_2_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_2_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_2_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_2_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_2_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_2_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 3*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_3
Address	0000000003010E38 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_3_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_3_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_3_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_3_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_3_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_3_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_3_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_3_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 4*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_4
Address	0000000003010E39 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_4_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_4_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_4_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_4_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_4_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_4_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_4_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_4_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 5*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_5
Address	0000000003010E3A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_5_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_5_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_5_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_5_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_5_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_5_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_5_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_5_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 6*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_6
Address	0000000003010E3B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_6_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_6_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_6_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_6_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_6_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_6_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_6_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_6_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 7*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_7
Address	0000000003010E3C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_7_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_7_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_7_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_7_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_7_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_7_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_7_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_7_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 8*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_8
Address	0000000003010E3D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_8_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_8_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_8_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_8_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_8_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_8_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_8_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_8_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 9*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_9
Address	0000000003010E3E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_9_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_9_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_9_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_9_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_9_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_9_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_9_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_9_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 10*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_10
Address	0000000003010E3F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_10_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_10_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_10_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_10_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_10_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_10_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_10_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_10_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 11*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_11
Address	0000000003010E40 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_11_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_11_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_11_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_11_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_11_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_11_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_11_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_11_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 12*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_12
Address	0000000003010E41 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_12_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_12_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_12_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_12_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_12_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_12_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_12_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_12_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 13*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_13
Address	0000000003010E42 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_13_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_13_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_13_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_13_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_13_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_13_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_13_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_13_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 14*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_14
Address	0000000003010E43 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_14_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_14_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_14_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_14_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_14_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_14_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_14_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_14_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 15*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_15
Address	0000000003010E44 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_15_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_15_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_15_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_15_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_15_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_15_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_15_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_15_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 16*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_16
Address	0000000003010E45 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_16_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_16_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_16_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_16_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_16_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_16_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_16_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_16_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 17*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_17
Address	0000000003010E46 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_17_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_17_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_17_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_17_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_17_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_17_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_17_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_17_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 18*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_18
Address	0000000003010E47 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_18_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_18_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_18_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_18_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_18_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_18_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_18_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_18_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 19*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_19
Address	0000000003010E48 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_19_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_19_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_19_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_19_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_19_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_19_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_19_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_19_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 20*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_20
Address	0000000003010E49 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_20_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_20_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_20_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_20_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_20_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_20_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_20_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_20_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 21*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_21
Address	0000000003010E4A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_21_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_21_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_21_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_21_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_21_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_21_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_21_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_21_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 22*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_22
Address	0000000003010E4B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_22_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_22_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_22_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_22_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_22_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_22_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_22_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_22_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 23*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_23
Address	0000000003010E4C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_23_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_23_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_23_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_23_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_23_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_23_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_23_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_23_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 24*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_24
Address	0000000003010E4D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_24_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_24_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_24_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_24_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_24_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_24_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_24_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_24_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	***CCS Instruction Array 1 25***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_25
Address	0000000003010E4E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_25_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_25_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_25_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_25_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_25_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_25_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_25_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_25_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	***CCS Instruction Array 1 26***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_26
Address	0000000003010E4F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_26_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_26_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_26_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_26_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_26_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_26_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_26_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_26_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 27*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_27
Address	0000000003010E50 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_27_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_27_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_27_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_27_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_27_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_27_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_27_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_27_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 28*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_28
Address	0000000003010E51 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_28_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_28_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_28_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_28_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_28_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_28_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_28_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_28_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	***CCS Instruction Array 1 29***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_29
Address	0000000003010E52 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_29_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_29_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_29_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_29_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_29_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_29_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_29_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_29_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	***CCS Instruction Array 1 30***
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_30
Address	0000000003010E53 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_30_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_30_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_30_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_30_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_30_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_30_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_30_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_30_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*CCS Instruction Array 1 31*
Mnemonic	MBU.MBA23.MBA_MCBIST.CCS.CCS_INST_ARR1_31
Address	0000000003010E54 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_INST_ARR1_31_IDLES: Number of Idle cycles before issuing next command
16:31	RW	CCS_INST_ARR1_31_REPEAT_CMD_CNT: Repeat this command this many times.
32:51	RW	CCS_INST_ARR1_31_READ_OR_WRITE_DATA: Write Data(0:19) if write command is coded up or Read Compare Byte if read command is coded up (Each bit represents a nibble of data)
52	RW	CCS_INST_ARR1_31_READ_COMPARE_REQUIRED: Set to 1b if this command is read and requires Data compare
53:56	RW	CCS_INST_ARR1_31_DDR_CAL_RANK: DDR Rank Address(0:3) to Calibrate
57	RW	CCS_INST_ARR1_31_DDR_CALIBRATION_ENABLE: Set to 1b to enable the calibration type in bit 56:59 in CCS Instruction Array 0
58	RW	CCS_INST_ARR1_31_CCS_END: Set to 1b if this is the last CCS command.
59:63	RW	CCS_INST_ARR1_31_GOTO_CMD: If CCS Instruction Array 1 bit 58 is 0b, Goto this command number next (after repeat count has expired).

Register Name	*Configured Command Sequence Control Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.CCS_CNTLQ
Address	0000000003010EA5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	CCS_CNTLQ_CCS_START: Start bit - Self resetting bit. Kicks off the CCS operation
1	RWX	CCS_CNTLQ_CCS_STOP: Stop bit - Self resetting bit. Stops Current CCS operation
2:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Configured Command Sequence Status Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.CCS_STATQ
Address	0000000003010EA6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	CCS_STATQ_CCS_IP: IP bit - Hdw sets to a '1'b when CCS run in progress
1	RWX	CCS_STATQ_CCS_DONE: Done bit - Hdw sets to a '1'b when CCS run complete
2	RWX	CCS_STATQ_CCS_FAIL: Fail bit - Hdw sets to a '1'b when CCS run failed
3:5	RWX	CCS_STATQ_CCS_FAIL_TYPE: Fail Type - Indicates type of CCS failure: Bit 3-> Read Miscompare Bit 4 -> UE or SUE Error Bit 5 -> Calibration operation times out

Bits	SCOM	Field Mnemonic: Description
6:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Configured Command Sequence Mode Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.CCS_MODEQ
Address	0000000003010EA7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	CCS_MODEQ_CCS_STOP_ON_ERR: User sets to a '1'b to tell the Hdw to stop CCS whenever failure occurs. When a '0'b, Hdw will continue CCS even if a failure occurs.
1	RW	CCS_MODEQ_CCS_UE_DISABLE: User sets to a '1'b to force the Hdw to ignore any array ue or sue errors during CCS command fetching.
2:3	RW	CCS_MODEQ_CCS_DATA_SEL: User sets to indicate which group of the data burst to compare. Values: DDR_BURST_1_AND_2=>0b00 DDR_BURST_3_AND_4=>0b01 DDR_BURST_5_AND_6=>0b10 DDR_BURST_7_AND_8=>0b11
4:5	RW	CCS_MODEQ_MCBIST_DDR_DPHY_NCLK: DDR Phy nclk control Values: PHY_NCLK_OUTPUT_DISABLED=>0b00 PHY_NCLK_OUTPUT_ENABLED=>0b01
6:7	RW	CCS_MODEQ_MCBIST_DDR_DPHY_PCLK: DDR Phy pclk control Values: PHY_PCLK_OUTPUT_DISABLED=>0b00 PHY_PCLK_OUTPUT_ENABLED=>0b10
8:23	RW	CCS_MODEQ_DDR_CAL_TIMEOUT_CNT: DDR calibration time counter - amount of time to wait for DDR calibration to complete. This value is multiplied by the factor in bits 30:31 to get the total timeout wait time.
24	RW	CCS_MODEQ_MCBIST_DDR_RESETN: DDR Resetn Signal
25	RW	CCS_MODEQ_MCBIST_DDR_DFI_RESET_RECOVER: DDR Reset Recover Signal
26	RW	CCS_MODEQ_COPY_CKE_TO_SPARE_CKE: Copy CKE signals to CKE Spare on both ports 0 - Spare CKEs not copied with values from CKE(0:1) and CKE(4:5) 1 - Port A CKE(0:1) copied to Port A CKE(2:3), Port A CKE(4:5) copied to Port A CKE(6:7), Port B CKE(0:1) copied to Port B CKE(2:3) and Port B CKE(4:5) copied to Port B CKE(6:7)
27	RW	CCS_MODEQ_DISABLE_ECC_ARRAY_CHK: Disable ecc checking on the CCS arrays 0 - ECC checking on 1 - ECC checking off
28	RW	CCS_MODEQ_DISABLE_ECC_ARRAY_CORRECTION: Disable ecc correction on the CCS arrays 0 - ECC correction on 1 - ECC correction off
29	RW	CCS_MODEQ_CCS_ADDR_MUX_SEL: CCS Address Mux Sel - This bit should be turned on until all multiple CCS instructions are completed. 0 - selects address data from mainline logic 1 - selects address data from CCS logic
30:31	RW	CCS_MODEQ_DDR_CAL_TIMEOUT_CNT_MULT: DDR calibration time counter multiplication factor. This value is multiplied by the counter in bits 8:23 to get the total timeout wait time. Values: 1_CCS_CYCLE=>0b00 512_CCS_CYCLES=>0b01 32768_CCS_CYCLES=>0b10 1073741824_CCS_CYCLES=>0b11
32:47	RW	CCS_MODEQ_MA_B_ADDRESS_IDLE_PAT: DDR Row and Column Address Idle Pattern (Addr 0 - Addr 15) For DDR4: Addr 14 - 15 is Addr 17 & BG1

Bits	SCOM	Field Mnemonic: Description
48:50	RW	CCS_MODEQ_MA_B_BANK_IDLE_PAT: DDR Bank Address Idle Pattern For DDR3: Bank 0 - Bank 2 For DDR4: B0, B1, BG0
51	RW	CCS_MODEQ_MA_B_ACTIVATE_IDLE_PAT: DDR4 Activate Idle Pattern
52	RW	CCS_MODEQ_MA_B_RASN_IDLE_PAT: DDR RAS# Idle Pattern
53	RW	CCS_MODEQ_MA_B_CASN_IDLE_PAT: DDR CAS# Idle Pattern
54	RW	CCS_MODEQ_MA_B_WEN_IDLE_PAT: DDR Write Enable (WE#) Idle Pattern
55	RW	CCS_MODEQ_NTTM_MODE: Non Traditional Transparent Mode When set to 1, limited non-traditional read and write operations can be done.
56:59	RW	CCS_MODEQ_NTTM_RW_DATA_DLY: Non Traditional Transparent ReadWrite Delay Use to delay the Write data start pulse or Read Data capture pulse to the DDR Phys. Maximum delay of 15 cycles is possible.
60	RW	CCS_MODEQ_DDR_RESETN_ENABLE: DDR Resetn Enabled When set to 1, bit 16 of the CCS_INST_ARR0 will be driven out to DDR Resetn. When set to 0, ccs_modeq(24) will be driven out to DDR Resetn.
61	RW	CCS_MODEQ_DDR_PARITY_ENABLE: DDR Parity Enabled When set to 1, bit 60 of the CCS_INST_ARR0 will be driven out to DDR parity. When set to 0, the hardware calculates the parity.
62	RW	CCS_MODEQ_GP_BIT_3_ENABLE: GP bit 3 enable (force_mclk_low) When set to 1, the inverted value of GP(3) will be driven on the force_mclk_low signal to the DDR PHYs. When set to 0, the value of inverted value of ccs_modeq(63) will be driven on the force_mclk_low signal to the DDR PHYs
63	RW	CCS_MODEQ_FORCE_MCLK_LOW_N: force_mclk_low_n When set to 0, a '1' will be driven on the force_mclk_low signal to the DDR PHYs. When set to 1, the inverted value of ccs_modeq(63) will be driven on the force_mclk_low signal to the DDR PHYs

Register Name	***MCBIST Memory Register 0***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR0Q
Address	0000000003010EA8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST00_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST00_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST00_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST00_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand

Bits	SCOM	Field Mnemonic: Description
6:7	RW	MCBIST_CFG_TEST00_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST00_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST00_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST00_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST00_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
16:18	RW	MCBIST_CFG_TEST01_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST01_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST01_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST01_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST01_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11

Bits	SCOM	Field Mnemonic: Description
24:26	RW	MCBIST_CFG_TEST01_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST01_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST01_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST01_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
32:34	RW	MCBIST_CFG_TEST02_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST02_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST02_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST02_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST02_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST02_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111

Bits	SCOM	Field Mnemonic: Description
43	RW	MCBIST_CFG_TEST02_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST02_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST02_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
48:50	RW	MCBIST_CFG_TEST03_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST03_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST03_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST03_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST03_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST03_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST03_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST03_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11

Bits	SCOM	Field Mnemonic: Description
62:63	RW	MCBIST_CFG_TEST03_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 1***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR1Q
Address	0000000003010EA9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST04_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST04_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST04_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST04_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST04_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST04_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST04_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1

Bits	SCOM	Field Mnemonic: Description
12:13	RW	MCBIST_CFG_TEST04_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST04_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
16:18	RW	MCBIST_CFG_TEST05_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST05_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST05_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST05_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST05_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST05_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST05_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST05_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11

Bits	SCOM	Field Mnemonic: Description
30:31	RW	MCBIST_CFG_TEST05_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11
32:34	RW	MCBIST_CFG_TEST06_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST06_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST06_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST06_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST06_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST06_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST06_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST06_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST06_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST07_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST07_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST07_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST07_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST07_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST07_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST07_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST07_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST07_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 2***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR2Q
Address	0000000003010EAA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST08_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST08_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST08_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST08_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST08_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST08_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST08_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST08_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST08_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST09_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST09_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST09_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST09_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST09_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST09_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST09_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST09_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST09_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST10_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST10_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST10_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST10_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST10_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST10_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST10_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST10_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST10_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST11_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST11_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST11_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST11_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST11_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST11_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST11_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST11_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST11_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 3***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR3Q
Address	0000000003010EAB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST12_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST12_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST12_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST12_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST12_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST12_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST12_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST12_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST12_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST13_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST13_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST13_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST13_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST13_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST13_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST13_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST13_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST13_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST14_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST14_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST14_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST14_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST14_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST14_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST14_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST14_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST14_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST15_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST15_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST15_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST15_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST15_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST15_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST15_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST15_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST15_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 4***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR4Q
Address	0000000003010EAC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST16_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST16_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST16_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST16_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST16_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST16_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST16_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST16_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST16_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST17_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST17_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST17_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST17_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST17_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST17_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST17_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST17_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST17_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST18_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST18_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST18_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST18_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST18_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST18_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST18_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST18_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST18_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST19_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST19_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST19_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST19_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST19_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST19_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST19_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST19_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST19_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 5***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR5Q
Address	0000000003010EAD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST20_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST20_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST20_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST20_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST20_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST20_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST20_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST20_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST20_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST21_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST21_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST21_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST21_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST21_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST21_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST21_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST21_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST21_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST22_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST22_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST22_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST22_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST22_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST22_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST22_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST22_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST22_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST23_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST23_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST23_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST23_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST23_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST23_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST23_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST23_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST23_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Register 6***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR6Q
Address	0000000003010EAE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST24_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST24_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST24_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST24_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST24_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST24_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST24_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST24_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST24_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST25_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST25_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST25_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST25_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST25_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST25_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST25_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST25_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST25_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST26_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST26_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST26_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST26_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST26_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST26_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST26_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST26_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST26_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST27_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST27_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST27_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST27_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST27_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST27_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST27_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST27_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST27_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Memory Parameter Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBPARMQ
Address	0000000003010EAF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RW	MCBPARMQ_RESERVED_0_49: Not used
50:52	RW	MCBPARMQ_CFG_RANDCMD_WGT: Specifies the weighting of random commands as follows (%Read %Write): Values: 12_87=>0b000 25_75=>0b001 50_50=>0b010 75_25=>0b011 87_12=>0b100
53:59	RW	MCBPARMQ_CFG_MIN_CMD_GAP: This is the minimum number of cycles between commands when cfg_en_randcmd_gap is a 0. If cfg_en_randcmd_gap is a 1 this becomes a 7 bit seed for the LFSR that randomly generates the gap intervals between 1-127. A value of all zeros will force MCBIST to issues commands as fast as possible.
60	RW	MCBPARMQ_CFG_EN_RANDCMD_GAP: When set to a 1 random command gaps from 1-1023 cycles are enabled and cfg_min_cmd_gap is disabled and becomes a seed for a LFSR that is randomly generating 1-127 cycle gaps (there is another 8 bit LFSR that is generating a 1-8 cycle multiplier).
61:62	RW	MCBPARMQ_CFG_RANDGAP_WGT: Forces the following command gap intervals when cfg_en_randcmd_gap is a 1: 00: 1 to 1023 cycles. 01: 1 to 511 cycles. 10: 1 to 255 cycles. 11: 1 to 127 cycles.
63	RW	MCBPARMQ_CFG_BC4_EN: BC4 enable When set, it enables BC4 data mode. This configuration cannot be use in ECC data mode.

Register Name	***MCBIST Runtime Counter Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.RUNTIMECTRQ
Address	0000000003010EB0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:36	RWX	RUNTIMECTRQ_CFG_RUNTIME_CTR: This is the runtime counter facility. This 37 bit counter will increment every 4 memory clock cycles which gives it a maximum value of 687 seconds at 800 MHz or 824 seconds at 667 MHz.
37:63	RO	constant=0b00000000000000000000000000000

Register Name	***MCBIST Refresh Control Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRCRQ
Address	0000000003010EB1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RW	MCBRCRQ_RESERVED_0_31: Not used
32	RW	MCBRCRQ_CFG_RUNTIME_MCBALL: Configures what the runtime counter counts: Values: JUST_ONE_SUBTEST=>0b0 FULL_MCBIST_RUN=>0b1
33:37	RW	MCBRCRQ_CFG_RUNTIME_SUBTEST: If bit 32 is a 0, these bits represent the subtest number that should be counted.

Bits	SCOM	Field Mnemonic: Description
38	RW	MCBRCRQ_CFG_RUNTIME_OVERHEAD: If bit 32 is a 1, this bit configures the starting point of the runtime counter: Values: WITHOUT_OVERHEAD_WAIT_UNTIL_SUBTEST_0_IS_STARTED=>0b0 WITH_OVERHEAD_AS_SOON_AS_MCBIST_LEAVES_THE_IDLE_STATE=>0b1
39	RW	MCBRCRQ_RESERVED_39: Not used
40:63	RO	constant=0b00000000000000000000000

Register Name	***Random Data Seed 0 Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS0Q
Address	0000000003010EB2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS0Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS0Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS0Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS0Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS0Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS0Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS0Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS0Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***Random Data Seed 1 Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS1Q
Address	0000000003010EB3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS1Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS1Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS1Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS1Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS1Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS1Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS1Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS1Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 2 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS2Q
Address	0000000003010EB4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS2Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS2Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS2Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS2Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS2Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS2Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS2Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS2Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 3 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS3Q
Address	0000000003010EB5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS3Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS3Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS3Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS3Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS3Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS3Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS3Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS3Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 4 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS4Q
Address	0000000003010EB6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS4Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS4Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MCBRDS4Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS4Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS4Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS4Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS4Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS4Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***Random Data Seed 5 Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS5Q
Address	0000000003010EB7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS5Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS5Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS5Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS5Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS5Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS5Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS5Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS5Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	***Random Data Seed 6 Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS6Q
Address	0000000003010EB8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS6Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS6Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS6Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS6Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS6Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS6Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS6Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS6Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 7 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS7Q
Address	0000000003010EB9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS7Q_DGEN_RNDD_SEED0: DQ(0) Random Data Seed
8:15	RW	MCBRDS7Q_DGEN_RNDD_SEED1: DQ(1) Random Data Seed
16:23	RW	MCBRDS7Q_DGEN_RNDD_SEED2: DQ(2) Random Data Seed
24:31	RW	MCBRDS7Q_DGEN_RNDD_SEED3: DQ(3) Random Data Seed
32:39	RW	MCBRDS7Q_DGEN_RNDD_SEED4: DQ(4) Random Data Seed
40:47	RW	MCBRDS7Q_DGEN_RNDD_SEED5: DQ(5) Random Data Seed
48:55	RW	MCBRDS7Q_DGEN_RNDD_SEED6: DQ(6) Random Data Seed
56:63	RW	MCBRDS7Q_DGEN_RNDD_SEED7: DQ(7) Random Data Seed

Register Name	*Random Data Seed 8 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDS8Q
Address	0000000003010EBA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDS8Q_DGEN_RNDD_SEED0: DQ(8) Burst 1 Random Data Seed
8:15	RW	MCBRDS8Q_DGEN_RNDD_SEED1: DQ(8) Burst 2 Random Data Seed
16:23	RW	MCBRDS8Q_DGEN_RNDD_SEED2: DQ(8) Burst 3 Random Data Seed
24:31	RW	MCBRDS8Q_DGEN_RNDD_SEED3: DQ(8) Burst 4 Random Data Seed
32:39	RW	MCBRDS8Q_DGEN_RNDD_SEED4: DQ(8) Burst 5 Random Data Seed
40:47	RW	MCBRDS8Q_DGEN_RNDD_SEED5: DQ(8) Burst 6 Random Data Seed
48:55	RW	MCBRDS8Q_DGEN_RNDD_SEED6: DQ(8) Burst 7 Random Data Seed
56:63	RW	MCBRDS8Q_DGEN_RNDD_SEED7: DQ(8) Burst 8 Random Data Seed

Register Name	*Random Data Seed Spare Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRDSSPQ
Address	0000000003010EBB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBRDSSPQ_DGEN_RNDD_SEED0: DQ(9) Burst 1 Random Data Seed
8:15	RW	MCBRDSSPQ_DGEN_RNDD_SEED1: DQ(9) Burst 2 Random Data Seed

Bits	SCOM	Field Mnemonic: Description
16:23	RW	MCBRDSSPQ_DGEN_RNDD_SEED2: DQ(9) Burst 3 Random Data Seed
24:31	RW	MCBRDSSPQ_DGEN_RNDD_SEED3: DQ(9) Burst 4 Random Data Seed
32:39	RW	MCBRDSSPQ_DGEN_RNDD_SEED4: DQ(9) Burst 5 Random Data Seed
40:47	RW	MCBRDSSPQ_DGEN_RNDD_SEED5: DQ(9) Burst 6 Random Data Seed
48:55	RW	MCBRDSSPQ_DGEN_RNDD_SEED6: DQ(9) Burst 7 Random Data Seed
56:63	RW	MCBRDSSPQ_DGEN_RNDD_SEED7: DQ(9) Burst 8 Random Data Seed

Register Name	***Data Rotate Seed Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBDRSRQ
Address	0000000003010EBC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBDRSRQ_CFG_DATA_ROT_SEED: Bits 0:63 of the Data Rotate Seed

Register Name	***Data Rotate Configuration Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBDRCRQ
Address	0000000003010EBD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	MCBDRCRQ_CFG_DATA_ROT: Bits to shift: Values: ROTATE_1_BIT=>0b0001 ROTATE_2_BITS=>0b0010 ROTATE_3_BITS=>0b0011 ROTATE_4_BITS=>0b0100 ROTATE_5_BITS=>0b0101 ROTATE_6_BITS=>0b0110 ROTATE_7_BITS=>0b0111 ROTATE_8_BITS=>0b1000 ROTATE_9_BITS=>0b1001 ROTATE_10_BITS=>0b1010 ROTATE_11_BITS=>0b1011 ROTATE_12_BITS=>0b1100 ROTATE_13_BITS=>0b1101 ROTATE_14_BITS=>0b1110 ROTATE_15_BITS=>0b1111
4:19	RW	MCBDRCRQ_CFG_DATA_ROT_SEED: Bits 64:79 of the Data Rotate Seed
20	RW	MCBDRCRQ_CFG_INVERT_DATA: These bits control the final inversion of data over to the write data flow. Bit 20 = Invert MA Data
21:63	RW	MCBDRCRQ_RESERVED_21_63: Not used

Register Name	*Fixed Data Seed Burst 0 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD0Q
Address	0000000003010EBE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD0Q_CFG_FIXED_SEED: Fixed Data Seed(0:63)

Register Name	*Fixed Data Seed Burst 1 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD1Q
Address	0000000003010EBF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD1Q_CFG_FIXED_SEED: Fixed Data Seed(72:135)

Register Name	*Fixed Data Seed Burst 2 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD2Q
Address	0000000003010EC0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD2Q_CFG_FIXED_SEED: Fixed Data Seed(144:207)

Register Name	*Fixed Data Seed Burst 3 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD3Q
Address	0000000003010EC1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD3Q_CFG_FIXED_SEED: Fixed Data Seed(216:279)

Register Name	*Fixed Data Seed Burst 4 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD4Q
Address	0000000003010EC2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD4Q_CFG_FIXED_SEED: Fixed Data Seed(288:351)

Register Name	*Fixed Data Seed Burst 5 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD5Q
Address	0000000003010EC3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD5Q_CFG_FIXED_SEED: Fixed Data Seed(360:423)

Register Name	*Fixed Data Seed Burst 6 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD6Q
Address	0000000003010EC4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD6Q_CFG_FIXED_SEED: Fixed Data Seed(432:495)

Register Name	*Fixed Data Seed Burst 7 Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFD7Q
Address	0000000003010EC5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	MCBFD7Q_CFG_FIXED_SEED: Fixed Data Seed(504:567)

Register Name	*Fixed Data Seed Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFDQ
Address	0000000003010EC6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBFDQ_CFG_FIXED_SEED1: DQ(8) Burst 1 Fixed Data Seed(64:71)
8:15	RW	MCBFDQ_CFG_FIXED_SEED2: DQ(8) Burst 2 Fixed Data Seed(136:143)
16:23	RW	MCBFDQ_CFG_FIXED_SEED3: DQ(8) Burst 3 Fixed Data Seed(208:215)
24:31	RW	MCBFDQ_CFG_FIXED_SEED4: DQ(8) Burst 4 Fixed Data Seed(280:287)
32:39	RW	MCBFDQ_CFG_FIXED_SEED5: DQ(8) Burst 5 Fixed Data Seed(352:359)
40:47	RW	MCBFDQ_CFG_FIXED_SEED6: DQ(8) Burst 6 Fixed Data Seed(424:431)
48:55	RW	MCBFDQ_CFG_FIXED_SEED7: DQ(8) Burst 7 Fixed Data Seed(496:503)
56:63	RW	MCBFDQ_CFG_FIXED_SEED8: DQ(8) Burst 8 Fixed Data Seed(568:575)

Register Name	*Fixed Data Seed Spare Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBFDSPQ
Address	0000000003010EC7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCBFDSPQ_CFG_FIXED_SEED1: DQ(9) Burst 1 Fixed Data Seed(576:583)
8:15	RW	MCBFDSPQ_CFG_FIXED_SEED2: DQ(9) Burst 2 Fixed Data Seed(584:591)
16:23	RW	MCBFDSPQ_CFG_FIXED_SEED3: DQ(9) Burst 3 Fixed Data Seed(592:599)
24:31	RW	MCBFDSPQ_CFG_FIXED_SEED4: DQ(9) Burst 4 Fixed Data Seed(600:607)
32:39	RW	MCBFDSPQ_CFG_FIXED_SEED5: DQ(9) Burst 5 Fixed Data Seed(608:615)
40:47	RW	MCBFDSPQ_CFG_FIXED_SEED6: DQ(9) Burst 6 Fixed Data Seed(616:623)
48:55	RW	MCBFDSPQ_CFG_FIXED_SEED7: DQ(9) Burst 7 Fixed Data Seed(624:631)
56:63	RW	MCBFDSPQ_CFG_FIXED_SEED8: DQ(9) Burst 8 Fixed Data Seed(632:639)

Register Name	*Port A Socket 0 Address Map Register 0*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR0A0Q
Address	0000000003010EC8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK0: Master Rank Bit 0 (MSB)
6:11	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK1: Master Rank Bit 1

Bits	SCOM	Field Mnemonic: Description
12:17	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK2: Master Rank Rank Bit 2
18:23	RW	MCBAMR0A0Q_CFG_A0MAP_MRANK3: Master Rank Rank Bit 3
24:29	RW	MCBAMR0A0Q_CFG_A0MAP_SRANK0: Slave Rank Bit 0 (MSB)
30:35	RW	MCBAMR0A0Q_CFG_A0MAP_SRANK1: Slave Rank Bit 1
36:41	RW	MCBAMR0A0Q_CFG_A0MAP_SRANK2: Slave Rank Rank Bit 2
42:47	RW	MCBAMR0A0Q_CFG_A0MAP_BANK3: DRAM Bank Address Bit 3 (MSB)
48:53	RW	MCBAMR0A0Q_CFG_A0MAP_BANK2: DRAM Bank Address Bit 2 (MSB)
54:59	RW	MCBAMR0A0Q_CFG_A0MAP_BANK1: DRAM Bank Address Bit 1
60:63	RW	MCBAMR0A0Q_RESERVED_60_63: Reserved

Register Name	***Port A Socket 0 Address Map Register 1***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR1A0Q
Address	0000000003010EC9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A0Q_CFG_A0MAP_BANK0: DRAM Bank Address Bit 0
6:11	RW	MCBAMR1A0Q_CFG_A0MAP_ROW16: DRAM Row Address Bit16 (MSB)
12:17	RW	MCBAMR1A0Q_CFG_A0MAP_ROW15: DRAM Row Address Bit15
18:23	RW	MCBAMR1A0Q_CFG_A0MAP_ROW14: DRAM Row Address Bit 14
24:29	RW	MCBAMR1A0Q_CFG_A0MAP_ROW13: DRAM Row Address Bit 13
30:35	RW	MCBAMR1A0Q_CFG_A0MAP_ROW12: DRAM Row Address Bit 12
36:41	RW	MCBAMR1A0Q_CFG_A0MAP_ROW11: DRAM Row Address Bit 11
42:47	RW	MCBAMR1A0Q_CFG_A0MAP_ROW10: DRAM Row Address Bit 10
48:53	RW	MCBAMR1A0Q_CFG_A0MAP_ROW9: DRAM Row Address Bit 9
54:59	RW	MCBAMR1A0Q_CFG_A0MAP_ROW8: DRAM Row Address Bit 8
60:63	RW	MCBAMR1A0Q_RESERVED_60_63: Not used

Register Name	***Port A Socket 0 Address Map Register 2***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR2A0Q
Address	0000000003010ECA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A0Q_CFG_A0MAP_ROW7: DRAM Row Address Bit 7
6:11	RW	MCBAMR2A0Q_CFG_A0MAP_ROW6: DRAM Row Address Bit 6
12:17	RW	MCBAMR2A0Q_CFG_A0MAP_ROW5: DRAM Row Address Bit 5
18:23	RW	MCBAMR2A0Q_CFG_A0MAP_ROW4: DRAM Row Address Bit 4

Bits	SCOM	Field Mnemonic: Description
24:29	RW	MCBAMR2A0Q_CFG_A0MAP_ROW3: DRAM Row Address Bit 3
30:35	RW	MCBAMR2A0Q_CFG_A0MAP_ROW2: DRAM Row Address Bit 2
36:41	RW	MCBAMR2A0Q_CFG_A0MAP_ROW1: DRAM Row Address Bit 1
42:47	RW	MCBAMR2A0Q_CFG_A0MAP_ROW0: DRAM Row Address Bit 0
48:53	RW	MCBAMR2A0Q_CFG_A0MAP_COL13: DRAM Column Address Bit 13 (MSB)
54:59	RW	MCBAMR2A0Q_CFG_A0MAP_COL11: DRAM Column Address Bit 11
60:63	RW	MCBAMR2A0Q_RESERVED_60_63: Not used

Register Name	***Port A Socket 0 Address Map Register 3***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR3A0Q
Address	0000000003010ECB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A0Q_CFG_A0MAP_COL9: DRAM Column Address Bit 9
6:11	RW	MCBAMR3A0Q_CFG_A0MAP_COL8: DRAM Column Address Bit 8
12:17	RW	MCBAMR3A0Q_CFG_A0MAP_COL7: DRAM Column Address Bit 7
18:23	RW	MCBAMR3A0Q_CFG_A0MAP_COL6: DRAM Column Address Bit 6
24:29	RW	MCBAMR3A0Q_CFG_A0MAP_COL5: DRAM Column Address Bit 5
30:35	RW	MCBAMR3A0Q_CFG_A0MAP_COL4: DRAM Column Address Bit 4
36:41	RW	MCBAMR3A0Q_CFG_A0MAP_COL3: DRAM Column Address Bit 3
42:47	RW	MCBAMR3A0Q_CFG_A0MAP_COL2: DRAM Column Address Bit 2 - Map to an Unused Address bit if NOT fixed BL= 4
48:63	RW	MCBAMR3A0Q_RESERVED_48_63: Not Used

Register Name	***Port A0 Random Start Address Configuration Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRSARA0Q
Address	0000000003010ECC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBRSARA0Q_CFG_RAND_START_ADDR_A0: Socket A0 Starting Address when addressing is random forward Ending Address when addressing is random reverse
38:63	RW	MCBRSARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Random Start Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBRSARA1Q
Address	0000000003010ECD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBRSARA1Q_CFG_RAND_START_ADDR_A1: Socket A1 Starting Address when addressing is random forward Ending Address when addressing is random reverse
38:63	RW	MCBRSARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Random End Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBREARA0Q
Address	0000000003010ECE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBREARA0Q_CFG_RAND_END_ADDR_A0: Socket A0 Ending Address when addressing is random forward Starting Address when addressing is random reverse
38:63	RW	MCBREARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Random End Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBREARA1Q
Address	0000000003010ECF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBREARA1Q_CFG_RAND_END_ADDR_A1: Socket A1 Ending Address when addressing is random forward Starting Address when addressing is random reverse
38:63	RW	MCBREARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Sequential Start Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBSSARA0Q
Address	0000000003010ED0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSSARA0Q_CFG_SEQ_START_ADDR_A0: Socket A0 Starting Address when addressing is sequential forward Ending Address when addressing is sequential reverse
38:63	RW	MCBSSARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Sequential Start Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBSSARA1Q
Address	0000000003010ED1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSSARA1Q_CFG_SEQ_START_ADDR_A1: Socket A1 Starting Address when addressing is sequential forward Ending Address when addressing is sequential reverse
38:63	RW	MCBSSARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Sequential End Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBSEARA0Q
Address	0000000003010ED2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSEARA0Q_CFG_SEQ_END_ADDR_A0: Socket A0 Ending Address when addressing is sequential forward Starting Address when addressing is sequential reverse
38:63	RW	MCBSEARA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Sequential End Address Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBSEARA1Q
Address	0000000003010ED3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBSEARA1Q_CFG_SEQ_END_ADDR_A1: Socket A1 Ending Address when addressing is sequential forward Starting Address when addressing is sequential reverse
38:63	RW	MCBSEARA1Q_RESERVED_38_63: Not Used

Register Name	*Port A0 Address LFSR Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBLFSRA0Q
Address	0000000003010ED4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBLFSRA0Q_CFG_LFSR_MASK_A0: Socket A0 Default configuration is for a 25 bit LFSR MASK Master Rank 0:3, Slave Rank 0:2, Bank(3:0), Row(16:15) fixed Row(14:0), Col(13,11,9:2) variable

Bits	SCOM	Field Mnemonic: Description
38:63	RW	MCBLFSRA0Q_RESERVED_38_63: Not Used

Register Name	*Port A1 Address LFSR Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBLFSRA1Q
Address	0000000003010ED5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	MCBLFSRA1Q_CFG_LFSR_MASK_A1: Socket A1 Default configuration is for a 25 bit LFSR MASK Master Rank 0:3, Slave Rank 0:2, Bank(3:0), Row(16:15) fixed Row(14:0), Col(13,11,9:2) variable
38:63	RW	MCBLFSRA1Q_RESERVED_38_63: Not Used

Register Name	*Port A Address Generator Configuration Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAGRAQ
Address	0000000003010ED6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAGRAQ_CFG_FIXED_WIDTH_A0: Sets the number of fixed slots in the address generator for Port A, socket A0. This will cause the bits from (MSB to MSB+cfg_fixed_width_a0-1) to not be included in the address generation. Used in conjunction with the configurable address map registers. Example: Fixed Rank, Fixed Bank, Fixed Row = 3 + 3 + 16 = 22 Program 0x16 Defaulted to a fixed Rank setting - Don needs to check this
6:11	RW	MCBAGRAQ_CFG_FIXED_WIDTH_A1: Sets the number of fixed slots in the address generator for Port A, socket A1. This will cause the bits from (MSB to MSB+cfg_fixed_width_a1-1) to not be included in the address generation. Used in conjunction with the configurable address map registers. Example: Fixed Rank, Fixed Bank, Fixed Row = 3 + 3 + 16 = 22 Program 0x16 Defaulted to a fixed Rank setting - Don needs to check this
12:15	RW	MCBAGRAQ_CFG_PORTA0_RATIO: Programs how often Port A, socket A0 addresses need to be generated relative to Port A, socket A1 addresses. Ratios can be set anywhere from [1-15] : [1-15]. Used for Deterministic address weighting.
16:19	RW	MCBAGRAQ_CFG_PORTA1_RATIO: Programs how often Port A, socket A1 addresses need to be generated relative to Port A, socket A0 addresses. Ratios can be set anywhere from [1-15] : [1-15]. Used for Deterministic address weighting.
20:22	RW	MCBAGRAQ_CFG_RANDPORT_WGT_A: Specify the weighting of A0A1 port accesses. A B 000 - 12.5 87.5 001 - 25 75 010 - 50 50 011 - 75 25 100 - 87.5 12.5
23	RW	MCBAGRAQ_CFG_DET_RAND_WGT_A: 0 - Use deterministic ratio to switch between socket A0 and socket A1 1 - Use random weighted ratio to switch between socket A0 and socket A1
24:25	RW	MCBAGRAQ_CFG_PORTA_SCKT_PPLTD: Socket Populated Values: SOCKET_A0_AND_SOCKET_A1_ARE_NOT_POPULATED=>0b00 ONLY_SOCKET_A1_IS_POPULATED=>0b01 ONLY_SOCKET_A0_IS_POPULATED=>0b10 SOCKET_A0_AND_SOCKET_A1_ARE_BOTH_POPULATED=>0b11
26:31	RW	MCBAGRAQ_RESERVED_26_31: Not used
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	*Port A Socket 1 Address Map Register 0*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR0A1Q
Address	0000000003010ED7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK0: Master Rank Bit 0 (MSB)
6:11	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK1: Master Rank Bit 1
12:17	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK2: Master Rank Rank Bit 2
18:23	RW	MCBAMR0A1Q_CFG_A1MAP_MRANK3: Master Rank Rank Bit 3
24:29	RW	MCBAMR0A1Q_CFG_A1MAP_SRANK0: Slave Rank Bit 0 (MSB)
30:35	RW	MCBAMR0A1Q_CFG_A1MAP_SRANK1: Slave Rank Bit 1
36:41	RW	MCBAMR0A1Q_CFG_A1MAP_SRANK2: Slave Rank Rank Bit 2
42:47	RW	MCBAMR0A1Q_CFG_A1MAP_BANK3: DRAM Bank Address Bit 3 (MSB)
48:53	RW	MCBAMR0A1Q_CFG_A1MAP_BANK2: DRAM Bank Address Bit 2 (MSB)
54:59	RW	MCBAMR0A1Q_CFG_A1MAP_BANK1: DRAM Bank Address Bit 1
60:63	RW	MCBAMR0A1Q_RESERVED_60_63: Reserved

Register Name	*Port A Socket 1 Address Map Register 1*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR1A1Q
Address	0000000003010ED8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A1Q_CFG_A1MAP_BANK0: DRAM Bank Address Bit 0
6:11	RW	MCBAMR1A1Q_CFG_A1MAP_ROW16: DRAM Row Address Bit16 (MSB)
12:17	RW	MCBAMR1A1Q_CFG_A1MAP_ROW15: DRAM Row Address Bit15
18:23	RW	MCBAMR1A1Q_CFG_A1MAP_ROW14: DRAM Row Address Bit 14
24:29	RW	MCBAMR1A1Q_CFG_A1MAP_ROW13: DRAM Row Address Bit 13
30:35	RW	MCBAMR1A1Q_CFG_A1MAP_ROW12: DRAM Row Address Bit 12
36:41	RW	MCBAMR1A1Q_CFG_A1MAP_ROW11: DRAM Row Address Bit 11
42:47	RW	MCBAMR1A1Q_CFG_A1MAP_ROW10: DRAM Row Address Bit 10
48:53	RW	MCBAMR1A1Q_CFG_A1MAP_ROW9: DRAM Row Address Bit 9
54:59	RW	MCBAMR1A1Q_CFG_A1MAP_ROW8: DRAM Row Address Bit 8
60:63	RW	MCBAMR1A1Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 1 Address Map Register 2*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR2A1Q
Address	0000000003010ED9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A1Q_CFG_A1MAP_ROW7: DRAM Row Address Bit 7
6:11	RW	MCBAMR2A1Q_CFG_A1MAP_ROW6: DRAM Row Address Bit 6
12:17	RW	MCBAMR2A1Q_CFG_A1MAP_ROW5: DRAM Row Address Bit 5
18:23	RW	MCBAMR2A1Q_CFG_A1MAP_ROW4: DRAM Row Address Bit 4
24:29	RW	MCBAMR2A1Q_CFG_A1MAP_ROW3: DRAM Row Address Bit 3
30:35	RW	MCBAMR2A1Q_CFG_A1MAP_ROW2: DRAM Row Address Bit 2
36:41	RW	MCBAMR2A1Q_CFG_A1MAP_ROW1: DRAM Row Address Bit 1
42:47	RW	MCBAMR2A1Q_CFG_A1MAP_ROW0: DRAM Row Address Bit 0
48:53	RW	MCBAMR2A1Q_CFG_A1MAP_COL13: DRAM Column Address Bit 13 (MSB)
54:59	RW	MCBAMR2A1Q_CFG_A1MAP_COL11: DRAM Column Address Bit 11
60:63	RW	MCBAMR2A1Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 1 Address Map Register 3*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR3A1Q
Address	0000000003010EDA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A1Q_CFG_A1MAP_COL9: DRAM Column Address Bit 9
6:11	RW	MCBAMR3A1Q_CFG_A1MAP_COL8: DRAM Column Address Bit 8
12:17	RW	MCBAMR3A1Q_CFG_A1MAP_COL7: DRAM Column Address Bit 7
18:23	RW	MCBAMR3A1Q_CFG_A1MAP_COL6: DRAM Column Address Bit 6
24:29	RW	MCBAMR3A1Q_CFG_A1MAP_COL5: DRAM Column Address Bit 5
30:35	RW	MCBAMR3A1Q_CFG_A1MAP_COL4: DRAM Column Address Bit 4
36:41	RW	MCBAMR3A1Q_CFG_A1MAP_COL3: DRAM Column Address Bit 3
42:47	RW	MCBAMR3A1Q_CFG_A1MAP_COL2: DRAM Column Address Bit 2 - Map to an Unused Address bit if NOT fixed BL= 4
48:63	RW	MCBAMR3A1Q_RESERVED_48_63: Not Implemented

Register Name	*MCBIST Control Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCB_CNTLQ
Address	0000000003010EDB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCB_CNTLQ_MCB_START: Start bit - Self resetting bit. Kicks off the MCBIST operation
1	RWX	MCB_CNTLQ_MCB_STOP: Stop bit - Self resetting bit. Stops after Current MCBIST subtest is done.
2:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Configured Command Sequence Status Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCB_CNTLSTATQ
Address	0000000003010EDC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCB_CNTLSTATQ_MCB_IP: IP bit - Hdw sets to a '1'b when MCBIST run in progress
1	RWX	MCB_CNTLSTATQ_MCB_DONE: Done bit - Hdw sets to a '1'b when MCBIST run complete
2	RWX	MCB_CNTLSTATQ_MCB_FAIL: Fail bit - Hdw sets to a '1'b when MCBIST run failed
3:63	RO	constant=0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*RCD/LRDIMM Control Words 0 - 15*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.RCD_LRDIM_CNTL_WORD0_15Q
Address	0000000003010EDD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD0: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
4:7	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD1: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
8:11	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD2: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
12:15	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD3: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
16:19	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD4: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
20:23	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD5: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
24:27	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD6: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)

Bits	SCOM	Field Mnemonic: Description
28:31	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD7: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
32:35	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD8: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
36:39	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD9: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
40:43	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD10: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
44:47	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD11: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
48:51	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD12: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
52:55	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD13: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
56:59	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD14: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)
60:63	RWX	RCD_LRDIM_CNTL_WORD0_15Q_RCD_LRDIMM_CNTL_WORD15: RCDLRDIM Control Word - BA1(0), BA0(0), A(4), A(3)

Register Name	***CCS Array Error Injection Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.CCSARRERRINJQ
Address	0000000003010EDE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	CCSARRERRINJQ_CCS_ARRAY_CE_ERR_INJ_MODE: CE Error inject mode into the ccs array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
1	RW	CCSARRERRINJQ_CCS_ARRAY_CE_ERR_INJ: CE Error inject into the ccs array
2	RW	CCSARRERRINJQ_CCS_ARRAY_UE_ERR_INJ_MODE: UE Error inject mode into the ccs array Values: SINGLE_SHOT=>0b0 CONTINUOUS=>0b1
3	RW	CCSARRERRINJQ_CCS_ARRAY_UE_ERR_INJ: UE Error inject into the ccs array
4	RW	CCSARRERRINJQ_CS_CHIP_ID_2N_MODE: CS_n(2), CS_n(3), CS_n(6), and CS_n(7) used for CHIP IDs for 2N mode Values: CHIP_SELECTS_WILL_BE_ASSERTED_FOR_1_CYCLE_IN_2N_MODE=>0b0 CHIP_SELECTS_BE_ASSERTED_FOR_2_CYCLES_IN_2N_MODE=>0b1
5	RW	CCSARRERRINJQ_DISABLE_2N_MODE: Disable 2N mode Values: ENABLED_2N_MODE_WHEN_THE_CHIP_IS_IN_2N_MODE=>0b0 DISABLES_2N_MODE_WHEN_THE_CHIP_IS_IN_2N_MODE=>0b1
6:63	RW	CCSARRERRINJQ_RESERVED_6_63: RESERVED

Register Name	*MCBIST Memory Register 7*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBMR7Q
Address	0000000003010EDF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	MCBIST_CFG_TEST28_OP_TYPE: Bits(0:2) - Operation Type If Subtest(0:2) = 111 and 8:10(Data mode) = 000 (goto command), then Subtest Addr -- 3:7 specifies which subtest address to change to (used for looping). If Subtest(0:2) = 111 and 8:10(Data mode) not = 000 (refresh only command), then Subtest Addr -- 3:7 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
3	RW	MCBIST_CFG_TEST28_COMPL_1ST_CMD: Bit 3 = Complement the data for the first subcommand
4	RW	MCBIST_CFG_TEST28_COMPL_2ND_CMD: Bit 4 = Complement the data for the second subcommand
5	RW	MCBIST_CFG_TEST28_COMPL_3RD_CMD: Bit 5 = Complement the data for the third subcommand
6:7	RW	MCBIST_CFG_TEST28_ADDR_MODE: Bits(6:7) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
8:10	RW	MCBIST_CFG_TEST28_DATA_MODE: Bits(8:10) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
11	RW	MCBIST_CFG_TEST28_DONE: Bit 11 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
12:13	RW	MCBIST_CFG_TEST28_DATA_SEL: Bits(12:13) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
14:15	RW	MCBIST_CFG_TEST28_ADDR_SEL: Bits(14:15) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
16:18	RW	MCBIST_CFG_TEST29_OP_TYPE: Bits(16:18) - Operation Type If Subtest(16:18) = 111 and 24:26(Data mode) = 000 (goto command), then Subtest Addr -- 22:23 specifies which subtest address to change to (used for looping). If Subtest(16:18) = 111 and 24:26(Data mode) not = 000 (refresh only command), then Subtest Addr -- 22:23 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
19	RW	MCBIST_CFG_TEST29_COMPL_1ST_CMD: Bit 19 = Complement the data for the first subcommand
20	RW	MCBIST_CFG_TEST29_COMPL_2ND_CMD: Bit 20 = Complement the data for the second subcommand
21	RW	MCBIST_CFG_TEST29_COMPL_3RD_CMD: Bit 21 = Complement the data for the third subcommand
22:23	RW	MCBIST_CFG_TEST29_ADDR_MODE: Bits(22:23) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
24:26	RW	MCBIST_CFG_TEST29_DATA_MODE: Bits(24:26) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
27	RW	MCBIST_CFG_TEST29_DONE: Bit 27 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
28:29	RW	MCBIST_CFG_TEST29_DATA_SEL: Bits(28:29) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
30:31	RW	MCBIST_CFG_TEST29_ADDR_SEL: Bits(30:31) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
32:34	RW	MCBIST_CFG_TEST30_OP_TYPE: Bits(32:34) - Operation Type If Subtest(32:34) = 111 and 40:42(Data mode) = 000 (goto command), then Subtest Addr -- 38:39 specifies which subtest address to change to (used for looping). If Subtest(32:34) = 111 and 40:42(Data mode) not = 000 (refresh only command), then Subtest Addr - 38:39 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
35	RW	MCBIST_CFG_TEST30_COMPL_1ST_CMD: Bit 35 = Complement the data for the first subcommand
36	RW	MCBIST_CFG_TEST30_COMPL_2ND_CMD: Bit 36 = Complement the data for the second subcommand
37	RW	MCBIST_CFG_TEST30_COMPL_3RD_CMD: Bit 37 = Complement the data for the third subcommand
38:39	RW	MCBIST_CFG_TEST30_ADDR_MODE: Bits(38:39) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
40:42	RW	MCBIST_CFG_TEST30_DATA_MODE: Bits(40:42) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
43	RW	MCBIST_CFG_TEST30_DONE: Bit 43 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
44:45	RW	MCBIST_CFG_TEST30_DATA_SEL: Bits(44:45) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
46:47	RW	MCBIST_CFG_TEST30_ADDR_SEL: Bits(46:47) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Bits	SCOM	Field Mnemonic: Description
48:50	RW	MCBIST_CFG_TEST31_OP_TYPE: Bits(48:50) - Operation Type If Subtest(48:50) = 111 and 56:58(Data mode) = 000 (goto command), then Subtest Addr -- 54:55 specifies which subtest address to change to (used for looping). If Subtest(48:50) = 111 and 56:58(Data mode) not = 000 (refresh only command), then Subtest Addr -- 54:55 is a don't care Values: WRITE=>0b000 READ=>0b001 READWRITE=>0b010 WRITEREAD=>0b011 READWRITEREAD=>0b100 READWRITEWRITE=>0b101 RANDOM_COMMAND_SEQUENCE=>0b110 GOTO_SUBTEST_N_OR_REFRESH_ONLY=>0b111
51	RW	MCBIST_CFG_TEST31_COMPL_1ST_CMD: Bit 51 = Complement the data for the first subcommand
52	RW	MCBIST_CFG_TEST31_COMPL_2ND_CMD: Bit 52 = Complement the data for the second subcommand
53	RW	MCBIST_CFG_TEST31_COMPL_3RD_CMD: Bit 53 = Complement the data for the third subcommand
54:55	RW	MCBIST_CFG_TEST31_ADDR_MODE: Bits(54:55) - Address Mode Values: SEQUENTIAL_FORWARD=>0b00 SEQUENTIAL_REVERSE=>0b01 RANDOM_FORWARD=>0b10 RANDOM_REVERSE=>0b11
56:58	RW	MCBIST_CFG_TEST31_DATA_MODE: Bits(56:58) - Data Mode Values: FIXED=>0b000 RANDOM_FORWARD=>0b001 RANDOM_REVERSE=>0b010 RANDOM_WECC_FORWARD=>0b011 RANDOM_WECC_REVERSE=>0b100 DATA_EQUAL_ADDRESS=>0b101 DATA_ROTATE_LEFT=>0b110 DATA_ROTATE_RIGHT=>0b111
59	RW	MCBIST_CFG_TEST31_DONE: Bit 59 - Done Bit Values: MCB_CONTINUES_TO_NEXT_SUBTEST=>0b0 MCB_ENDS_AFTER_THIS_SUBTEST=>0b1
60:61	RW	MCBIST_CFG_TEST31_DATA_SEL: Bits(60:61) - Data Select Mode - 00 is original Memory Buffer Mode Values: EACH_BURST_HAVE_DIFFERENT_SEED_DATA=>0b00 BURST_0_SEED_USED_FOR_ALL_BURSTS=>0b01 BURST_1_SEED_USED_FOR_ALL_BURSTS=>0b10 BURST_2_SEED_USED_FOR_ALL_BURSTS=>0b11
62:63	RW	MCBIST_CFG_TEST31_ADDR_SEL: Bits(62:63) - Address Select Mode - 00 is original Memory Buffer Mode Values: FIXED_ADDR_FOR_RAND_SEQ_OR_LFSR=>0b00 PORT_A0_RANDOM_STARTEND_ADDR=>0b01 PORT_A1_RANDOM_STARTEND_ADDR=>0b10 PORT_A0_SEQUENTIAL_STARTEND_ADDR=>0b11

Register Name	***MCBIST Configuration Register***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBCFGQ
Address	0000000003010EE0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:41	RW	MCBCFGQ_RESERVED_0_41: Not used
42:55	RW	MCBIST_CFG_REF_WAIT_TIME: This is the refresh wait time in memory clock cycles. When doing the Refresh only subtest, MCBIST will wait time amount of time before it goes on to the next subtest.
56:59	RW	MCBCFGQ_RESERVED_56_59: Not used
60	RW	MCBIST_CFG_RESET_ERROR_DATA: Reset error log RA, error counters, Status Reg and error map. Note SRB buffer cannot be reset all the time since the data path is not accessible by MCBIST. Rising edge triggered. Must be a 0 and then set to a 1 to force a reset: Values: RESET_INACTIVE=>0b0 RESET_ERROR_LOGS=>0b1
61	RW	MCBIST_CFG_BREAK_ON_SUBTEST: Break on subtest Values: DO_NOT_BREAK_WHEN_SUBTEST_COMPLETES=>0b0 BREAK_WHEN_CURRENT_SUBTEST_COMPLETES_IS_USED_TO_STOP_A_LOOPING_RUN_OF_REFRESH_ONLY=>0b1
62	RW	MCBIST_CFG_STOP_ON_ERR: Stop on error. MCBCMABQ[36] will determine if the stop on error occurs after 1 error is seen or after 8 errors is seen. Values: DO_NOT_STOP_ON_ERROR=>0b0 STOP_ON_ERROR_AFTER_SUBTEST_COMPLETES=>0b1
63	RW	MCBCFGQ_RESERVED_63: Not used

Register Name	***Port A Socket 2 Address Map Register 0***
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR0A2Q
Address	0000000003010EE1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK0: Master Rank Bit 0 (MSB)
6:11	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK1: Master Rank Bit 1
12:17	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK2: Master Rank Rank Bit 2
18:23	RW	MCBAMR0A2Q_CFG_A2MAP_MRANK3: Master Rank Rank Bit 3
24:29	RW	MCBAMR0A2Q_CFG_A2MAP_SRANK0: Slave Rank Bit 0 (MSB)
30:35	RW	MCBAMR0A2Q_CFG_A2MAP_SRANK1: Slave Rank Bit 1
36:41	RW	MCBAMR0A2Q_CFG_A2MAP_SRANK2: Slave Rank Rank Bit 2
42:47	RW	MCBAMR0A2Q_CFG_A2MAP_BANK3: DRAM Bank Address Bit 3 (MSB)
48:53	RW	MCBAMR0A2Q_CFG_A2MAP_BANK2: DRAM Bank Address Bit 2 (MSB)
54:59	RW	MCBAMR0A2Q_CFG_A2MAP_BANK1: DRAM Bank Address Bit 1
60:63	RW	MCBAMR0A2Q_RESERVED_60_63: Reserved

Register Name	*Port A Socket 2 Address Map Register 1*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR1A2Q
Address	0000000003010EE2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR1A2Q_CFG_A2MAP_BANK0: DRAM Bank Address Bit 0
6:11	RW	MCBAMR1A2Q_CFG_A2MAP_ROW16: DRAM Row Address Bit16 (MSB)
12:17	RW	MCBAMR1A2Q_CFG_A2MAP_ROW15: DRAM Row Address Bit15
18:23	RW	MCBAMR1A2Q_CFG_A2MAP_ROW14: DRAM Row Address Bit 14
24:29	RW	MCBAMR1A2Q_CFG_A2MAP_ROW13: DRAM Row Address Bit 13
30:35	RW	MCBAMR1A2Q_CFG_A2MAP_ROW12: DRAM Row Address Bit 12
36:41	RW	MCBAMR1A2Q_CFG_A2MAP_ROW11: DRAM Row Address Bit 11
42:47	RW	MCBAMR1A2Q_CFG_A2MAP_ROW10: DRAM Row Address Bit 10
48:53	RW	MCBAMR1A2Q_CFG_A2MAP_ROW9: DRAM Row Address Bit 9
54:59	RW	MCBAMR1A2Q_CFG_A2MAP_ROW8: DRAM Row Address Bit 8
60:63	RW	MCBAMR1A2Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 2 Address Map Register 2*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR2A2Q
Address	0000000003010EE3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR2A2Q_CFG_A2MAP_ROW7: DRAM Row Address Bit 7
6:11	RW	MCBAMR2A2Q_CFG_A2MAP_ROW6: DRAM Row Address Bit 6
12:17	RW	MCBAMR2A2Q_CFG_A2MAP_ROW5: DRAM Row Address Bit 5
18:23	RW	MCBAMR2A2Q_CFG_A2MAP_ROW4: DRAM Row Address Bit 4
24:29	RW	MCBAMR2A2Q_CFG_A2MAP_ROW3: DRAM Row Address Bit 3
30:35	RW	MCBAMR2A2Q_CFG_A2MAP_ROW2: DRAM Row Address Bit 2
36:41	RW	MCBAMR2A2Q_CFG_A2MAP_ROW1: DRAM Row Address Bit 1
42:47	RW	MCBAMR2A2Q_CFG_A2MAP_ROW0: DRAM Row Address Bit 0
48:53	RW	MCBAMR2A2Q_CFG_A2MAP_COL13: DRAM Column Address Bit 13 (MSB)
54:59	RW	MCBAMR2A2Q_CFG_A2MAP_COL11: DRAM Column Address Bit 11
60:63	RW	MCBAMR2A2Q_RESERVED_60_63: Not used

Register Name	*Port A Socket 2 Address Map Register 3*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MCBAMR3A2Q
Address	0000000003010EE4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RW	MCBAMR3A2Q_CFG_A2MAP_COL9: DRAM Column Address Bit 9
6:11	RW	MCBAMR3A2Q_CFG_A2MAP_COL8: DRAM Column Address Bit 8
12:17	RW	MCBAMR3A2Q_CFG_A2MAP_COL7: DRAM Column Address Bit 7
18:23	RW	MCBAMR3A2Q_CFG_A2MAP_COL6: DRAM Column Address Bit 6
24:29	RW	MCBAMR3A2Q_CFG_A2MAP_COL5: DRAM Column Address Bit 5
30:35	RW	MCBAMR3A2Q_CFG_A2MAP_COL4: DRAM Column Address Bit 4
36:41	RW	MCBAMR3A2Q_CFG_A2MAP_COL3: DRAM Column Address Bit 3
42:47	RW	MCBAMR3A2Q_CFG_A2MAP_COL2: DRAM Column Address Bit 2 - Map to an Unused Address bit if NOT fixed BL= 4
48:63	RW	MCBAMR3A2Q_RESERVED_48_63: Not Implemented

Register Name	*CCS Fixed Data Register 0*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.CCS_FIXED_DATA0Q
Address	0000000003010EE5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	CCS_FIXED_DATA0Q_FIXED_DATA_0_63: Fixed data from Non traditional Transparent Mode

Register Name	*CCS Fixed Data Register 1*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.CCS_FIXED_DATA1Q
Address	0000000003010EE6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	CCS_FIXED_DATA1Q_FIXED_DATA_64_79: Fixed data from Non traditional Transparent Mode
16:63	RW	CCS_FIXED_DATA1Q_RESERVED_16_63: RESERVED

Register Name	*MBA Error Report Register*
Mnemonic	MBU.MBA23.MBA_MCBIST.SCOMFIR.MBA_MCBERRPTQ
Address	0000000003010EE7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	MBA_MCBERRPTQ_MAINT_START_ADDR_ERR: Maint Start Address Error on linked to MBAFIR bit 1
1	ROX	MBA_MCBERRPTQ_MAINT_END_ADDR_ERR: Maint End Address Error on linked to MBAFIR bit 1
2	ROX	MBA_MCBERRPTQ_MCB_FIR_CCS_ERR: CCS FSM Parity Error on linked to MBAFIR bit 3
3	ROX	MBA_MCBERRPTQ_MAINT_1HOT_ST_ERROR: Maint FSM Parity Error on linked to MBAFIR bit 6
4	ROX	MBA_MCBERRPTQ_MCB_FIR_MCBAGEN_ERR: MCBIST Address Generation FSM Parity Error on linked to MBAFIR bit 3
5	ROX	MBA_MCBERRPTQ_MCB_FIR_MCBFSM_ERR: MCBIST Control FSM Parity Error on linked to MBAFIR bit 3
6	ROX	MBA_MCBERRPTQ_MBMCCQ_PE: SCOM Register Parity Error on mbmccq linked to MBAFIR bit 5
7	ROX	MBA_MCBERRPTQ_CCS_CNTLQ_PE: SCOM Register Parity Error on ccs_cntlq linked to MBAFIR bit 6
8	ROX	MBA_MCBERRPTQ_MCB_CNTLQ_PE: SCOM Register Parity Error on mcb_cntlq linked to MBAFIR bit 6
9	ROX	MBA_MCBERRPTQ_MBSPAQ_PE: SCOM Register Parity Error on mbspaq linked to MBAFIR bit 5
10	ROX	MBA_MCBERRPTQ_MAINT_CCS_PE: SCOM Register Parity Error on maint and ccs register linked to MBAFIR bit 5
11	ROX	MBA_MCBERRPTQ_MCBAGEN_PE: SCOM Register Parity Error linked on mcbist address generation registers to MBAFIR bit 5
12	ROX	MBA_MCBERRPTQ_MCBDGEN_PE: SCOM Register Parity Error linked on mcbist data generation registers to MBAFIR bit 5
13	ROX	MBA_MCBERRPTQ_MCB_CONTROLLER_PE: SCOM Register Parity Error linked on mcbist controller configuration registers to MBAFIR bit 5
14	ROX	MBA_MCBERRPTQ_MBABS0_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
15	ROX	MBA_MCBERRPTQ_MBABS1_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
16	ROX	MBA_MCBERRPTQ_MBABS2_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
17	ROX	MBA_MCBERRPTQ_MBABS3_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
18	ROX	MBA_MCBERRPTQ_MBABS4_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
19	ROX	MBA_MCBERRPTQ_MBABS5_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
20	ROX	MBA_MCBERRPTQ_MBABS6_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
21	ROX	MBA_MCBERRPTQ_MBABS7_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
22	ROX	MBA_MCBERRPTQ_MBA_INJQ_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 5
23	ROX	MBA_MCBERRPTQ_MBA_WRD_MODE_PE: WRD SCOM Register Parity Error linked to MBAFIR bit 6
24	ROX	MBA_MCBERRPTQ_MBMACAQ_PE: Maint Address SCOM Register Parity Error linked to MBAFIR bit 6
25	ROX	MBA_MCBERRPTQ_MBMCTQ_PE: Maint Command Type SCOM Register Parity Error linked to MBAFIR bit 6
26:63	ROX	MBA_MCBERRPTQ_RESERVED_26_63: RESERVED

Register Name	*Trace Array High Data Register*
Mnemonic	TCM.TRA.MBA23TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	00000000030110C0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	*Trace Array Low Data Register*
Mnemonic	TCM.TRA.MBA23TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	00000000030110C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	*Configuration Of CC Counters*
Mnemonic	TCM.SYNC_CONFIG
Address	0000000003030000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ISLE_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from chiplet
1	RW	PCB_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from pcb
2	RW	CLKSTP_SYNC_EN: stop clocks aligned to sync pulse
3	RW	EDRAM_XSTOP_MASK_B: mask for clockstop of eDRAM clock on any xstop
4	RW	PLL_XSTOP_MASK_B: mask for clockstop of pll clock on any xstop
5	RW	LOCAL_XSTOP_MASK_B: mask for clockstop of all island clocks on local xstop from chiplet
6	RW	DISABLE_PCB_ITR: disable interrupt generation within CC
7	RW	USE_SYNC_FOR_SCAN: if set, use opcg initial alignment for scan requests
8	RW	KEEP_EDRAM_ON_XSTOP: keep eDRAM enabled when a checkstop occurs
9	RW	TRIGGER_OPCG_ON_XSTOP: trigger opcg on xstop instead of performing clockstop

Bits	PCB	Field Mnemonic: Description
10	RW	SEL_EXT_OPCG_TRIGGER: select external OPCG trigger (set OPCG in slave mode)
11	RW	LISTEN_TO_SYNC_PULSE: enable phase counter synchronization by sync_pulse signal
12	RW	SYNC_CLK_START_ENABLE: enable clk start driven by tc_sync_clk_stop (falling edge)
13	RW	SYNC_CLK_STOP_ENABLE: enable clk stop driven by tc_sync_clk_stop (rising_edge)
14	RWX_WOR	CHIP_PROTECTION_ENABLE: Memory Buffer only - can only be set, but not cleared via PCB. When this bit is SET, no clock starts are possible
15	RW	SPARE15: spare
16	RW	SPARE16: spare
17	RW	SPARE17: spare
18	RW	SPARE18: spare
19	RW	SPARE19: spare
20	RW	SPARE20: spare

Register Name	***Counter Offset***
Mnemonic	TCM.PHASE_SHADOW
Address	0000000003030001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RWX	PHASE_COUNT_SHADOW_Q: offset for sync counter
6	RO	constant=0b0

Register Name	***OPCG Control Register 0***
Mnemonic	TCM.OPCG_REG0
Address	0000000003030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), runn-mode: loopcnt(4:6)
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)

Bits	PCB	Field Mnemonic: Description
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count (l = 1-2^28 (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	***OPCG Control Register 1***
Mnemonic	TCM.OPCG_REG1
Address	0000000003030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1
4:43	RW	FUNC_CAPT_INSTR_F: BIST mode: functional capture Instr 0-7 f domain (sl, nsl, ary, sg, fce)
44:63	RW	FUNC_CAPT_INSTR_FBY2: BIST mode: functional capture Instr 0-3 f/2 domain (sl, nsl, ary, sg, fce)

Register Name	***OPCG Control Register 2***
Mnemonic	TCM.OPCG_REG2
Address	0000000003030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	SCAN_CLK_USE_EVEN: BIST mode: Generate scan clock in f odd cycle. runn-mode: run one additional clock in f domain
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill and SNOP runn-mode: OPCG engine controls start_abist (overrides GP0 setting)
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	*Opcg Start Register*
Mnemonic	TCM.OPCG_REG3
Address	0000000003030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence)
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse)
2	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse)
3:4	RW	ALIGN_SOURCE_SELECT: 0: use inopa setting from opcg_reg0, 1: use rising edge of sync pulse, 2: use input from unit (for AVP)
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: set to 0 for prpg always on, else seed
20	RW	EXTEND_INOPW_ENOPW: extend I/ENOPW: add 256 cycles if i/enop>0, else 257+max i/enop
21	RW	EXTEND_SNOPW: add 256 cycles if snop>0, else 257+max snop
22	RW	FORCE_SG_HIGH_DURING_SNOP: force sg high during snop
23:31	RW	CHKSW: reserved for debug switch (keep 0 unless chows required)
32:43	RW	PRPG_A_VAL: a value for PRPG aperture
44:55	RW	PRPG_B_VAL: b value for PRPG aperture
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end)
57:63	RW	SPARE3: spares

Register Name	*Start/stop Of Clocks*
Mnemonic	TCM.CLK_REGION
Address	0000000003030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	constant=0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)
5	RWX	CLOCK_REGION_FASTUNIT0: for clock region memn
6	RWX	CLOCK_REGION_FASTUNIT1: for clock region mems
7	RWX	CLOCK_REGION_UNIT2: for clock region mte
8	RWX	CLOCK_REGION_UNIT3: for clock region ddrn
9	RWX	CLOCK_REGION_UNIT4: for clock region ddrs
10	RWX	CLOCK_REGION_UNIT5: for clock region unit5 region is UNUSED
11	RWX	CLOCK_REGION_PLL: for clock region pll region is UNUSED
12:19	RO	constant=0b00000000
20	RWX	SEL_THOLD_SL: select sl tholds

Bits	PCB	Field Mnemonic: Description
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name	***Scan Region And Type***
Mnemonic	TCM.SCANSELQ
Address	0000000003030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b000
3	RW_WCLRPART	SCANSEL_CLK_VITL: scan clock region vitl (Vital = Clock)
4	RWX	SCANSEL_CLK_PERV: scan clock region perv (Pervasive)
5	RWX	SCANSEL_CLK_FASTUNIT0: scan clock region memn
6	RWX	SCANSEL_CLK_FASTUNIT1: scan clock region mems
7	RWX	SCANSEL_CLK_UNIT2: scan clock region mte
8	RWX	SCANSEL_CLK_UNIT3: scan clock region ddrn
9	RWX	SCANSEL_CLK_UNIT4: scan clock region ddrs
10	RWX	SCANSEL_CLK_UNIT5: scan clock region unit5 region is UNUSED
11	RWX	SCANSEL_CLK_PLL: scan clock region pll region is UNUSED
12:19	RO	constant=0b00000000
20	RW	SCANSEL_FUNC: scan chain func (functional)
21	RW	SCANSEL_CFG: scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: scan chain ccfg / gptr (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: scan chain regf (register files)
24	RW	SCANSEL_LBIST: scan chain lbst (LBIST)
25	RW	SCANSEL_ABIST: scan chain abst (ABIST)
26	RW	SCANSEL_REPR: scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: scan chain time (Array Timing)
28	RW	SCANSEL_BNDY_FARY: scan chain bndy (Boundary IOs)
29	RW	SCANSEL_FARR: scan chain farr (fast array unload)
30	RW	SCANSEL_CMSK: scan chain cmsk (lbist channel mask)

Register Name	***Clocks Running***
Mnemonic	TCM.CLOCK_STAT
Address	0000000003030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: status of perv func_sl_thold 0=run, 1=stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: status of perv func_nsl_thold 0=run, 1=stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: status of perv ary_nsl_thold 0=run, 1=stop
3	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_SL: status of memn_odd func_sl_thold 0=run, 1=stop
4	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_SL: status of memn_even func_sl_thold 0=run, 1=stop
5	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_NSL: status of memn_odd func_nsl_thold 0=run, 1=stop
6	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_NSL: status of memn_even func_nsl_thold 0=run, 1=stop
7	ROX	CLOCK_STATUS_FASTUNIT0_ODD_ARY_NSL: status of memn_odd ary_nsl_thold 0=run, 1=stop
8	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_ARY_NSL: status of memn_even ary_nsl_thold 0=run, 1=stop
9	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_SL: status of mems_odd func_sl_thold 0=run, 1=stop
10	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_SL: status of mems_even func_sl_thold 0=run, 1=stop
11	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_NSL: status of mems_odd func_nsl_thold 0=run, 1=stop
12	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_NSL: status of mems_even func_nsl_thold 0=run, 1=stop
13	ROX	CLOCK_STATUS_FASTUNIT1_ODD_ARY_NSL: status of mems_odd ary_nsl_thold 0=run, 1=stop
14	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_ARY_NSL: status of mems_even ary_nsl_thold 0=run, 1=stop
15	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of mte func_sl_thold 0=run, 1=stop
16	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of mte func_nsl_thold 0=run, 1=stop
17	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of mte ary_nsl_thold 0=run, 1=stop
18	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of ddrn func_sl_thold 0=run, 1=stop
19	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of ddrn func_nsl_thold 0=run, 1=stop
20	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of ddrn ary_nsl_thold 0=run, 1=stop
21	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of ddrs func_sl_thold 0=run, 1=stop
22	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of ddrs func_nsl_thold 0=run, 1=stop
23	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of ddrs ary_nsl_thold 0=run, 1=stop
24	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of unit5 func_sl_thold 0=run, 1=stop region is UNUSED
25	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of unit5 func_nsl_thold 0=run, 1=stop region is UNUSED
26	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of unit5 ary_nsl_thold 0=run, 1=stop region is UNUSED
27	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of pll func_sl_thold 0=run, 1=stop region is UNUSED
28	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of pll func_nsl_thold 0=run, 1=stop region is UNUSED
29	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of pll ary_nsl_thold 0=run, 1=stop region is UNUSED
30:63	RO	constant=0b11111111111111111111111111111111

Register Name	*Error Status Of CC*
Mnemonic	TCM.ERROR_STATUS
Address	0000000003030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed

Bits	PCB	Field Mnemonic: Description
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: scan collision - high when scan protection error occurred
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error - during test its ok, but in system its a error
13	RWX	PHASE_CNT_CORRUPTED: phase hold counter corruption detected
14:15	RWX	CC_PAR_ERR: parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: parity error in GP0 register
17	RWX	SECURITY_VIOLATION: security_violation - when Chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name	***CC Protect Mode Register***
Mnemonic	TCM.CC_PROTECT_MODE_REG
Address	00000000030303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TCM.CC_ATOMIC_LOCK_REG
Address	00000000030303FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	CC_ATOMIC_ID: Atomic ID

Register Name	***Global Checkstop FIR***
Mnemonic	TCM.XFIR
Address	0000000003040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: unused
3	RWX	XFIR_IN3: xstop pervasive unit
4	RWX	XFIR_IN4: unused
5	RWX	XFIR_IN5: xstop from memn0
6	RWX	XFIR_IN6: xstop from memn1
7	RWX	XFIR_IN7: xstop from mems0
8	RWX	XFIR_IN8: xstop from mems1
9	RWX	XFIR_IN9: xstop from ddrn
10	RWX	XFIR_IN10: xstop from ddrs
11	RWX	XFIR_IN11: xstop from fbistm
12	RWX	XFIR_IN12: xstop from mba01 secure fir
13	RWX	XFIR_IN13: xstop from mba23 secure fir
14	RWX	XFIR_IN14: unused
15:25	RWX	XFIR_IN15: unused
26	RWX	XFIR_IN26: xstop on debug trigger

Register Name	***Global Recoverable FIR***
Mnemonic	TCM.RFIR
Address	0000000003040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: unused
1	ROX	LFIR_RECOV_ERR: error from local LFIR
2:23	ROX	RFIR_IN: recoverable errors: same mapping as XFIR(4:25)

Register Name	***FIR Mask***
Mnemonic	TCM.FIR_MASK
Address	0000000003040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit
1	RW	FIR_MASK_IN1: mask for xfir PCB status bit
2	RW	FIR_MASK_IN2: mask for xfir IO status bit
3	RW	FIR_MASK_IN3: mask for LFIR status bit
4:26	RW	FIR_MASK_IN4: masks for XFIR and RFIR

Register Name	*Special Attention*
Mnemonic	TCM.EPS.FIR.SPATTN
Address	0000000003040004 (PCB) 0000000003040005 (PCB1) 0000000003040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: MEM Chiplet Only: Special Attention from MBA01
1	ROX	NCX	NCX	SPATTN_IN1: MEM Chiplet Only: Special Attention from MBA23
2:9	ROX	NCX	NCX	SPATTN_IN2: unused special attentions

Register Name	*Special Attention Mask*
Mnemonic	TCM.EPS.FIR.SPA_MASK
Address	0000000003040007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask

Register Name	*Mode Register*
Mnemonic	TCM.EPS.FIR.MODE_REG
Address	0000000003040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable

Bits	PCB	Field Mnemonic: Description
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: unused

Register Name	***Local FIR***
Mnemonic	TCM.LOCAL_FIR
Address	000000000304000A (PCB) 000000000304000B (PCB1) 000000000304000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (critical Trip error)
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (fatal Trip error)
10	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Thermal (Voltage trip error)
11	RWX	WOX_AND	WOX_OR	FIR_IN11: local errors from mba01 Trace Array (error)
12	RWX	WOX_AND	WOX_OR	FIR_IN12: local errors from mba01 Trace Array (error)
13	RWX	WOX_AND	WOX_OR	FIR_IN13: local errors from mba23 Trace Array (error)
14	RWX	WOX_AND	WOX_OR	FIR_IN14: local errors from mba23 Trace Array (error)
15:39	RWX	WOX_AND	WOX_OR	FIR_IN15: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	***Local FIR Mask***
Mnemonic	TCM.EPS.FIR.LOCAL_FIR_MASK
Address	000000000304000D (PCB) 000000000304000E (PCB1) 000000000304000F (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

Register Name	***Local FIR Action0***
Mnemonic	TCM.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000003040010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name	***Local FIR Action1***
Mnemonic	TCM.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000003040011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name	***DTS Thermal Sensor Results***
Mnemonic	TCM.EPS.THERM.DTS_RESULT0
Address	0000000003050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***DTS Trace Results***
Mnemonic	TCM.EPS.THERM.DTS_TRC_RESULT
Address	0000000003050003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.

Bits	PCB	Field Mnemonic: Description
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant=0b000
48:63	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.

Register Name	***DTS0-1 Bit 0 - 15: Temperature Result DTS0, Bit 16 - 31: Temperature Result DTS1(available Only In NEST Chiplet),***
Mnemonic	TCM.EPS.THERM.ENC_CPM_RESULT0
Address	0000000003050008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.
32:55	RO	constant=0b00000000000000000000000

Register Name	***Voltage Sensor Results***
Mnemonic	TCM.EPS.THERM.VOLT_READ0
Address	000000000305000B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	Reserved field (Access type is volt_data0)
16:31	ROX	Reserved field (Access type is volt_data1)
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	***CPM & DTS Enables And Controls***
Mnemonic	TCM.EPS.THERM.THERM_MODE_REG
Address	000000000305000F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	THERM_DIS_CPM_BUBBLE_CORR: critical path result bubble correction active
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables 1xx: trip0 - warning x1x: trip1 - critical xx1: trip2 - fatal

Bits	PCB	Field Mnemonic: Description
5	RW	THERM_DTS_SAMPLE_ENA: 0: no dts sampling, 1: dts sampling is enabled and below counter compare match can occur.
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is feed into an 18 Bit counter, with the therm_sample_pulse_cnt it is possible to select a highorder bit of the counter to enable a resolutions of sampling dtss between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a dts sample 0000: 16 ms 0001: 8 ms 0010: 4 ms 0011: 2 ms 0100: 1 ms 0101: 0.5 ms 0110: 250 us 0111: 125 us 1000: 62 .5us 1001: 31.3 us 1010: 15.6 us 1011: 7.8 us 1100: 3.9 us 1101: 2 us 1110: 1 us 1111: 0.5 us
10:11	RW	THERM_THRES_MODE_ENA: forces max or min mode in threshold unit: 00: is off 11: is illegal 10: max mode 01: min mode
12	RW	DTS_TRIGGER_MODE: unused
13	RW	DTS_TRIGGER_SEL: unused
14:15	RW	THERM_MODE_UNUSED: unused
16:19	RW	THERM_DTS_READ_SEL: selects which dts result will be provided with pcb read addr_v(4): 000: DTS 0 001: DTS 1 010: DTS 2 011: DTS 3 100: DTS 4 111: Worst Case Sensor
20:21	RW	THERM_DTS_ENABLE: dts enables: 1xxxx: DTS 0 available x1xx: DTS 1 available
22:34	RO	constant=0b0000000000000
35:36	RW	THERM_CPM_ENABLE: com enables

Register Name	***Skitter Control Register***
Mnemonic	TCM.EPS.THERM.SKITTER_MODE_REG
Address	0000000003050010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: forces skitter to hold current sample
1	RW	DISABLE_SKITTER_STICKINESS: if '0' accumulation mode, '1' samples new value each cycle and resets sticky value
2:3	RW	SKITTER_MODE_UNUSED1: unused

Bits	PCB	Field Mnemonic: Description
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0 bit1: _on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0 bit1: reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: selects guts to measure: 00: guts1 01: guts2 10: guts3 11: guts4
10:43	RO	constant=0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: forces skitter to hold current sample on dbg trigger, this has highest priority
45	ROX	SKITTER_DATA_V_LT: if '1' the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 pcb reads

Register Name	***Error Injection Control Register***
Mnemonic	TCM.EPS.THERM.INJECT_REG
Address	0000000003050011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection 01: warning trip level injection 10: critical trip level injection 11: fatal trip level injection
2:3	RW	THERM_INJECT_MODE: 00: no injection 01: injection on the next dts sample 10: solid injection for the next dts samples till bit setting changes 11: not used

Register Name	***Control / Force Reset Register***
Mnemonic	TCM.EPS.THERM.CONTROL_REG
Address	0000000003050012 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	WO_1P	Reserved field (Access type is reset_trip_history)
1	WO_1P	Reserved field (Access type is reset_sample_pulse_cnt)
2	WO_1P	Reserved field (Access type is f_reset_cpm_rd)
3	WO_1P	Reserved field (Access type is f_reset_cpm_wr)
4	WO_1P	Reserved field (Access type is reset_sample_dts)
5	WO_1P	Reserved field (Access type is force_sample_dts)
6	WO_1P	Reserved field (Access type is force_sample_dts_interruptible)

Bits	PCB	Field Mnemonic: Description
7	WO_1P	Reserved field (Access type is force_reset_thres_l1results)
8	WO_1P	Reserved field (Access type is force_reset_thres_l2results)
9	WO_1P	Reserved field (Access type is force_reset_thres_l3results)
10	WO_1P	Reserved field (Access type is force_measure_volt_interruptible)
11	WO_1P	Reserved field (Access type is force_reset_measure_volt)
12	WO_1P	Reserved field (Access type is force_shift_sensor)

Register Name	***Thermal Error Status Register***
Mnemonic	TCM.EPS.THERM.ERR_STATUS_REG
Address	0000000003050013 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is serial_shiftcnt_modereg_parity_err_hold)
1	ROX	Reserved field (Access type is therm_modereg_parity_err_hold)
2	ROX	Reserved field (Access type is skitter_modereg_parity_err_hold)
3	ROX	Reserved field (Access type is skitter_forcereg_parity_err_hold)
4	ROX	Reserved field (Access type is scan_init_version_reg_parity_err_hold)
5	ROX	Reserved field (Access type is volt_modereg_parity_err_hold)
6	ROX	Reserved field (Access type is skitter_clksrcreg_parity_err_hold)
7	ROX	Reserved field (Access type is count_state_err_hold)
8	ROX	Reserved field (Access type is run_state_err_hold)
9	ROX	Reserved field (Access type is thres_therm_state_err_hold)
10	ROX	Reserved field (Access type is thres_therm_overflow_err_hold)
11	ROX	Reserved field (Access type is shifter_parity_err_hold)
12	ROX	Reserved field (Access type is shifter_valid_err_hold)
13	ROX	Reserved field (Access type is timeout_err_hold)
14	ROX	Reserved field (Access type is f_skitter_err_hold)
15	ROX	Reserved field (Access type is pcb_err_hold_out)
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: serial shift count parity error mask
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: therm mode reg parity error mask
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: skitter mode register parity error mask
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: skitter force register parity error mask
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: scan init version register parity error mask
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: volt mode reg parity error mask
22	RO	constant=0b0
23	ROX	COUNT_STATE_ERR_MASK: count state machine error mask
24	ROX	RUN_STATE_ERR_MASK: run state machine error mask
25	ROX	THRES_STATE_ERR_MASK: thres state machine error mask
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask

Bits	PCB	Field Mnemonic: Description
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask
30	ROX	F_SKITTER_READ_ERR_MASK: force skitter read one hot error mask
31	ROX	PCB_ERR_MASK: pervasive control bus error mask
32:39	RO	constant=0b00000000
40:43	ROX	Reserved field (Access type is count_state_lt)
44:46	ROX	Reserved field (Access type is run_state_lt)
47	ROX	Reserved field (Access type is shift_dts_lt)
48	ROX	Reserved field (Access type is shift_volt_lt)
49:50	ROX	Reserved field (Access type is read_state_lt)
51:54	ROX	Reserved field (Access type is write_state_lt)
55	ROX	Reserved field (Access type is sample_dts_lt)
56	ROX	Reserved field (Access type is measure_volt_lt)
57	ROX	Reserved field (Access type is read_cpm_lt)
58	ROX	Reserved field (Access type is write_cpm_lt)
59	ROX	Reserved field (Access type is unused)
60:63	RO	constant=0b0000

Register Name	***Skitter Force Read Register***
Mnemonic	TCM.EPS.THERM.SKITTER_FORCE_REG
Address	0000000003050014 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter

Register Name	***Voltage Sensor Enables And Controls***
Mnemonic	TCM.EPS.THERM.VOLT_MODE_REG
Address	0000000003050015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	VOLT_MEASURE_ENA: enables the measurement of voltage sensor
1	RW	VOLT_TRIP_ENA: enables the trip of voltage sensor
2:3	RW	VOLT_ENABLE: Voltage sensor enables 1xxxx:voltage sensor0 available

Register Name	***Skitter Clock Src Control Register***
Mnemonic	TCM.EPS.THERM.SKITTER_CLKSRC_REG
Address	0000000003050016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: selects clock to measure: 000: local mesh clock 001: external pin skitter_c1_1_in 010: local d1clk only if d_mode = 1 011: external pin skitter_c1_2_in 100: local lclk only if d_mode = 1 101: external pin skitter_c1_3_in 110: unused 111: external pin skitter_c1_4_in
3:35	RO	constant=0b00000000000000000000000000000000

Register Name	***Skitter Data Register Read Bit0:63***
Mnemonic	TCM.EPS.THERM.SKITTER_DATA0
Address	0000000003050019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Skitter Data Register Read Bit32:95***
Mnemonic	TCM.EPS.THERM.SKITTER_DATA1
Address	000000000305001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Skitter Data Register Read Bit64:127***
Mnemonic	TCM.EPS.THERM.SKITTER_DATA2
Address	000000000305001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	***Timestamp Counter Read***
Mnemonic	TCM.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000000305001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.

Register Name	***Contains The Slave's Primary Address***
Mnemonic	TPTOP.NET.PCBSLMEM.PRIMARY_ADDRESS_REG
Address	00000000030F0000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	***Multicast Group 1***
Mnemonic	TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_1
Address	00000000030F0001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	***Multicast Group 2***
Mnemonic	TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_2
Address	00000000030F0002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name	***Multicast Group 3***
Mnemonic	TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_3
Address	00000000030F0003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	***Multicast Group 4***
Mnemonic	TPTOP.NET.PCBSLMEM.MULTICAST_GROUP_4
Address	00000000030F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	***Timeout Select Register***
Mnemonic	TPTOP.NET.PCBSLMEM.TIMEOUT_REG
Address	00000000030F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	***Assist Interrupt Register***
Mnemonic	TPTOP.NET.PCBSLMEM.ASSIST_INTERRUPT_REG
Address	00000000030F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

Register Name	*GP3 Register (NA In PERV CPLT)*
Mnemonic	TPTOP.NET.PCBSLMEM.GP3_REG
Address	00000000030F0012 (PCB) 00000000030F0013 (PCB1) 00000000030F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2:4	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
5	RWX	RWX_WAND	RWX_WOR	NCLK_NODIV: Force cache_nclk to equal nclk (for test only).
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	FENCE2_EN: Fencing signal for chiplet.
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
22	RWX	RWX_WAND	RWX_WOR	RESCLK_FLUSH: Flush for resonant clocking.
23	RWX	RWX_WAND	RWX_WOR	RESCLK_OVERRIDE_VALUE: Override value for resonant clocking.
24	RWX	RWX_WAND	RWX_WOR	DPHY_PLL: dphy pll
25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	FSYNC_ENABLE: Set the 'Frame Synchronous (Geared) Clocking Mode' .
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
30	RWX	RWX_WAND	RWX_WOR	CHIPET_RI: Chiplet RI
31	RWX	RWX_WAND	RWX_WOR	CHIPET_DI1: Chiplet DI1

Register Name	*Skew Adjust Data*
Mnemonic	TPTOP.NET.PCBSLMEM.CLK_ADJ_REG
Address	00000000030F0015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	*Clock Adjust Config*
Mnemonic	TPTOP.NET.PCBSLMEM.CLK_ADJ_SET
Address	00000000030F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	*Vital Scan Out*
Mnemonic	TPTOP.NET.PCBSLMEM.VITAL_SCAN_OUT
Address	00000000030F0017 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	*Chiplet Heartbeat Register*
Mnemonic	TPTOP.NET.PCBSLMEM.HEARTBEAT_REG
Address	00000000030F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

Register Name	*Lock Indications From PLLs*
Mnemonic	TPTOP.NET.PCBSLMEM.PLL_LOCK_REG
Address	00000000030F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	***Attn Interrupt***
Mnemonic	TPTOP.NET.PCBSLMEM.ATTN_INTERRUPT_REG
Address	00000000030F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	***Recov Interrupt***
Mnemonic	TPTOP.NET.PCBSLMEM.RECOV_INTERRUPT_REG
Address	00000000030F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	***Xstop Interrupt***
Mnemonic	TPTOP.NET.PCBSLMEM.XSTOP_INTERRUPT_REG
Address	00000000030F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

Register Name	***Slave Config Register***
Mnemonic	TPTOP.NET.PCBSLMEM.SLAVE_CONFIG_REG
Address	00000000030F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting

Bits	PCB	Field Mnemonic: Description
13:15	RW	

Register Name	*Error Capture Register*
Mnemonic	TPTOP.NET.PCBSLMEM.ERROR_REG
Address	00000000030F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad

Bits	PCB	Field Mnemonic: Description
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name	***Hang Pulse Generation Register 0***
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_0_REG
Address	00000000030F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 1***
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_1_REG
Address	00000000030F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Hang Pulse Generation Register 2***
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_2_REG
Address	00000000030F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 3*
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_3_REG
Address	00000000030F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 4*
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_4_REG
Address	00000000030F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 5*
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_5_REG
Address	00000000030F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	*Hang Pulse Generation Register 6*
Mnemonic	TPTOP.NET.PCBSLMEM.HANG_PULSE_6_REG
Address	00000000030F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2^value * (precounter_reg+1) / pcb_freq, 34>=value>0
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	***Divider For Hang Counter Clock***
Mnemonic	TPTOP.NET.PCBSLMEM.PRE_COUNTER_REG
Address	00000000030F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

Register Name	***Protect Mode Register***
Mnemonic	TPTOP.NET.PCBSLMEM.PROTECT_MODE_REG
Address	00000000030F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	***Atomic Lock Register***
Mnemonic	TPTOP.NET.PCBSLMEM.ATOMIC_LOCK_REG
Address	00000000030F03FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

6. PCB Slave 3: DPHY01 Indirect Registers

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR0	0x800040000301143F	2521
DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR1	0x800044000301143F	2531
DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR2	0x800048000301143F	2541
DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR3	0x80004C000301143F	2551
DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR0	0x800140000301143F	3218
DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR1	0x800144000301143F	3228
DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR2	0x800148000301143F	3238
DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR3	0x80014C000301143F	3248
DPHY01.DDRPHY_ADR_DELAY0_P0_ADR0	0x800040040301143F	2523
DPHY01.DDRPHY_ADR_DELAY0_P0_ADR1	0x800044040301143F	2533
DPHY01.DDRPHY_ADR_DELAY0_P0_ADR2	0x800048040301143F	2543
DPHY01.DDRPHY_ADR_DELAY0_P0_ADR3	0x80004C040301143F	2553
DPHY01.DDRPHY_ADR_DELAY0_P1_ADR0	0x800140040301143F	3220
DPHY01.DDRPHY_ADR_DELAY0_P1_ADR1	0x800144040301143F	3230
DPHY01.DDRPHY_ADR_DELAY0_P1_ADR2	0x800148040301143F	3240
DPHY01.DDRPHY_ADR_DELAY0_P1_ADR3	0x80014C040301143F	3250
DPHY01.DDRPHY_ADR_DELAY1_P0_ADR0	0x800040050301143F	2523
DPHY01.DDRPHY_ADR_DELAY1_P0_ADR1	0x800044050301143F	2533
DPHY01.DDRPHY_ADR_DELAY1_P0_ADR2	0x800048050301143F	2543
DPHY01.DDRPHY_ADR_DELAY1_P0_ADR3	0x80004C050301143F	2553
DPHY01.DDRPHY_ADR_DELAY1_P1_ADR0	0x800140050301143F	3220
DPHY01.DDRPHY_ADR_DELAY1_P1_ADR1	0x800144050301143F	3230
DPHY01.DDRPHY_ADR_DELAY1_P1_ADR2	0x800148050301143F	3240
DPHY01.DDRPHY_ADR_DELAY1_P1_ADR3	0x80014C050301143F	3250
DPHY01.DDRPHY_ADR_DELAY2_P0_ADR0	0x800040060301143F	2523
DPHY01.DDRPHY_ADR_DELAY2_P0_ADR1	0x800044060301143F	2533
DPHY01.DDRPHY_ADR_DELAY2_P0_ADR2	0x800048060301143F	2543
DPHY01.DDRPHY_ADR_DELAY2_P0_ADR3	0x80004C060301143F	2553
DPHY01.DDRPHY_ADR_DELAY2_P1_ADR0	0x800140060301143F	3220
DPHY01.DDRPHY_ADR_DELAY2_P1_ADR1	0x800144060301143F	3230
DPHY01.DDRPHY_ADR_DELAY2_P1_ADR2	0x800148060301143F	3240
DPHY01.DDRPHY_ADR_DELAY2_P1_ADR3	0x80014C060301143F	3250
DPHY01.DDRPHY_ADR_DELAY3_P0_ADR0	0x800040070301143F	2524
DPHY01.DDRPHY_ADR_DELAY3_P0_ADR1	0x800044070301143F	2534
DPHY01.DDRPHY_ADR_DELAY3_P0_ADR2	0x800048070301143F	2544
DPHY01.DDRPHY_ADR_DELAY3_P0_ADR3	0x80004C070301143F	2554
DPHY01.DDRPHY_ADR_DELAY3_P1_ADR0	0x800140070301143F	3221
DPHY01.DDRPHY_ADR_DELAY3_P1_ADR1	0x800144070301143F	3231
DPHY01.DDRPHY_ADR_DELAY3_P1_ADR2	0x800148070301143F	3241
DPHY01.DDRPHY_ADR_DELAY3_P1_ADR3	0x80014C070301143F	3251
DPHY01.DDRPHY_ADR_DELAY4_P0_ADR0	0x800040080301143F	2524
DPHY01.DDRPHY_ADR_DELAY4_P0_ADR1	0x800044080301143F	2534
DPHY01.DDRPHY_ADR_DELAY4_P0_ADR2	0x800048080301143F	2544
DPHY01.DDRPHY_ADR_DELAY4_P0_ADR3	0x80004C080301143F	2554
DPHY01.DDRPHY_ADR_DELAY4_P1_ADR0	0x800140080301143F	3221

Mnemonic	Address	Page
DPHY01.DDRPHY_ADR_DELAY4_P1_ADR1	0x800144080301143F	3231
DPHY01.DDRPHY_ADR_DELAY4_P1_ADR2	0x800148080301143F	3241
DPHY01.DDRPHY_ADR_DELAY4_P1_ADR3	0x80014C080301143F	3251
DPHY01.DDRPHY_ADR_DELAY5_P0_ADR0	0x800040090301143F	2525
DPHY01.DDRPHY_ADR_DELAY5_P0_ADR1	0x800044090301143F	2535
DPHY01.DDRPHY_ADR_DELAY5_P0_ADR2	0x800048090301143F	2545
DPHY01.DDRPHY_ADR_DELAY5_P0_ADR3	0x80004C090301143F	2555
DPHY01.DDRPHY_ADR_DELAY5_P1_ADR0	0x800140090301143F	3222
DPHY01.DDRPHY_ADR_DELAY5_P1_ADR1	0x800144090301143F	3232
DPHY01.DDRPHY_ADR_DELAY5_P1_ADR2	0x800148090301143F	3242
DPHY01.DDRPHY_ADR_DELAY5_P1_ADR3	0x80014C090301143F	3252
DPHY01.DDRPHY_ADR_DELAY6_P0_ADR0	0x8000400A0301143F	2525
DPHY01.DDRPHY_ADR_DELAY6_P0_ADR1	0x8000440A0301143F	2535
DPHY01.DDRPHY_ADR_DELAY6_P0_ADR2	0x8000480A0301143F	2545
DPHY01.DDRPHY_ADR_DELAY6_P0_ADR3	0x80004C0A0301143F	2555
DPHY01.DDRPHY_ADR_DELAY6_P1_ADR0	0x8001400A0301143F	3222
DPHY01.DDRPHY_ADR_DELAY6_P1_ADR1	0x8001440A0301143F	3232
DPHY01.DDRPHY_ADR_DELAY6_P1_ADR2	0x8001480A0301143F	3242
DPHY01.DDRPHY_ADR_DELAY6_P1_ADR3	0x80014C0A0301143F	3252
DPHY01.DDRPHY_ADR_DELAY7_P0_ADR0	0x8000400B0301143F	2525
DPHY01.DDRPHY_ADR_DELAY7_P0_ADR1	0x8000440B0301143F	2535
DPHY01.DDRPHY_ADR_DELAY7_P0_ADR2	0x8000480B0301143F	2545
DPHY01.DDRPHY_ADR_DELAY7_P0_ADR3	0x80004C0B0301143F	2555
DPHY01.DDRPHY_ADR_DELAY7_P1_ADR0	0x8001400B0301143F	3222
DPHY01.DDRPHY_ADR_DELAY7_P1_ADR1	0x8001440B0301143F	3232
DPHY01.DDRPHY_ADR_DELAY7_P1_ADR2	0x8001480B0301143F	3242
DPHY01.DDRPHY_ADR_DELAY7_P1_ADR3	0x80014C0B0301143F	3252
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR0	0x8000400C0301143F	2526
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR1	0x8000440C0301143F	2536
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR2	0x8000480C0301143F	2546
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR3	0x80004C0C0301143F	2556
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR0	0x8001400C0301143F	3223
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR1	0x8001440C0301143F	3233
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR2	0x8001480C0301143F	3243
DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR3	0x80014C0C0301143F	3253
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR0	0x800040010301143F	2521
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR1	0x800044010301143F	2531
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR2	0x800048010301143F	2541
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR3	0x80004C010301143F	2551
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR0	0x800140010301143F	3218
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR1	0x800144010301143F	3228
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR2	0x800148010301143F	3238
DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR3	0x80014C010301143F	3248
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR0	0x800040200301143F	2527
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR1	0x800044200301143F	2537
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR2	0x800048200301143F	2547
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR3	0x80004C200301143F	2557
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR0	0x800140200301143F	3224
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR1	0x800144200301143F	3234
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR2	0x800148200301143F	3244
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR3	0x80014C200301143F	3254

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DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR0	0x8000402103011 43F	2528
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR1	0x8000442103011 43F	2538
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR2	0x8000482103011 43F	2548
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR3	0x80004C2103011 43F	2558
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR0	0x8001402103011 43F	3225
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR1	0x8001442103011 43F	3235
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR2	0x8001482103011 43F	3245
DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR3	0x80014C2103011 43F	3255
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0	0x8000402A0301143F	2529
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1	0x8000442A0301143F	2539
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2	0x8000482A0301143F	2549
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3	0x80004C2A0301143F	2559
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0	0x8001402A0301143F	3226
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1	0x8001442A0301143F	3236
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2	0x8001482A0301143F	3246
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3	0x80014C2A0301143F	3256
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0	0x8000402B0301143F	2530
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1	0x8000442B0301143F	2540
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2	0x8000482B0301143F	2550
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3	0x80004C2B0301143F	2560
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0	0x8001402B0301143F	3227
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1	0x8001442B0301143F	3237
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2	0x8001482B0301143F	3247
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3	0x80014C2B0301143F	3257
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR0	0x8000401A0301143F	2527
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR1	0x8000441A0301143F	2537
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR2	0x8000481A0301143F	2547
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR3	0x80004C1A0301143F	2557
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR0	0x8001401A0301143F	3224
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR1	0x8001441A0301143F	3234
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR2	0x8001481A0301143F	3244
DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR3	0x80014C1A0301143F	3254
DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S0	0x8000803303011 43F	2564
DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S1	0x8000843303011 43F	2569
DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S0	0x8001803303011 43F	3261
DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S1	0x8001843303011 43F	3266
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S0	0x8000803603011 43F	2566
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S1	0x8000843603011 43F	2571
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S0	0x8001803603011 43F	3263
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S1	0x8001843603011 43F	3268
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S0	0x8000803703011 43F	2566
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S1	0x8000843703011 43F	2571
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S0	0x8001803703011 43F	3263
DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S1	0x8001843703011 43F	3268
DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S0	0x8000803503011 43F	2565
DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S1	0x8000843503011 43F	2571
DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S0	0x8001803503011 43F	3262
DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S1	0x8001843503011 43F	3268
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S0	0x8000803003011 43F	2561
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S1	0x8000843003011 43F	2567
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S0	0x8001803003011 43F	3258

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DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S1	0x8001843003011 43F	3264
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S0	0x8000803103011 43F	2562
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S1	0x8000843103011 43F	2567
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S0	0x8001803103011 43F	3259
DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S1	0x8001843103011 43F	3264
DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR0	0x8000402C03011 43F	2531
DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR1	0x8000442C03011 43F	2541
DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR2	0x8000482C03011 43F	2551
DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR3	0x80004C2C03011 43F	2561
DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR0	0x8001402C03011 43F	3228
DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR1	0x8001442C03011 43F	3238
DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR2	0x8001482C03011 43F	3248
DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR3	0x80014C2C03011 43F	3258
DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S0	0x8000803903011 43F	2566
DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S1	0x8000843903011 43F	2572
DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S0	0x8001803903011 43F	3263
DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S1	0x8001843903011 43F	3269
DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S0	0x8000803203011 43F	2563
DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S1	0x8000843203011 43F	2568
DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S0	0x8001803203011 43F	3260
DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S1	0x8001843203011 43F	3265
DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S0	0x8000803403011 43F	2564
DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S1	0x8000843403011 43F	2570
DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S0	0x8001803403011 43F	3261
DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S1	0x8001843403011 43F	3267
DPHY01.DDRPHY_APB_ATEST_MUX_SEL_P0	0x8000D0050301143F	2616
DPHY01.DDRPHY_APB_ATEST_MUX_SEL_P1	0x8001D0050301143F	3313
DPHY01.DDRPHY_APB_CONFIG0_P0	0x8000D0000301143F	2615
DPHY01.DDRPHY_APB_CONFIG0_P1	0x8001D0000301143F	3312
DPHY01.DDRPHY_APB_ERROR_MASK0_P0	0x8000D0020301143F	2616
DPHY01.DDRPHY_APB_ERROR_MASK0_P1	0x8001D0020301143F	3313
DPHY01.DDRPHY_APB_ERROR_STATUS0_P0	0x8000D0010301143F	2616
DPHY01.DDRPHY_APB_ERROR_STATUS0_P1	0x8001D0010301143F	3313
DPHY01.DDRPHY_APB_FIR_ERR0_P0	0x8000D0060301143F	2617
DPHY01.DDRPHY_APB_FIR_ERR0_P1	0x8001D0060301143F	3314
DPHY01.DDRPHY_APB_FIR_ERR1_P0	0x8000D0070301143F	2617
DPHY01.DDRPHY_APB_FIR_ERR1_P1	0x8001D0070301143F	3314
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_0	0x8000000203011 43F	1923
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_1	0x8000040203011 43F	2042
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_2	0x8000080203011 43F	2162
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_3	0x80000C0203011 43F	2282
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_4	0x8000100203011 43F	2402
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_0	0x8001000203011 43F	2619
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_1	0x8001040203011 43F	2739
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_2	0x8001080203011 43F	2859
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_3	0x80010C0203011 43F	2979
DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_4	0x8001100203011 43F	3099
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_0	0x8000000303011 43F	1923
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_1	0x8000040303011 43F	2043
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_2	0x8000080303011 43F	2163
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_3	0x80000C0303011 43F	2283

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DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_4	0x8000100303011 43F	2403
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_0	0x8001000303011 43F	2619
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_1	0x8001040303011 43F	2740
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_2	0x8001080303011 43F	2860
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_3	0x80010C0303011 43F	2980
DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_4	0x8001100303011 43F	3100
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_0	0x8000007C0301143F	1967
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_1	0x8000047C0301143F	2087
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_2	0x8000087C0301143F	2207
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_3	0x80000C7C0301143F	2327
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_4	0x8000107C0301143F	2447
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_0	0x8001007C0301143F	2664
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_1	0x8001047C0301143F	2784
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_2	0x8001087C0301143F	2904
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_3	0x80010C7C0301143F	3024
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_4	0x8001107C0301143F	3144
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_0	0x8000017C0301143F	1991
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_1	0x8000057C0301143F	2111
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_2	0x8000097C0301143F	2231
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_3	0x80000D7C0301143F	2351
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_4	0x8000117C0301143F	2471
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_0	0x8001017C0301143F	2688
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_1	0x8001057C0301143F	2808
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_2	0x8001097C0301143F	2928
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_3	0x80010D7C0301143F	3048
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_4	0x8001117C0301143F	3168
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_0	0x8000027C0301143F	2015
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_1	0x8000067C0301143F	2135
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_2	0x80000A7C0301143F	2255
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_3	0x80000E7C0301143F	2375
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_4	0x8000127C0301143F	2495
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_0	0x8001027C0301143F	2712
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_1	0x8001067C0301143F	2832
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_2	0x80010A7C0301143F	2952
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_3	0x80010E7C0301143F	3072
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_4	0x8001127C0301143F	3192
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_0	0x8000037C0301143F	2040
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_1	0x8000077C0301143F	2160
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_2	0x80000B7C0301143F	2280
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_3	0x80000F7C0301143F	2400
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_4	0x8000137C0301143F	2520
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_0	0x8001037C0301143F	2737
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_1	0x8001077C0301143F	2857
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_2	0x80010B7C0301143F	2977
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_3	0x80010F7C0301143F	3097
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_4	0x8001137C0301143F	3217
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_0	0x8000007D0301143F	1967
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_1	0x8000047D0301143F	2087
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_2	0x8000087D0301143F	2207
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_3	0x80000C7D0301143F	2327
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_4	0x8000107D0301143F	2447

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DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_0	0x8001007D0301143F	2664
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_1	0x8001047D0301143F	2784
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_2	0x8001087D0301143F	2904
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_3	0x80010C7D0301143F	3024
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_4	0x8001107D0301143F	3144
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_0	0x8000017D0301143F	1991
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_1	0x8000057D0301143F	2111
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_2	0x8000097D0301143F	2231
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_3	0x80000D7D0301143F	2351
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_4	0x8000117D0301143F	2471
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_0	0x8001017D0301143F	2688
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_1	0x8001057D0301143F	2808
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_2	0x8001097D0301143F	2928
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_3	0x80010D7D0301143F	3048
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_4	0x8001117D0301143F	3168
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_0	0x8000027D0301143F	2016
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_1	0x8000067D0301143F	2136
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_2	0x80000A7D0301143F	2256
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_3	0x80000E7D0301143F	2376
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_4	0x8000127D0301143F	2496
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_0	0x8001027D0301143F	2713
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_1	0x8001067D0301143F	2833
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_2	0x80010A7D0301143F	2953
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_3	0x80010E7D0301143F	3073
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_4	0x8001127D0301143F	3193
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_0	0x8000037D0301143F	2040
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_1	0x8000077D0301143F	2160
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_2	0x80000B7D0301143F	2280
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_3	0x80000F7D0301143F	2400
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_4	0x8000137D0301143F	2520
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_0	0x8001037D0301143F	2737
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_1	0x8001077D0301143F	2857
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_2	0x80010B7D0301143F	2977
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_3	0x80010F7D0301143F	3097
DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_4	0x8001137D0301143F	3217
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_0	0x8000000000301143F	1921
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_1	0x8000040000301143F	2041
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_2	0x8000080000301143F	2161
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_3	0x80000C000301143F	2281
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_4	0x8000100000301143F	2401
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_0	0x8001000000301143F	2618
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_1	0x8001040000301143F	2738
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_2	0x8001080000301143F	2858
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_3	0x80010C000301143F	2978
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_4	0x8001100000301143F	3098
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_0	0x8000000010301143F	1922
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_1	0x8000040010301143F	2041
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_2	0x8000080010301143F	2161
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_3	0x80000C010301143F	2281
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_4	0x8000100010301143F	2401
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_0	0x8001000010301143F	2618

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DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_1	0x800104010301143F	2738
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_2	0x800108010301143F	2858
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_3	0x80010C010301143F	2978
DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_4	0x800110010301143F	3098
DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_0	0x8000000B0301143F	1930
DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_1	0x8000040B0301143F	2050
DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_2	0x8000080B0301143F	2170
DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_3	0x80000C0B0301143F	2290
DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_4	0x8000100B0301143F	2410
DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_0	0x8001000B0301143F	2627
DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_1	0x8001040B0301143F	2747
DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_2	0x8001080B0301143F	2867
DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_3	0x80010C0B0301143F	2987
DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_4	0x8001100B0301143F	3107
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0	0x8000006F0301143F	1960
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1	0x8000046F0301143F	2080
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2	0x8000086F0301143F	2200
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3	0x80000C6F0301143F	2320
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4	0x8000106F0301143F	2440
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0	0x8001006F0301143F	2657
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1	0x8001046F0301143F	2777
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2	0x8001086F0301143F	2897
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3	0x80010C6F0301143F	3017
DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4	0x8001106F0301143F	3137
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_0	0x8000000080301143F	1929
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_1	0x8000040080301143F	2048
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_2	0x8000080080301143F	2168
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_3	0x80000C080301143F	2288
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_4	0x8000100080301143F	2408
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_0	0x8001000080301143F	2625
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_1	0x800104080301143F	2745
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_2	0x800108080301143F	2865
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_3	0x80010C080301143F	2985
DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_4	0x800110080301143F	3105
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_0	0x8000001D0301143F	1939
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_1	0x8000041D0301143F	2059
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_2	0x8000081D0301143F	2179
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_3	0x80000C1D0301143F	2299
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_4	0x8000101D0301143F	2419
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_0	0x8001001D0301143F	2636
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_1	0x8001041D0301143F	2756
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_2	0x8001081D0301143F	2876
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_3	0x80010C1D0301143F	2996
DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_4	0x8001101D0301143F	3116
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_0	0x8000003703011 43F	1942
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_1	0x8000043703011 43F	2062
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_2	0x8000083703011 43F	2182
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_3	0x80000C3703011 43F	2302
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_4	0x8000103703011 43F	2422
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_0	0x8001003703011 43F	2639
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_1	0x8001043703011 43F	2759

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DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_2	0x800108370301143F	2879
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_3	0x80010C370301143F	2999
DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_4	0x800110370301143F	3119
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_0	0x800000300301143F	1940
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_1	0x800004300301143F	2060
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_2	0x800008300301143F	2180
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_3	0x80000C300301143F	2300
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_4	0x800010300301143F	2420
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_0	0x800100300301143F	2637
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_1	0x800104300301143F	2757
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_2	0x800108300301143F	2877
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_3	0x80010C300301143F	2997
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_4	0x800110300301143F	3117
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_0	0x800001300301143F	1973
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_1	0x800005300301143F	2093
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_2	0x800009300301143F	2213
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_3	0x80000D300301143F	2333
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_4	0x800011300301143F	2453
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_0	0x800101300301143F	2670
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_1	0x800105300301143F	2790
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_2	0x800109300301143F	2910
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_3	0x80010D300301143F	3030
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_4	0x800111300301143F	3150
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_0	0x800002300301143F	1997
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_1	0x800006300301143F	2117
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_2	0x80000A300301143F	2237
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_3	0x80000E300301143F	2357
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_4	0x800012300301143F	2477
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_0	0x800102300301143F	2694
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_1	0x800106300301143F	2814
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_2	0x80010A300301143F	2934
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_3	0x80010E300301143F	3054
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_4	0x800112300301143F	3174
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_0	0x800003300301143F	2022
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_1	0x800007300301143F	2142
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_2	0x80000B300301143F	2262
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_3	0x80000F300301143F	2382
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_4	0x800013300301143F	2502
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_0	0x800103300301143F	2719
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_1	0x800107300301143F	2839
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_2	0x80010B300301143F	2959
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_3	0x80010F300301143F	3079
DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_4	0x800113300301143F	3199
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_0	0x800000310301143F	1940
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_1	0x800004310301143F	2060
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_2	0x800008310301143F	2180
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_3	0x80000C310301143F	2300
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_4	0x800010310301143F	2420
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_0	0x800100310301143F	2637
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_1	0x800104310301143F	2757
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_2	0x800108310301143F	2877

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DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_3	0x80010C310301143F	2997
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_4	0x800110310301143F	3117
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_0	0x800001310301143F	1973
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_1	0x800005310301143F	2093
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_2	0x800009310301143F	2213
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_3	0x80000D310301143F	2333
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_4	0x800011310301143F	2453
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_0	0x800101310301143F	2670
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_1	0x800105310301143F	2790
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_2	0x800109310301143F	2910
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_3	0x80010D310301143F	3030
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_4	0x800111310301143F	3150
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_0	0x800002310301143F	1998
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_1	0x800006310301143F	2118
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_2	0x80000A310301143F	2238
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_3	0x80000E310301143F	2358
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_4	0x800012310301143F	2478
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_0	0x800102310301143F	2695
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_1	0x800106310301143F	2815
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_2	0x80010A310301143F	2935
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_3	0x80010E310301143F	3055
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_4	0x800112310301143F	3175
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_0	0x800003310301143F	2022
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_1	0x800007310301143F	2142
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_2	0x80000B310301143F	2262
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_3	0x80000F310301143F	2382
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_4	0x800013310301143F	2502
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_0	0x800103310301143F	2719
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_1	0x800107310301143F	2839
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_2	0x80010B310301143F	2959
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_3	0x80010F310301143F	3079
DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_4	0x800113310301143F	3199
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_0	0x800000130301143F	1933
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_1	0x800004130301143F	2053
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_2	0x800008130301143F	2173
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_3	0x80000C130301143F	2293
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_4	0x800010130301143F	2413
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_0	0x800100130301143F	2630
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_1	0x800104130301143F	2750
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_2	0x800108130301143F	2870
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_3	0x80010C130301143F	2990
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_4	0x800110130301143F	3110
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_0	0x800001130301143F	1972
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_1	0x800005130301143F	2092
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_2	0x800009130301143F	2212
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_3	0x80000D130301143F	2332
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_4	0x800011130301143F	2452
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_0	0x800101130301143F	2669
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_1	0x800105130301143F	2789
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_2	0x800109130301143F	2909
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_3	0x80010D130301143F	3029

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DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_4	0x8001111130301143F	3149
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_0	0x8000021130301143F	1997
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_1	0x8000061130301143F	2117
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_2	0x80000A1130301143F	2237
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_3	0x80000E1130301143F	2357
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_4	0x8000121130301143F	2477
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_0	0x8001021130301143F	2694
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_1	0x8001061130301143F	2814
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_2	0x80010A1130301143F	2934
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_3	0x80010E1130301143F	3054
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_4	0x8001121130301143F	3174
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_0	0x8000031130301143F	2021
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_1	0x8000071130301143F	2141
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_2	0x80000B1130301143F	2261
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_3	0x80000F1130301143F	2381
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_4	0x8000131130301143F	2501
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_0	0x8001031130301143F	2718
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_1	0x8001071130301143F	2838
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_2	0x80010B1130301143F	2958
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_3	0x80010F1130301143F	3078
DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_4	0x8001131130301143F	3198
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_0	0x8000000090301143F	1929
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_1	0x8000040090301143F	2049
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_2	0x8000080090301143F	2169
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_3	0x80000C090301143F	2289
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_4	0x8000100090301143F	2409
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_0	0x8001000090301143F	2626
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_1	0x8001040090301143F	2746
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_2	0x8001080090301143F	2866
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_3	0x80010C090301143F	2986
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_4	0x8001100090301143F	3106
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_0	0x8000010090301143F	1971
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_1	0x8000050090301143F	2091
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_2	0x8000090090301143F	2211
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_3	0x80000D090301143F	2331
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_4	0x8000110090301143F	2451
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_0	0x8001010090301143F	2668
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_1	0x8001050090301143F	2788
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_2	0x8001090090301143F	2908
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_3	0x80010D090301143F	3028
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_4	0x8001110090301143F	3148
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_0	0x8000020090301143F	1995
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_1	0x8000060090301143F	2115
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_2	0x80000A090301143F	2235
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_3	0x80000E090301143F	2355
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_4	0x8000120090301143F	2475
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_0	0x8001020090301143F	2692
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_1	0x8001060090301143F	2812
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_2	0x80010A090301143F	2932
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_3	0x80010E090301143F	3052
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_4	0x8001120090301143F	3172

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DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_0	0x8000030903011 43F	2020
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_1	0x8000070903011 43F	2140
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_2	0x80000B0903011 43F	2260
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_3	0x80000F0903011 43F	2380
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_4	0x8000130903011 43F	2500
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_0	0x8001030903011 43F	2717
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_1	0x8001070903011 43F	2837
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_2	0x80010B0903011 43F	2957
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_3	0x80010F0903011 43F	3077
DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_4	0x8001130903011 43F	3197
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_0	0x8000007E0301143F	1967
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_1	0x8000047E0301143F	2087
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_2	0x8000087E0301143F	2207
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_3	0x80000C7E0301143F	2327
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_4	0x8000107E0301143F	2447
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_0	0x8001007E0301143F	2664
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_1	0x8001047E0301143F	2784
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_2	0x8001087E0301143F	2904
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_3	0x80010C7E0301143F	3024
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_4	0x8001107E0301143F	3144
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_0	0x8000017E0301143F	1992
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_1	0x8000057E0301143F	2112
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_2	0x8000097E0301143F	2232
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_3	0x80000D7E0301143F	2352
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_4	0x8000117E0301143F	2472
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_0	0x8001017E0301143F	2689
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_1	0x8001057E0301143F	2809
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_2	0x8001097E0301143F	2929
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_3	0x80010D7E0301143F	3049
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_4	0x8001117E0301143F	3169
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_0	0x8000027E0301143F	2016
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_1	0x8000067E0301143F	2136
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_2	0x80000A7E0301143F	2256
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_3	0x80000E7E0301143F	2376
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_4	0x8000127E0301143F	2496
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_0	0x8001027E0301143F	2713
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_1	0x8001067E0301143F	2833
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_2	0x80010A7E0301143F	2953
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_3	0x80010E7E0301143F	3073
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_4	0x8001127E0301143F	3193
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_0	0x8000037E0301143F	2040
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_1	0x8000077E0301143F	2160
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_2	0x80000B7E0301143F	2280
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_3	0x80000F7E0301143F	2400
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_4	0x8000137E0301143F	2520
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_0	0x8001037E0301143F	2737
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_1	0x8001077E0301143F	2857
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_2	0x80010B7E0301143F	2977
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_3	0x80010F7E0301143F	3097
DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_4	0x8001137E0301143F	3217
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_0	0x8000000A0301143F	1930

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DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_1	0x8000040A0301143F	2049
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_2	0x8000080A0301143F	2169
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_3	0x80000C0A0301143F	2289
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_4	0x8000100A0301143F	2409
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_0	0x8001000A0301143F	2626
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_1	0x8001040A0301143F	2746
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_2	0x8001080A0301143F	2866
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_3	0x80010C0A0301143F	2986
DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_4	0x8001100A0301143F	3106
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_0	0x8000005C0301143F	1953
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_1	0x8000045C0301143F	2073
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_2	0x8000085C0301143F	2193
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_3	0x80000C5C0301143F	2313
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_4	0x8000105C0301143F	2433
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_0	0x8001005C0301143F	2650
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_1	0x8001045C0301143F	2770
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_3	0x80010C5C0301143F	3010
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_4	0x8001105C0301143F	3130
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_0	0x8000015C0301143F	1984
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_1	0x8000055C0301143F	2104
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_2	0x8000095C0301143F	2224
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_3	0x80000D5C0301143F	2344
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_4	0x8000115C0301143F	2464
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_0	0x8001015C0301143F	2681
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_1	0x8001055C0301143F	2801
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_2	0x8001095C0301143F	2921
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_3	0x80010D5C0301143F	3041
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_4	0x8001115C0301143F	3161
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_0	0x8000025C0301143F	2009
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_1	0x8000065C0301143F	2129
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_2	0x80000A5C0301143F	2249
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_3	0x80000E5C0301143F	2369
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_4	0x8000125C0301143F	2489
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_0	0x8001025C0301143F	2706
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_0	0x8000035C0301143F	2033
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_0	0x8000005D0301143F	1954
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_1	0x8000045D0301143F	2073

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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_2	0x8000085D0301143F	2193
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_3	0x80000C5D0301143F	2313
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_4	0x8000105D0301143F	2433
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_0	0x8001005D0301143F	2650
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_1	0x8001045D0301143F	2770
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_2	0x8001085D0301143F	2890
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_3	0x80010C5D0301143F	3010
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_1	0x8000055D0301143F	2105
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_2	0x8000095D0301143F	2225
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_1	0x8001055D0301143F	2802
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_2	0x8001095D0301143F	2922
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_3	0x80010D5D0301143F	3042
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_4	0x8001115D0301143F	3162
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_0	0x8000025D0301143F	2009
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_1	0x8000065D0301143F	2129
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_2	0x80000A5D0301143F	2249
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_3	0x80000E5D0301143F	2369
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_4	0x8000125D0301143F	2489
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_0	0x8001025D0301143F	2706
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_3	0x80000F5D0301143F	2393
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DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_1	0x8001075D0301143F	2850
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_2	0x80010B5D0301143F	2970
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_3	0x80010F5D0301143F	3090
DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_4	0x8001135D0301143F	3210
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_0	0x800000750301143F	1962
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_1	0x800004750301143F	2082
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_2	0x800008750301143F	2202
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_3	0x80000C750301143F	2322
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_4	0x800010750301143F	2442
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_0	0x800100750301143F	2659
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_1	0x800104750301143F	2779
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_2	0x800108750301143F	2899
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_3	0x80010C750301143F	3019
DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_4	0x800110750301143F	3139
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_0	0x800000780301143F	1965
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_1	0x800004780301143F	2085
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_2	0x800008780301143F	2205

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DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_3	0x80000C780301143F	2325
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_4	0x800010780301143F	2445
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_0	0x800100780301143F	2662
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_1	0x800104780301143F	2782
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_2	0x800108780301143F	2902
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_3	0x80010C780301143F	3022
DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_4	0x800110780301143F	3142
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_0	0x8000007A0301143F	1966
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_1	0x8000047A0301143F	2086
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_2	0x8000087A0301143F	2206
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_3	0x80000C7A0301143F	2326
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_4	0x8000107A0301143F	2446
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_0	0x8001007A0301143F	2663
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_1	0x8001047A0301143F	2783
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_2	0x8001087A0301143F	2903
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_3	0x80010C7A0301143F	3023
DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_4	0x8001107A0301143F	3143
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_0	0x800000790301143F	1965
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_1	0x800004790301143F	2085
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_2	0x800008790301143F	2205
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_3	0x80000C790301143F	2325
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_4	0x800010790301143F	2445
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_0	0x800100790301143F	2662
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_1	0x800104790301143F	2782
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_2	0x800108790301143F	2902
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_3	0x80010C790301143F	3022
DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_4	0x800110790301143F	3142
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_0	0x8000007B0301143F	1966
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_1	0x8000047B0301143F	2086
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_2	0x8000087B0301143F	2206
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_3	0x80000C7B0301143F	2326
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_4	0x8000107B0301143F	2446
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_0	0x8001007B0301143F	2663
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_1	0x8001047B0301143F	2783
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_2	0x8001087B0301143F	2903
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_3	0x80010C7B0301143F	3023
DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_4	0x8001107B0301143F	3143
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_0	0x800000320301143F	1940
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_1	0x800004320301143F	2060
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_2	0x800008320301143F	2180
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_3	0x80000C320301143F	2300
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_4	0x800010320301143F	2420
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_0	0x800100320301143F	2637
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_1	0x800104320301143F	2757
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_2	0x800108320301143F	2877
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_3	0x80010C320301143F	2997
DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_4	0x800110320301143F	3117
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_0	0x800000330301143F	1941
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_1	0x800004330301143F	2061
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_2	0x800008330301143F	2181
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_3	0x80000C330301143F	2301

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DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_4	0x800010330301143F	2421
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_0	0x800100330301143F	2638
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_1	0x800104330301143F	2758
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_2	0x800108330301143F	2878
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_3	0x80010C330301143F	2998
DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_4	0x800110330301143F	3118
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_0	0x800000340301143F	1942
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_1	0x800004340301143F	2061
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_2	0x800008340301143F	2181
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_3	0x80000C340301143F	2301
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_4	0x800010340301143F	2421
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_0	0x800100340301143F	2638
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_1	0x800104340301143F	2758
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_2	0x800108340301143F	2878
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_3	0x80010C340301143F	2998
DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_4	0x800110340301143F	3118
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_0	0x800000760301143F	1963
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_1	0x800004760301143F	2083
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_2	0x800008760301143F	2203
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_3	0x80000C760301143F	2323
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_4	0x800010760301143F	2443
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_0	0x800100760301143F	2660
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_1	0x800104760301143F	2780
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_2	0x800108760301143F	2900
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_3	0x80010C760301143F	3020
DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_4	0x800110760301143F	3140
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_0	0x800000770301143F	1964
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_1	0x800004770301143F	2084
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_2	0x800008770301143F	2204
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_3	0x80000C770301143F	2324
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_4	0x800010770301143F	2444
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_0	0x800100770301143F	2661
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_1	0x800104770301143F	2781
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_2	0x800108770301143F	2901
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_3	0x80010C770301143F	3021
DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_4	0x800110770301143F	3141
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_0	0x8000006D0301143F	1960
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_1	0x8000046D0301143F	2080
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_2	0x8000086D0301143F	2200
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_3	0x80000C6D0301143F	2320
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_4	0x8000106D0301143F	2440
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_0	0x8001006D0301143F	2657
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_1	0x8001046D0301143F	2777
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_2	0x8001086D0301143F	2897
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_3	0x80010C6D0301143F	3017
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_4	0x8001106D0301143F	3137
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_0	0x800000120301143F	1932
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_1	0x800004120301143F	2052
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_2	0x800008120301143F	2172
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_3	0x80000C120301143F	2292
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_4	0x800010120301143F	2412

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DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_0	0x8001001203011 43F	2629
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_1	0x8001041203011 43F	2749
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_2	0x8001081203011 43F	2869
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_3	0x80010C1203011 43F	2989
DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_4	0x8001101203011 43F	3109
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_0	0x8000001503011 43F	1935
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_1	0x8000041503011 43F	2055
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_2	0x8000081503011 43F	2175
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_3	0x80000C1503011 43F	2295
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_4	0x8000101503011 43F	2415
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_0	0x8001001503011 43F	2632
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_1	0x8001041503011 43F	2752
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_2	0x8001081503011 43F	2872
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_3	0x80010C1503011 43F	2992
DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_4	0x8001101503011 43F	3112
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_0	0x8000000E0301143F	1931
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_1	0x8000040E0301143F	2051
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_2	0x8000080E0301143F	2171
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_3	0x80000C0E0301143F	2291
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_4	0x8000100E0301143F	2411
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_0	0x8001000E0301143F	2628
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_1	0x8001040E0301143F	2748
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_2	0x8001080E0301143F	2868
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_3	0x80010C0E0301143F	2988
DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_4	0x8001100E0301143F	3108
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_0	0x8000000F0301143F	1931
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_1	0x8000040F0301143F	2051
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_2	0x8000080F0301143F	2171
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_3	0x80000C0F0301143F	2291
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_4	0x8000100F0301143F	2411
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_0	0x8001000F0301143F	2628
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_1	0x8001040F0301143F	2748
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_2	0x8001080F0301143F	2868
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_3	0x80010C0F0301143F	2988
DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_4	0x8001100F0301143F	3108
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_0	0x8000001003011 43F	1932
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_1	0x8000041003011 43F	2052
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_2	0x8000081003011 43F	2172
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_3	0x80000C1003011 43F	2292
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_4	0x8000101003011 43F	2412
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_0	0x8001001003011 43F	2628
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_1	0x8001041003011 43F	2749
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_2	0x8001081003011 43F	2869
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_3	0x80010C1003011 43F	2989
DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_4	0x8001101003011 43F	3109
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_0	0x8000001103011 43F	1932
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_1	0x8000041103011 43F	2052
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_2	0x8000081103011 43F	2172
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_3	0x80000C1103011 43F	2292
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_4	0x8000101103011 43F	2412
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_0	0x8001001103011 43F	2629

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DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_1	0x8001041103011 43F	2749
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_2	0x8001081103011 43F	2869
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_3	0x80010C1103011 43F	2989
DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_4	0x8001101103011 43F	3109
DPHY01.DDRPHY_DP18_RD_STATUS0_P0_0	0x8000001403011 43F	1933
DPHY01.DDRPHY_DP18_RD_STATUS0_P0_1	0x8000041403011 43F	2053
DPHY01.DDRPHY_DP18_RD_STATUS0_P0_2	0x8000081403011 43F	2173
DPHY01.DDRPHY_DP18_RD_STATUS0_P0_3	0x80000C1403011 43F	2293
DPHY01.DDRPHY_DP18_RD_STATUS0_P0_4	0x8000101403011 43F	2413
DPHY01.DDRPHY_DP18_RD_STATUS0_P1_0	0x8001001403011 43F	2630
DPHY01.DDRPHY_DP18_RD_STATUS0_P1_1	0x8001041403011 43F	2750
DPHY01.DDRPHY_DP18_RD_STATUS0_P1_2	0x8001081403011 43F	2870
DPHY01.DDRPHY_DP18_RD_STATUS0_P1_3	0x80010C1403011 43F	2990
DPHY01.DDRPHY_DP18_RD_STATUS0_P1_4	0x8001101403011 43F	3110
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_0	0x8000000403011 43F	1924
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_1	0x8000040403011 43F	2044
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_2	0x8000080403011 43F	2164
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_3	0x80000C0403011 43F	2284
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_4	0x8000100403011 43F	2404
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_0	0x8001000403011 43F	2620
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_1	0x8001040403011 43F	2741
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_2	0x8001080403011 43F	2861
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_3	0x80010C0403011 43F	2981
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_4	0x8001100403011 43F	3101
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_0	0x8000010403011 43F	1968
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_1	0x8000050403011 43F	2088
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_2	0x8000090403011 43F	2208
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_3	0x80000D0403011 43F	2328
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_4	0x8000110403011 43F	2448
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_0	0x8001010403011 43F	2665
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_1	0x8001050403011 43F	2785
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_2	0x8001090403011 43F	2905
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_3	0x80010D0403011 43F	3025
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_4	0x8001110403011 43F	3145
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_0	0x8000020403011 43F	1992
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_1	0x8000060403011 43F	2112
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_2	0x80000A0403011 43F	2232
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_3	0x80000E0403011 43F	2352
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_4	0x8000120403011 43F	2472
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_0	0x8001020403011 43F	2689
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_1	0x8001060403011 43F	2809
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_2	0x80010A0403011 43F	2929
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_3	0x80010E0403011 43F	3049
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_4	0x8001120403011 43F	3169
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_0	0x8000030403011 43F	2017
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_1	0x8000070403011 43F	2137
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_2	0x80000B0403011 43F	2257
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_3	0x80000F0403011 43F	2377
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_4	0x8000130403011 43F	2497
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_0	0x8001030403011 43F	2714
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_1	0x8001070403011 43F	2834

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DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_2	0x80010B040301143F	2954
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_3	0x80010F040301143F	3074
DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_4	0x800113040301143F	3194
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_0	0x800000500301143F	1949
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_1	0x800004500301143F	2069
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_2	0x800008500301143F	2189
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_3	0x80000C500301143F	2309
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_4	0x800010500301143F	2429
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_0	0x800100500301143F	2646
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_1	0x800104500301143F	2766
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_2	0x800108500301143F	2886
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_3	0x80010C500301143F	3006
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_4	0x800110500301143F	3126
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_0	0x800001500301143F	1980
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_1	0x800005500301143F	2100
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_2	0x800009500301143F	2220
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_3	0x80000D500301143F	2340
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_4	0x800011500301143F	2460
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_0	0x800101500301143F	2677
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_1	0x800105500301143F	2797
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_2	0x800109500301143F	2917
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_3	0x80010D500301143F	3037
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_4	0x800111500301143F	3157
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_0	0x800002500301143F	2005
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_1	0x800006500301143F	2125
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_2	0x80000A500301143F	2245
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_3	0x80000E500301143F	2365
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_4	0x800012500301143F	2485
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_0	0x800102500301143F	2702
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_1	0x800106500301143F	2822
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_2	0x80010A500301143F	2942
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_3	0x80010E500301143F	3062
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_4	0x800112500301143F	3182
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_0	0x800003500301143F	2029
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_1	0x800007500301143F	2149
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_2	0x80000B500301143F	2269
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_3	0x80000F500301143F	2389
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_4	0x800013500301143F	2509
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_0	0x800103500301143F	2726
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_1	0x800107500301143F	2846
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_2	0x80010B500301143F	2966
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_3	0x80010F500301143F	3086
DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_4	0x800113500301143F	3206
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_0	0x800000510301143F	1950
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_1	0x800004510301143F	2070
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_2	0x800008510301143F	2190
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_3	0x80000C510301143F	2310
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_4	0x800010510301143F	2430
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_0	0x800100510301143F	2647
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_1	0x800104510301143F	2767
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_2	0x800108510301143F	2887

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DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_3	0x80010C510301143F	3007
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_4	0x800110510301143F	3127
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_0	0x800001510301143F	1981
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_1	0x800005510301143F	2101
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_2	0x800009510301143F	2221
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_3	0x80000D510301143F	2341
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_4	0x800011510301143F	2461
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_0	0x800101510301143F	2678
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_1	0x800105510301143F	2798
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_2	0x800109510301143F	2918
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_3	0x80010D510301143F	3038
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_4	0x800111510301143F	3158
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_0	0x800002510301143F	2005
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_1	0x800006510301143F	2125
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_2	0x80000A510301143F	2245
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_3	0x80000E510301143F	2365
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_4	0x800012510301143F	2485
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_0	0x800102510301143F	2702
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_1	0x800106510301143F	2822
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_2	0x80010A510301143F	2942
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_3	0x80010E510301143F	3062
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_4	0x800112510301143F	3182
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_0	0x800003510301143F	2030
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_1	0x800007510301143F	2150
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_2	0x80000B510301143F	2270
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_3	0x80000F510301143F	2390
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_4	0x800013510301143F	2510
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_0	0x800103510301143F	2727
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_1	0x800107510301143F	2847
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_2	0x80010B510301143F	2967
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_3	0x80010F510301143F	3087
DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_4	0x800113510301143F	3207
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_0	0x800000520301143F	1950
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_1	0x800004520301143F	2070
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_2	0x800008520301143F	2190
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_3	0x80000C520301143F	2310
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_4	0x800010520301143F	2430
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_0	0x800100520301143F	2647
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_1	0x800104520301143F	2767
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_2	0x800108520301143F	2887
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_3	0x80010C520301143F	3007
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_4	0x800110520301143F	3127
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_0	0x800001520301143F	1981
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_1	0x800005520301143F	2101
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_2	0x800009520301143F	2221
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_3	0x80000D520301143F	2341
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_4	0x800011520301143F	2461
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_0	0x800101520301143F	2678
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_1	0x800105520301143F	2798
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_2	0x800109520301143F	2918
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_3	0x80010D520301143F	3038

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DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_4	0x800111520301143F	3158
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_0	0x800002520301143F	2006
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_1	0x800006520301143F	2126
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_2	0x80000A520301143F	2246
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_3	0x80000E520301143F	2366
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_4	0x800012520301143F	2486
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_0	0x800102520301143F	2703
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_1	0x800106520301143F	2823
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_2	0x80010A520301143F	2943
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_3	0x80010E520301143F	3063
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_4	0x800112520301143F	3183
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_0	0x800003520301143F	2030
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_1	0x800007520301143F	2150
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_2	0x80000B520301143F	2270
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_3	0x80000F520301143F	2390
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_4	0x800013520301143F	2510
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_0	0x800103520301143F	2727
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_1	0x800107520301143F	2847
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_2	0x80010B520301143F	2967
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_3	0x80010F520301143F	3087
DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_4	0x800113520301143F	3207
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_0	0x800000530301143F	1951
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_1	0x800004530301143F	2071
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_2	0x800008530301143F	2191
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_3	0x80000C530301143F	2311
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_4	0x800010530301143F	2431
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_0	0x800100530301143F	2648
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_1	0x800104530301143F	2768
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_2	0x800108530301143F	2888
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_3	0x80010C530301143F	3008
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_4	0x800110530301143F	3128
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_0	0x800001530301143F	1982
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_1	0x800005530301143F	2102
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_2	0x800009530301143F	2222
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_3	0x80000D530301143F	2342
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_4	0x800011530301143F	2462
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_0	0x800101530301143F	2679
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_1	0x800105530301143F	2799
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_2	0x800109530301143F	2919
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_3	0x80010D530301143F	3039
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_4	0x800111530301143F	3159
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_0	0x800002530301143F	2006
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_1	0x800006530301143F	2126
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_2	0x80000A530301143F	2246
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_3	0x80000E530301143F	2366
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_4	0x800012530301143F	2486
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_0	0x800102530301143F	2703
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_1	0x800106530301143F	2823
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_2	0x80010A530301143F	2943
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_3	0x80010E530301143F	3063
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_4	0x800112530301143F	3183

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DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_0	0x8000035303011 43F	2031
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_1	0x8000075303011 43F	2151
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_2	0x80000B5303011 43F	2271
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_3	0x80000F5303011 43F	2391
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_4	0x8000135303011 43F	2511
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_0	0x8001035303011 43F	2728
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_1	0x8001075303011 43F	2848
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_2	0x80010B5303011 43F	2968
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_3	0x80010F5303011 43F	3088
DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_4	0x8001135303011 43F	3208
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_0	0x8000005403011 43F	1951
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_1	0x8000045403011 43F	2071
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_2	0x8000085403011 43F	2191
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_3	0x80000C5403011 43F	2311
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_4	0x8000105403011 43F	2431
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_0	0x8001005403011 43F	2648
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_1	0x8001045403011 43F	2768
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_2	0x8001085403011 43F	2888
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_3	0x80010C5403011 43F	3008
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_4	0x8001105403011 43F	3128
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_0	0x8000015403011 43F	1982
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_1	0x8000055403011 43F	2102
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_2	0x8000095403011 43F	2222
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_3	0x80000D5403011 43F	2342
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_4	0x8000115403011 43F	2462
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_0	0x8001015403011 43F	2679
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_1	0x8001055403011 43F	2799
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_2	0x8001095403011 43F	2919
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_3	0x80010D5403011 43F	3039
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_4	0x8001115403011 43F	3159
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_0	0x8000025403011 43F	2007
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_1	0x8000065403011 43F	2127
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_2	0x80000A5403011 43F	2247
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_3	0x80000E5403011 43F	2367
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_4	0x8000125403011 43F	2487
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_0	0x8001025403011 43F	2704
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_1	0x8001065403011 43F	2824
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_2	0x80010A5403011 43F	2944
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_3	0x80010E5403011 43F	3064
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_4	0x8001125403011 43F	3184
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_0	0x8000035403011 43F	2031
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_1	0x8000075403011 43F	2151
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_2	0x80000B5403011 43F	2271
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_3	0x80000F5403011 43F	2391
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_4	0x8000135403011 43F	2511
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_0	0x8001035403011 43F	2728
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_1	0x8001075403011 43F	2848
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_2	0x80010B5403011 43F	2968
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_3	0x80010F5403011 43F	3088
DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_4	0x8001135403011 43F	3208
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_0	0x8000005503011 43F	1952

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DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_1	0x8000045503011 43F	2072
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_2	0x8000085503011 43F	2192
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_3	0x80000C5503011 43F	2312
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_4	0x8000105503011 43F	2432
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_0	0x8001005503011 43F	2649
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_1	0x8001045503011 43F	2769
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_2	0x8001085503011 43F	2889
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_3	0x80010C5503011 43F	3009
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_4	0x8001105503011 43F	3129
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_0	0x8000015503011 43F	1983
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_1	0x8000055503011 43F	2103
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_2	0x8000095503011 43F	2223
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_3	0x80000D5503011 43F	2343
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_4	0x8000115503011 43F	2463
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_0	0x8001015503011 43F	2680
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_1	0x8001055503011 43F	2800
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_2	0x8001095503011 43F	2920
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_3	0x80010D5503011 43F	3040
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_4	0x8001115503011 43F	3160
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_0	0x8000025503011 43F	2007
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_1	0x8000065503011 43F	2127
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_2	0x80000A5503011 43F	2247
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_3	0x80000E5503011 43F	2367
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_4	0x8000125503011 43F	2487
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_0	0x8001025503011 43F	2704
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_1	0x8001065503011 43F	2824
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_2	0x80010A5503011 43F	2944
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_3	0x80010E5503011 43F	3064
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_4	0x8001125503011 43F	3184
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_0	0x8000035503011 43F	2032
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_1	0x8000075503011 43F	2152
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_2	0x80000B5503011 43F	2272
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_3	0x80000F5503011 43F	2392
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_4	0x8000135503011 43F	2512
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_0	0x8001035503011 43F	2729
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_1	0x8001075503011 43F	2849
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_2	0x80010B5503011 43F	2969
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_3	0x80010F5503011 43F	3089
DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_4	0x8001135503011 43F	3209
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_0	0x8000005603011 43F	1952
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_1	0x8000045603011 43F	2072
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_2	0x8000085603011 43F	2192
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_3	0x80000C5603011 43F	2312
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_4	0x8000105603011 43F	2432
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_0	0x8001005603011 43F	2649
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_1	0x8001045603011 43F	2769
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_2	0x8001085603011 43F	2889
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_3	0x80010C5603011 43F	3009
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_4	0x8001105603011 43F	3129
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_0	0x8000015603011 43F	1983
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_1	0x8000055603011 43F	2103

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DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_2	0x8000095603011 43F	2223
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_3	0x80000D560301143F	2343
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_4	0x800011560301143F	2463
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_0	0x800101560301143F	2680
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_1	0x800105560301143F	2800
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_2	0x800109560301143F	2920
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_3	0x80010D560301143F	3040
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_4	0x800111560301143F	3160
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_0	0x800002560301143F	2008
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_1	0x800006560301143F	2128
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_2	0x80000A560301143F	2248
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_3	0x80000E560301143F	2368
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_4	0x800012560301143F	2488
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_0	0x800102560301143F	2705
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_1	0x800106560301143F	2825
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_2	0x80010A560301143F	2945
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_3	0x80010E560301143F	3065
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_4	0x800112560301143F	3185
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_0	0x800003560301143F	2032
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_1	0x800007560301143F	2152
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_2	0x80000B560301143F	2272
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_3	0x80000F560301143F	2392
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_4	0x800013560301143F	2512
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_0	0x800103560301143F	2729
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_1	0x800107560301143F	2849
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_2	0x80010B560301143F	2969
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_3	0x80010F560301143F	3089
DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_4	0x800113560301143F	3209
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_0	0x800000570301143F	1953
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_1	0x800004570301143F	2073
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_2	0x800008570301143F	2193
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_3	0x80000C570301143F	2313
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_4	0x800010570301143F	2433
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_0	0x800100570301143F	2650
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_1	0x800104570301143F	2770
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_2	0x800108570301143F	2890
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_3	0x80010C570301143F	3010
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_4	0x800110570301143F	3130
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_0	0x800001570301143F	1984
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_1	0x800005570301143F	2104
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_2	0x800009570301143F	2224
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_3	0x80000D570301143F	2344
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_4	0x800011570301143F	2464
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_0	0x800101570301143F	2681
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_1	0x800105570301143F	2801
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_2	0x800109570301143F	2921
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_3	0x80010D570301143F	3041
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_4	0x800111570301143F	3161
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_0	0x800002570301143F	2008
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_1	0x800006570301143F	2128
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_2	0x80000A570301143F	2248

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DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_3	0x80000E570301143F	2368
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_4	0x800012570301143F	2488
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_0	0x800102570301143F	2705
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_1	0x800106570301143F	2825
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_2	0x80010A570301143F	2945
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_3	0x80010E570301143F	3065
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_4	0x800112570301143F	3185
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_0	0x800003570301143F	2033
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_1	0x800007570301143F	2153
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_2	0x80000B570301143F	2273
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_3	0x80000F570301143F	2393
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_4	0x800013570301143F	2513
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_0	0x800103570301143F	2730
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_1	0x800107570301143F	2850
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_2	0x80010B570301143F	2970
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_3	0x80010F570301143F	3090
DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_4	0x800113570301143F	3210
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_0	0x8000000C0301143F	1930
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_1	0x8000040C0301143F	2050
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_2	0x8000080C0301143F	2170
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_3	0x80000C0C0301143F	2290
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_4	0x8000100C0301143F	2410
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_0	0x8001000C0301143F	2627
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_1	0x8001040C0301143F	2747
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_2	0x8001080C0301143F	2867
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_3	0x80010C0C0301143F	2987
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_4	0x8001100C0301143F	3107
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_0	0x8000010C0301143F	1971
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_1	0x8000050C0301143F	2091
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_2	0x8000090C0301143F	2211
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_3	0x80000D0C0301143F	2331
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_4	0x8000110C0301143F	2451
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_0	0x8001010C0301143F	2668
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_1	0x8001050C0301143F	2788
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_2	0x8001090C0301143F	2908
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_3	0x80010D0C0301143F	3028
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_4	0x8001110C0301143F	3148
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_0	0x8000020C0301143F	1996
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_1	0x8000060C0301143F	2116
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_2	0x80000A0C0301143F	2236
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_3	0x80000E0C0301143F	2356
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_4	0x8000120C0301143F	2476
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_0	0x8001020C0301143F	2693
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_1	0x8001060C0301143F	2813
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_2	0x80010A0C0301143F	2933
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_3	0x80010E0C0301143F	3053
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_4	0x8001120C0301143F	3173
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_0	0x8000030C0301143F	2020
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_1	0x8000070C0301143F	2140
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_2	0x80000B0C0301143F	2260
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_3	0x80000F0C0301143F	2380

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DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_4	0x8000130C0301143F	2500
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_0	0x8001030C0301143F	2717
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_1	0x8001070C0301143F	2837
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_2	0x80010B0C0301143F	2957
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_3	0x80010F0C0301143F	3077
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_4	0x8001130C0301143F	3197
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_0	0x8000000D0301143F	1931
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_1	0x8000040D0301143F	2051
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_2	0x8000080D0301143F	2171
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_3	0x80000C0D0301143F	2291
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_4	0x8000100D0301143F	2411
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_0	0x8001000D0301143F	2627
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_1	0x8001040D0301143F	2748
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_2	0x8001080D0301143F	2868
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_3	0x80010C0D0301143F	2988
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_4	0x8001100D0301143F	3108
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_0	0x8000010D0301143F	1972
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_1	0x8000050D0301143F	2092
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_2	0x8000090D0301143F	2212
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_3	0x80000D0D0301143F	2332
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_4	0x8000110D0301143F	2452
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_0	0x8001010D0301143F	2669
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_1	0x8001050D0301143F	2789
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_2	0x8001090D0301143F	2909
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_3	0x80010D0D0301143F	3029
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_4	0x8001110D0301143F	3149
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_0	0x8000020D0301143F	1996
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_1	0x8000060D0301143F	2116
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_2	0x80000A0D0301143F	2236
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_3	0x80000E0D0301143F	2356
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_4	0x8000120D0301143F	2476
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_0	0x8001020D0301143F	2693
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_1	0x8001060D0301143F	2813
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_2	0x80010A0D0301143F	2933
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_3	0x80010E0D0301143F	3053
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_4	0x8001120D0301143F	3173
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_0	0x8000030D0301143F	2021
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_1	0x8000070D0301143F	2141
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_2	0x80000B0D0301143F	2261
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_3	0x80000F0D0301143F	2381
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_4	0x8000130D0301143F	2501
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_0	0x8001030D0301143F	2718
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_1	0x8001070D0301143F	2838
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_2	0x80010B0D0301143F	2958
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_3	0x80010F0D0301143F	3078
DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_4	0x8001130D0301143F	3198
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_0	0x800000720301143F	1961
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_1	0x800004720301143F	2081
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_2	0x800008720301143F	2201
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_3	0x80000C720301143F	2321
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_4	0x800010720301143F	2441

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DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_0	0x800100720301143F	2658
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_1	0x800104720301143F	2778
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_2	0x800108720301143F	2898
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_3	0x80010C720301143F	3018
DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_4	0x800110720301143F	3138
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_0	0x800000600301143F	1954
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_1	0x800004600301143F	2074
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_2	0x800008600301143F	2194
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_3	0x80000C600301143F	2314
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_4	0x800010600301143F	2434
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_0	0x800100600301143F	2651
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_1	0x800104600301143F	2771
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_2	0x800108600301143F	2891
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_3	0x80010C600301143F	3011
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_4	0x800110600301143F	3131
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_0	0x800001600301143F	1985
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_1	0x800005600301143F	2105
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_2	0x800009600301143F	2225
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_3	0x80000D600301143F	2345
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_4	0x800011600301143F	2465
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_0	0x800101600301143F	2682
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_1	0x800105600301143F	2802
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_2	0x800109600301143F	2922
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_3	0x80010D600301143F	3042
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_4	0x800111600301143F	3162
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_0	0x800002600301143F	2009
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_1	0x800006600301143F	2129
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_2	0x80000A600301143F	2249
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_3	0x80000E600301143F	2369
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_4	0x800012600301143F	2489
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_0	0x800102600301143F	2706
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_1	0x800106600301143F	2826
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_2	0x80010A600301143F	2946
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_3	0x80010E600301143F	3066
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_4	0x800112600301143F	3186
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_0	0x800003600301143F	2034
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_1	0x800007600301143F	2154
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_2	0x80000B600301143F	2274
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_3	0x80000F600301143F	2394
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_4	0x800013600301143F	2514
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_0	0x800103600301143F	2731
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_1	0x800107600301143F	2851
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_2	0x80010B600301143F	2971
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_3	0x80010F600301143F	3091
DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_4	0x800113600301143F	3211
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_0	0x8000006A0301143F	1959
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_1	0x8000046A0301143F	2079
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_2	0x8000086A0301143F	2199
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_3	0x80000C6A0301143F	2319
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_4	0x8000106A0301143F	2439
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_0	0x8001006A0301143F	2656

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_1	0x8001046A0301143F	2776
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_2	0x8001086A0301143F	2896
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_3	0x80010C6A0301143F	3016
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_4	0x8001106A0301143F	3136
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_0	0x8000016A0301143F	1990
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_1	0x8000056A0301143F	2110
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_2	0x8000096A0301143F	2230
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_3	0x80000D6A0301143F	2350
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_4	0x8000116A0301143F	2470
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_0	0x8001016A0301143F	2687
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_1	0x8001056A0301143F	2807
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_2	0x8001096A0301143F	2927
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_3	0x80010D6A0301143F	3047
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_4	0x8001116A0301143F	3167
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_0	0x8000026A0301143F	2014
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_1	0x8000066A0301143F	2134
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_2	0x80000A6A0301143F	2254
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_3	0x80000E6A0301143F	2374
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_4	0x8000126A0301143F	2494
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_0	0x8001026A0301143F	2711
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_1	0x8001066A0301143F	2831
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_2	0x80010A6A0301143F	2951
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_3	0x80010E6A0301143F	3071
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_4	0x8001126A0301143F	3191
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_0	0x8000036A0301143F	2039
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_1	0x8000076A0301143F	2159
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_2	0x80000B6A0301143F	2279
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_3	0x80000F6A0301143F	2399
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_4	0x8000136A0301143F	2519
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_0	0x8001036A0301143F	2736
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_1	0x8001076A0301143F	2856
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_2	0x80010B6A0301143F	2976
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_3	0x80010F6A0301143F	3096
DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_4	0x8001136A0301143F	3216
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_0	0x8000006B0301143F	1959
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_1	0x8000046B0301143F	2079
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_2	0x8000086B0301143F	2199
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_3	0x80000C6B0301143F	2319
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_4	0x8000106B0301143F	2439
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_0	0x8001006B0301143F	2656
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_1	0x8001046B0301143F	2776
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_2	0x8001086B0301143F	2896
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_3	0x80010C6B0301143F	3016
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_4	0x8001106B0301143F	3136
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_0	0x8000016B0301143F	1990
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_1	0x8000056B0301143F	2110
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_2	0x8000096B0301143F	2230
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_3	0x80000D6B0301143F	2350
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_4	0x8000116B0301143F	2470
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_0	0x8001016B0301143F	2687
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_1	0x8001056B0301143F	2807

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_2	0x8001096B0301143F	2927
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_3	0x80010D6B0301143F	3047
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_4	0x8001116B0301143F	3167
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_0	0x8000026B0301143F	2015
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_1	0x8000066B0301143F	2135
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_2	0x80000A6B0301143F	2255
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_3	0x80000E6B0301143F	2375
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_4	0x8000126B0301143F	2495
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_0	0x8001026B0301143F	2712
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_1	0x8001066B0301143F	2832
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_2	0x80010A6B0301143F	2952
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_3	0x80010E6B0301143F	3072
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_4	0x8001126B0301143F	3192
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_0	0x8000036B0301143F	2039
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_1	0x8000076B0301143F	2159
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_2	0x80000B6B0301143F	2279
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_3	0x80000F6B0301143F	2399
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_4	0x8000136B0301143F	2519
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_0	0x8001036B0301143F	2736
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_1	0x8001076B0301143F	2856
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_2	0x80010B6B0301143F	2976
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_3	0x80010F6B0301143F	3096
DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_4	0x8001136B0301143F	3216
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_0	0x8000006103011 43F	1954
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_1	0x8000046103011 43F	2074
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_2	0x8000086103011 43F	2194
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_3	0x80000C6103011 43F	2314
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_4	0x8000106103011 43F	2434
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_0	0x8001006103011 43F	2651
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_1	0x8001046103011 43F	2771
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_2	0x8001086103011 43F	2891
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_3	0x80010C6103011 43F	3011
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_4	0x8001106103011 43F	3131
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_0	0x8000016103011 43F	1985
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_1	0x8000056103011 43F	2105
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_2	0x8000096103011 43F	2225
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_3	0x80000D6103011 43F	2345
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_4	0x8000116103011 43F	2465
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_0	0x8001016103011 43F	2682
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_1	0x8001056103011 43F	2802
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_2	0x8001096103011 43F	2922
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_3	0x80010D6103011 43F	3042
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_4	0x8001116103011 43F	3162
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_0	0x8000026103011 43F	2010
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_1	0x8000066103011 43F	2130
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_2	0x80000A6103011 43F	2250
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_3	0x80000E6103011 43F	2370
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_4	0x8000126103011 43F	2490
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_0	0x8001026103011 43F	2707
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_1	0x8001066103011 43F	2827
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_2	0x80010A6103011 43F	2947

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_3	0x80010E610301143F	3067
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_4	0x800112610301143F	3187
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_0	0x800003610301143F	2034
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_1	0x800007610301143F	2154
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_2	0x80000B610301143F	2274
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_3	0x80000F610301143F	2394
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_4	0x800013610301143F	2514
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_0	0x800103610301143F	2731
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_1	0x800107610301143F	2851
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_2	0x80010B610301143F	2971
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_3	0x80010F610301143F	3091
DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_4	0x800113610301143F	3211
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_0	0x800000620301143F	1955
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_1	0x800004620301143F	2075
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_2	0x800008620301143F	2195
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_3	0x80000C620301143F	2315
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_4	0x800010620301143F	2435
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_0	0x800100620301143F	2652
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_1	0x800104620301143F	2772
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_2	0x800108620301143F	2892
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_3	0x80010C620301143F	3012
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_4	0x800110620301143F	3132
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_0	0x800001620301143F	1986
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_1	0x800005620301143F	2106
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_2	0x800009620301143F	2226
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_3	0x80000D620301143F	2346
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_4	0x800011620301143F	2466
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_0	0x800101620301143F	2683
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_1	0x800105620301143F	2803
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_2	0x800109620301143F	2923
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_3	0x80010D620301143F	3043
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_4	0x800111620301143F	3163
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_0	0x800002620301143F	2010
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_1	0x800006620301143F	2130
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_2	0x80000A620301143F	2250
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_3	0x80000E620301143F	2370
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_4	0x800012620301143F	2490
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_0	0x800102620301143F	2707
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_1	0x800106620301143F	2827
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_2	0x80010A620301143F	2947
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_3	0x80010E620301143F	3067
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_4	0x800112620301143F	3187
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_0	0x800003620301143F	2035
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_1	0x800007620301143F	2155
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_2	0x80000B620301143F	2275
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_3	0x80000F620301143F	2395
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_4	0x800013620301143F	2515
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_0	0x800103620301143F	2732
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_1	0x800107620301143F	2852
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_2	0x80010B620301143F	2972
DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_3	0x80010F620301143F	3092

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_4	0x800113620301143F	3212
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_0	0x800000630301143F	1955
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_1	0x800004630301143F	2075
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_2	0x800008630301143F	2195
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_3	0x80000C630301143F	2315
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_4	0x800010630301143F	2435
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_0	0x800100630301143F	2652
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_1	0x800104630301143F	2772
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_2	0x800108630301143F	2892
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_3	0x80010C630301143F	3012
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_4	0x800110630301143F	3132
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_0	0x800001630301143F	1986
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_1	0x800005630301143F	2106
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_2	0x800009630301143F	2226
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_3	0x80000D630301143F	2346
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_4	0x800011630301143F	2466
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_0	0x800101630301143F	2683
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_1	0x800105630301143F	2803
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_2	0x800109630301143F	2923
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_3	0x80010D630301143F	3043
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_4	0x800111630301143F	3163
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_0	0x800002630301143F	2011
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_1	0x800006630301143F	2131
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_2	0x80000A630301143F	2251
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_3	0x80000E630301143F	2371
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_4	0x800012630301143F	2491
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_0	0x800102630301143F	2708
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_1	0x800106630301143F	2828
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_2	0x80010A630301143F	2948
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_3	0x80010E630301143F	3068
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_4	0x800112630301143F	3188
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_0	0x800003630301143F	2035
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_1	0x800007630301143F	2155
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_2	0x80000B630301143F	2275
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_3	0x80000F630301143F	2395
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_4	0x800013630301143F	2515
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_0	0x800103630301143F	2732
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_1	0x800107630301143F	2852
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_2	0x80010B630301143F	2972
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_3	0x80010F630301143F	3092
DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_4	0x800113630301143F	3212
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_0	0x800000640301143F	1956
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_1	0x800004640301143F	2076
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_2	0x800008640301143F	2196
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_3	0x80000C640301143F	2316
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_4	0x800010640301143F	2436
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_0	0x800100640301143F	2653
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_1	0x800104640301143F	2773
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_2	0x800108640301143F	2893
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_3	0x80010C640301143F	3013
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_4	0x800110640301143F	3133

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_0	0x800001640301143F	1987
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_1	0x800005640301143F	2107
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_2	0x800009640301143F	2227
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_3	0x80000D640301143F	2347
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_4	0x800011640301143F	2467
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_0	0x800101640301143F	2684
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_1	0x800105640301143F	2804
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_2	0x800109640301143F	2924
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_3	0x80010D640301143F	3044
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_4	0x800111640301143F	3164
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_0	0x800002640301143F	2011
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_1	0x800006640301143F	2131
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_2	0x80000A640301143F	2251
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_3	0x80000E640301143F	2371
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_4	0x800012640301143F	2491
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_0	0x800102640301143F	2708
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_1	0x800106640301143F	2828
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_2	0x80010A640301143F	2948
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_3	0x80010E640301143F	3068
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_4	0x800112640301143F	3188
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_0	0x800003640301143F	2036
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_1	0x800007640301143F	2156
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_2	0x80000B640301143F	2276
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_3	0x80000F640301143F	2396
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_4	0x800013640301143F	2516
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_0	0x800103640301143F	2733
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_1	0x800107640301143F	2853
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_2	0x80010B640301143F	2973
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_3	0x80010F640301143F	3093
DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_4	0x800113640301143F	3213
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_0	0x800000650301143F	1956
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_1	0x800004650301143F	2076
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_2	0x800008650301143F	2196
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_3	0x80000C650301143F	2316
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_4	0x800010650301143F	2436
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_0	0x800100650301143F	2653
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_1	0x800104650301143F	2773
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_2	0x800108650301143F	2893
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_3	0x80010C650301143F	3013
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_4	0x800110650301143F	3133
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_0	0x800001650301143F	1987
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_1	0x800005650301143F	2107
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_2	0x800009650301143F	2227
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_3	0x80000D650301143F	2347
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_4	0x800011650301143F	2467
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_0	0x800101650301143F	2684
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_1	0x800105650301143F	2804
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_2	0x800109650301143F	2924
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_3	0x80010D650301143F	3044
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_4	0x800111650301143F	3164
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_0	0x800002650301143F	2012

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_1	0x8000066503011 43F	2132
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_2	0x80000A650301143F	2252
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_3	0x80000E650301143F	2372
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_4	0x8000126503011 43F	2492
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_0	0x8001026503011 43F	2709
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_1	0x8001066503011 43F	2829
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_2	0x80010A650301143F	2949
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_3	0x80010E650301143F	3069
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_4	0x8001126503011 43F	3189
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_0	0x8000036503011 43F	2036
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_1	0x8000076503011 43F	2156
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_2	0x80000B650301143F	2276
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_3	0x80000F650301143F	2396
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_4	0x8000136503011 43F	2516
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_0	0x8001036503011 43F	2733
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_1	0x8001076503011 43F	2853
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_2	0x80010B650301143F	2973
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_3	0x80010F650301143F	3093
DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_4	0x8001136503011 43F	3213
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_0	0x8000006603011 43F	1957
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_1	0x8000046603011 43F	2077
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_2	0x8000086603011 43F	2197
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_3	0x80000C660301143F	2317
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_4	0x8000106603011 43F	2437
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_0	0x8001006603011 43F	2654
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_1	0x8001046603011 43F	2774
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_2	0x8001086603011 43F	2894
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_3	0x80010C660301143F	3014
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_4	0x8001106603011 43F	3134
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_0	0x8000016603011 43F	1988
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_1	0x8000056603011 43F	2108
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_2	0x8000096603011 43F	2228
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_3	0x80000D660301143F	2348
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_4	0x8000116603011 43F	2468
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_0	0x8001016603011 43F	2685
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_1	0x8001056603011 43F	2805
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_2	0x8001096603011 43F	2925
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_3	0x80010D660301143F	3045
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_4	0x8001116603011 43F	3165
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_0	0x8000026603011 43F	2012
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_1	0x8000066603011 43F	2132
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_2	0x80000A660301143F	2252
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_3	0x80000E660301143F	2372
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_4	0x8000126603011 43F	2492
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_0	0x8001026603011 43F	2709
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_1	0x8001066603011 43F	2829
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_2	0x80010A660301143F	2949
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_3	0x80010E660301143F	3069
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_4	0x8001126603011 43F	3189
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_0	0x8000036603011 43F	2037
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_1	0x8000076603011 43F	2157

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_2	0x80000B660301143F	2277
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_3	0x80000F660301143F	2397
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_4	0x800013660301143F	2517
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_0	0x800103660301143F	2734
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_1	0x800107660301143F	2854
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_2	0x80010B660301143F	2974
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_3	0x80010F660301143F	3094
DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_4	0x800113660301143F	3214
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_0	0x800000670301143F	1957
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_1	0x800004670301143F	2077
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_2	0x800008670301143F	2197
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_3	0x80000C670301143F	2317
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_4	0x800010670301143F	2437
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_0	0x800100670301143F	2654
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_1	0x800104670301143F	2774
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_2	0x800108670301143F	2894
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_3	0x80010C670301143F	3014
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_4	0x800110670301143F	3134
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_0	0x800001670301143F	1988
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_1	0x800005670301143F	2108
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_2	0x800009670301143F	2228
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_3	0x80000D670301143F	2348
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_4	0x800011670301143F	2468
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_0	0x800101670301143F	2685
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_1	0x800105670301143F	2805
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_2	0x800109670301143F	2925
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_3	0x80010D670301143F	3045
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_4	0x800111670301143F	3165
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_0	0x800002670301143F	2013
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_1	0x800006670301143F	2133
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_2	0x80000A670301143F	2253
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_3	0x80000E670301143F	2373
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_4	0x800012670301143F	2493
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_0	0x800102670301143F	2710
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_1	0x800106670301143F	2830
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_2	0x80010A670301143F	2950
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_3	0x80010E670301143F	3070
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_4	0x800112670301143F	3190
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_0	0x800003670301143F	2037
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_1	0x800007670301143F	2157
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_2	0x80000B670301143F	2277
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_3	0x80000F670301143F	2397
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_4	0x800013670301143F	2517
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_0	0x800103670301143F	2734
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_1	0x800107670301143F	2854
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_2	0x80010B670301143F	2974
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_3	0x80010F670301143F	3094
DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_4	0x800113670301143F	3214
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_0	0x800000680301143F	1958
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_1	0x800004680301143F	2078
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_2	0x800008680301143F	2198

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_3	0x80000C680301143F	2318
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_4	0x800010680301143F	2438
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_0	0x800100680301143F	2655
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_1	0x800104680301143F	2775
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_2	0x800108680301143F	2895
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_3	0x80010C680301143F	3015
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_4	0x800110680301143F	3135
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_0	0x800001680301143F	1989
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_1	0x800005680301143F	2109
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_2	0x800009680301143F	2229
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_3	0x80000D680301143F	2349
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_4	0x800011680301143F	2469
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_0	0x800101680301143F	2686
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_1	0x800105680301143F	2806
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_2	0x800109680301143F	2926
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_3	0x80010D680301143F	3046
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_4	0x800111680301143F	3166
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_0	0x800002680301143F	2013
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_1	0x800006680301143F	2133
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_2	0x80000A680301143F	2253
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_3	0x80000E680301143F	2373
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_4	0x800012680301143F	2493
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_0	0x800102680301143F	2710
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_1	0x800106680301143F	2830
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_2	0x80010A680301143F	2950
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_3	0x80010E680301143F	3070
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_4	0x800112680301143F	3190
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_0	0x800003680301143F	2038
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_1	0x800007680301143F	2158
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_2	0x80000B680301143F	2278
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_3	0x80000F680301143F	2398
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_4	0x800013680301143F	2518
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_0	0x800103680301143F	2735
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_1	0x800107680301143F	2855
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_2	0x80010B680301143F	2975
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_3	0x80010F680301143F	3095
DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_4	0x800113680301143F	3215
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_0	0x800000690301143F	1958
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_1	0x800004690301143F	2078
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_2	0x800008690301143F	2198
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_3	0x80000C690301143F	2318
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_4	0x800010690301143F	2438
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_0	0x800100690301143F	2655
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_1	0x800104690301143F	2775
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_2	0x800108690301143F	2895
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_3	0x80010C690301143F	3015
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_4	0x800110690301143F	3135
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_0	0x800001690301143F	1989
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_1	0x800005690301143F	2109
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_2	0x800009690301143F	2229
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_3	0x80000D690301143F	2349

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DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_4	0x800011690301143F	2469
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_0	0x800101690301143F	2686
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_1	0x800105690301143F	2806
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_2	0x800109690301143F	2926
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_3	0x80010D690301143F	3046
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_4	0x800111690301143F	3166
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_0	0x800002690301143F	2014
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_1	0x800006690301143F	2134
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_2	0x80000A690301143F	2254
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_3	0x80000E690301143F	2374
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_4	0x800012690301143F	2494
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_0	0x800102690301143F	2711
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_1	0x800106690301143F	2831
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_2	0x80010A690301143F	2951
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_3	0x80010E690301143F	3071
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_4	0x800112690301143F	3191
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_0	0x800003690301143F	2038
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_1	0x800007690301143F	2158
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_2	0x80000B690301143F	2278
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_3	0x80000F690301143F	2398
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_4	0x800013690301143F	2518
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_0	0x800103690301143F	2735
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_1	0x800107690301143F	2855
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_2	0x80010B690301143F	2975
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_3	0x80010F690301143F	3095
DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_4	0x800113690301143F	3215
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_0	0x800000700301143F	1961
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_1	0x800004700301143F	2081
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_2	0x800008700301143F	2201
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_3	0x80000C700301143F	2321
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_4	0x800010700301143F	2441
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_0	0x800100700301143F	2658
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_1	0x800104700301143F	2778
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_2	0x800108700301143F	2898
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_3	0x80010C700301143F	3018
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_4	0x800110700301143F	3138
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_0	0x800000710301143F	1961
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_1	0x800004710301143F	2081
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_2	0x800008710301143F	2201
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_3	0x80000C710301143F	2321
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_4	0x800010710301143F	2441
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_0	0x800100710301143F	2658
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_1	0x800104710301143F	2778
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_2	0x800108710301143F	2898
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_3	0x80010C710301143F	3018
DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_4	0x800110710301143F	3138
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_0	0x800000060301143F	1927
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_1	0x800004060301143F	2047
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_2	0x800008060301143F	2167
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_3	0x80000C060301143F	2287
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_4	0x800010060301143F	2407

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DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_0	0x8001000060301143F	2623
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_1	0x800104060301143F	2744
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_2	0x800108060301143F	2864
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_3	0x80010C060301143F	2984
DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_4	0x800110060301143F	3104
DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_0	0x8000000070301143F	1928
DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_1	0x8000040070301143F	2047
DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_2	0x8000080070301143F	2167
DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_3	0x80000C070301143F	2287
DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_4	0x8000100070301143F	2407
DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_0	0x8001000070301143F	2624
DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_1	0x8001040070301143F	2744
DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_2	0x8001080070301143F	2864
DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_3	0x80010C070301143F	2984
DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_4	0x8001100070301143F	3104
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_0	0x8000000730301143F	1962
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_1	0x8000040730301143F	2082
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_2	0x8000080730301143F	2202
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_3	0x80000C730301143F	2322
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_4	0x8000100730301143F	2442
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_0	0x8001000730301143F	2659
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_1	0x8001040730301143F	2779
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_2	0x8001080730301143F	2899
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_3	0x80010C730301143F	3019
DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_4	0x8001100730301143F	3139
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_0	0x8000000050301143F	1925
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_1	0x8000040050301143F	2045
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_2	0x8000080050301143F	2165
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_3	0x80000C050301143F	2285
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_4	0x8000100050301143F	2405
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_0	0x8001000050301143F	2622
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_1	0x8001040050301143F	2742
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_2	0x8001080050301143F	2862
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_3	0x80010C050301143F	2982
DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_4	0x8001100050301143F	3102
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_0	0x8000001050301143F	1969
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_1	0x8000005050301143F	2089
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_2	0x8000009050301143F	2209
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_3	0x80000D050301143F	2329
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_4	0x8000011050301143F	2449
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_0	0x8001010050301143F	2666
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_1	0x8001050050301143F	2786
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_2	0x8001090050301143F	2906
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_3	0x80010D050301143F	3026
DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_4	0x8001110050301143F	3146
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_0	0x8000002050301143F	1994
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_1	0x8000006050301143F	2114
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_2	0x80000A050301143F	2234
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_3	0x80000E050301143F	2354
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_4	0x8000012050301143F	2474
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_0	0x8001020050301143F	2691

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DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_1	0x8001060503011 43F	2811
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_2	0x80010A050301143F	2931
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_3	0x80010E050301143F	3051
DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_4	0x8001120503011 43F	3171
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_0	0x8000030503011 43F	2018
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_1	0x8000070503011 43F	2138
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_2	0x80000B050301143F	2258
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_3	0x80000F050301143F	2378
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_4	0x8000130503011 43F	2498
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_0	0x8001030503011 43F	2715
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_1	0x8001070503011 43F	2835
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_2	0x80010B050301143F	2955
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_3	0x80010F050301143F	3075
DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_4	0x8001130503011 43F	3195
DPHY01.DDRPHY_DP18_WRCLK_PR_P0_0	0x8000007403011 43F	1962
DPHY01.DDRPHY_DP18_WRCLK_PR_P0_1	0x8000047403011 43F	2082
DPHY01.DDRPHY_DP18_WRCLK_PR_P0_2	0x8000087403011 43F	2202
DPHY01.DDRPHY_DP18_WRCLK_PR_P0_3	0x80000C740301143F	2322
DPHY01.DDRPHY_DP18_WRCLK_PR_P0_4	0x8000107403011 43F	2442
DPHY01.DDRPHY_DP18_WRCLK_PR_P1_0	0x8001007403011 43F	2659
DPHY01.DDRPHY_DP18_WRCLK_PR_P1_1	0x8001047403011 43F	2779
DPHY01.DDRPHY_DP18_WRCLK_PR_P1_2	0x8001087403011 43F	2899
DPHY01.DDRPHY_DP18_WRCLK_PR_P1_3	0x80010C740301143F	3019
DPHY01.DDRPHY_DP18_WRCLK_PR_P1_4	0x8001107403011 43F	3139
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_0	0x8000001803011 43F	1936
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_1	0x8000041803011 43F	2056
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_2	0x8000081803011 43F	2176
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_3	0x80000C180301143F	2296
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_4	0x8000101803011 43F	2416
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_0	0x8001001803011 43F	2633
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_1	0x8001041803011 43F	2753
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_2	0x8001081803011 43F	2873
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_3	0x80010C180301143F	2993
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_4	0x8001101803011 43F	3113
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_0	0x8000001903011 43F	1937
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_1	0x8000041903011 43F	2057
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_2	0x8000081903011 43F	2177
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_3	0x80000C190301143F	2297
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_4	0x8000101903011 43F	2417
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_0	0x8001001903011 43F	2634
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_1	0x8001041903011 43F	2754
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_2	0x8001081903011 43F	2874
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_3	0x80010C190301143F	2994
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_4	0x8001101903011 43F	3114
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_0	0x8000001A03011 43F	1937
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_1	0x8000041A03011 43F	2057
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_2	0x8000081A03011 43F	2177
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_3	0x80000C1A03011 43F	2297
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_4	0x8000101A03011 43F	2417
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_0	0x8001001A03011 43F	2634
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_1	0x8001041A03011 43F	2754

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DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_2	0x8001081A0301143F	2874
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_3	0x80010C1A0301143F	2994
DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_4	0x8001101A0301143F	3114
DPHY01.DDRPHY_DP18_WR_ERROR0_P0_0	0x8000001B0301143F	1938
DPHY01.DDRPHY_DP18_WR_ERROR0_P0_1	0x8000041B0301143F	2057
DPHY01.DDRPHY_DP18_WR_ERROR0_P0_2	0x8000081B0301143F	2177
DPHY01.DDRPHY_DP18_WR_ERROR0_P0_3	0x80000C1B0301143F	2297
DPHY01.DDRPHY_DP18_WR_ERROR0_P0_4	0x8000101B0301143F	2417
DPHY01.DDRPHY_DP18_WR_ERROR0_P1_0	0x8001001B0301143F	2634
DPHY01.DDRPHY_DP18_WR_ERROR0_P1_1	0x8001041B0301143F	2754
DPHY01.DDRPHY_DP18_WR_ERROR0_P1_2	0x8001081B0301143F	2874
DPHY01.DDRPHY_DP18_WR_ERROR0_P1_3	0x80010C1B0301143F	2994
DPHY01.DDRPHY_DP18_WR_ERROR0_P1_4	0x8001101B0301143F	3114
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_0	0x8000001C0301143F	1938
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_1	0x8000041C0301143F	2058
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_2	0x8000081C0301143F	2178
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_3	0x80000C1C0301143F	2298
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_4	0x8000101C0301143F	2418
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_0	0x8001001C0301143F	2635
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_1	0x8001041C0301143F	2755
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_2	0x8001081C0301143F	2875
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_3	0x80010C1C0301143F	2995
DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_4	0x8001101C0301143F	3115
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_0	0x8000001700301143F	1936
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_1	0x8000041700301143F	2055
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_2	0x8000081700301143F	2175
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_3	0x80000C1700301143F	2295
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_4	0x8000101700301143F	2415
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_0	0x8001001700301143F	2632
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_1	0x8001041700301143F	2752
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_2	0x8001081700301143F	2872
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_3	0x80010C1700301143F	2992
DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_4	0x8001101700301143F	3112
DPHY01.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P0	0x8000C0010301143F	2573
DPHY01.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P1	0x8001C0010301143F	3270
DPHY01.DDRPHY_PC_BASE_CNTR0_P0	0x8000C0040301143F	2574
DPHY01.DDRPHY_PC_BASE_CNTR0_P1	0x8001C0040301143F	3271
DPHY01.DDRPHY_PC_BASE_CNTR1_P0	0x8000C0060301143F	2575
DPHY01.DDRPHY_PC_BASE_CNTR1_P1	0x8001C0060301143F	3272
DPHY01.DDRPHY_PC_CAL_TIMER_P0	0x8000C0070301143F	2575
DPHY01.DDRPHY_PC_CAL_TIMER_P1	0x8001C0070301143F	3272
DPHY01.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0	0x8000C0080301143F	2575
DPHY01.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1	0x8001C0080301143F	3272
DPHY01.DDRPHY_PC_CONFIG0_P0	0x8000C00C0301143F	2577
DPHY01.DDRPHY_PC_CONFIG0_P1	0x8001C00C0301143F	3274
DPHY01.DDRPHY_PC_CONFIG1_P0	0x8000C00D0301143F	2578
DPHY01.DDRPHY_PC_CONFIG1_P1	0x8001C00D0301143F	3275
DPHY01.DDRPHY_PC_CSID_CFG_P0	0x8000C0330301143F	2590
DPHY01.DDRPHY_PC_CSID_CFG_P1	0x8001C0330301143F	3287
DPHY01.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P0	0x8000C0000301143F	2572
DPHY01.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P1	0x8001C0000301143F	3269

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DPHY01.DDRPHY_PC_ERROR_MASK0_P0	0x8000C0130301143F	2582
DPHY01.DDRPHY_PC_ERROR_MASK0_P1	0x8001C0130301143F	3279
DPHY01.DDRPHY_PC_ERROR_STATUS0_P0	0x8000C0120301143F	2581
DPHY01.DDRPHY_PC_ERROR_STATUS0_P1	0x8001C0120301143F	3278
DPHY01.DDRPHY_PC_INIT_CAL_CONFIG0_P0	0x8000C0160301143F	2583
DPHY01.DDRPHY_PC_INIT_CAL_CONFIG0_P1	0x8001C0160301143F	3280
DPHY01.DDRPHY_PC_INIT_CAL_CONFIG1_P0	0x8000C0170301143F	2584
DPHY01.DDRPHY_PC_INIT_CAL_CONFIG1_P1	0x8001C0170301143F	3281
DPHY01.DDRPHY_PC_INIT_CAL_ERROR_P0	0x8000C0180301143F	2585
DPHY01.DDRPHY_PC_INIT_CAL_ERROR_P1	0x8001C0180301143F	3282
DPHY01.DDRPHY_PC_INIT_CAL_MASK_P0	0x8000C01A0301143F	2586
DPHY01.DDRPHY_PC_INIT_CAL_MASK_P1	0x8001C01A0301143F	3283
DPHY01.DDRPHY_PC_INIT_CAL_STATUS_P0	0x8000C0190301143F	2586
DPHY01.DDRPHY_PC_INIT_CAL_STATUS_P1	0x8001C0190301143F	3283
DPHY01.DDRPHY_PC_IO_PVT_FET_CONTROL_P0	0x8000C0140301143F	2582
DPHY01.DDRPHY_PC_IO_PVT_FET_CONTROL_P1	0x8001C0140301143F	3279
DPHY01.DDRPHY_PC_IO_PVT_FET_STATUS_P0	0x8000C01B0301143F	2587
DPHY01.DDRPHY_PC_IO_PVT_FET_STATUS_P1	0x8001C01B0301143F	3284
DPHY01.DDRPHY_PC_MR0_PRI_RP0_P0	0x8000C01C0301143F	2587
DPHY01.DDRPHY_PC_MR0_PRI_RP0_P1	0x8001C01C0301143F	3284
DPHY01.DDRPHY_PC_MR0_PRI_RP1_P0	0x8000C11C0301143F	2591
DPHY01.DDRPHY_PC_MR0_PRI_RP1_P1	0x8001C11C0301143F	3288
DPHY01.DDRPHY_PC_MR0_PRI_RP2_P0	0x8000C21C0301143F	2594
DPHY01.DDRPHY_PC_MR0_PRI_RP2_P1	0x8001C21C0301143F	3291
DPHY01.DDRPHY_PC_MR0_PRI_RP3_P0	0x8000C31C0301143F	2596
DPHY01.DDRPHY_PC_MR0_PRI_RP3_P1	0x8001C31C0301143F	3293
DPHY01.DDRPHY_PC_MR0_SEC_RP0_P0	0x8000C0200301143F	2588
DPHY01.DDRPHY_PC_MR0_SEC_RP0_P1	0x8001C0200301143F	3285
DPHY01.DDRPHY_PC_MR0_SEC_RP1_P0	0x8000C1200301143F	2592
DPHY01.DDRPHY_PC_MR0_SEC_RP1_P1	0x8001C1200301143F	3289
DPHY01.DDRPHY_PC_MR0_SEC_RP2_P0	0x8000C2200301143F	2595
DPHY01.DDRPHY_PC_MR0_SEC_RP2_P1	0x8001C2200301143F	3292
DPHY01.DDRPHY_PC_MR0_SEC_RP3_P0	0x8000C3200301143F	2597
DPHY01.DDRPHY_PC_MR0_SEC_RP3_P1	0x8001C3200301143F	3294
DPHY01.DDRPHY_PC_MR1_PRI_RP0_P0	0x8000C01D0301143F	2587
DPHY01.DDRPHY_PC_MR1_PRI_RP0_P1	0x8001C01D0301143F	3284
DPHY01.DDRPHY_PC_MR1_PRI_RP1_P0	0x8000C11D0301143F	2592
DPHY01.DDRPHY_PC_MR1_PRI_RP1_P1	0x8001C11D0301143F	3289
DPHY01.DDRPHY_PC_MR1_PRI_RP2_P0	0x8000C21D0301143F	2594
DPHY01.DDRPHY_PC_MR1_PRI_RP2_P1	0x8001C21D0301143F	3291
DPHY01.DDRPHY_PC_MR1_PRI_RP3_P0	0x8000C31D0301143F	2596
DPHY01.DDRPHY_PC_MR1_PRI_RP3_P1	0x8001C31D0301143F	3293
DPHY01.DDRPHY_PC_MR1_SEC_RP0_P0	0x8000C0210301143F	2588
DPHY01.DDRPHY_PC_MR1_SEC_RP0_P1	0x8001C0210301143F	3285
DPHY01.DDRPHY_PC_MR1_SEC_RP1_P0	0x8000C1210301143F	2593
DPHY01.DDRPHY_PC_MR1_SEC_RP1_P1	0x8001C1210301143F	3290
DPHY01.DDRPHY_PC_MR1_SEC_RP2_P0	0x8000C2210301143F	2595
DPHY01.DDRPHY_PC_MR1_SEC_RP2_P1	0x8001C2210301143F	3292
DPHY01.DDRPHY_PC_MR1_SEC_RP3_P0	0x8000C3210301143F	2598
DPHY01.DDRPHY_PC_MR1_SEC_RP3_P1	0x8001C3210301143F	3295
DPHY01.DDRPHY_PC_MR2_PRI_RP0_P0	0x8000C01E0301143F	2587

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DPHY01.DDRPHY_PC_MR2_PRI_RP0_P1	0x8001C01E0301143F	3284
DPHY01.DDRPHY_PC_MR2_PRI_RP1_P0	0x8000C11E0301143F	2592
DPHY01.DDRPHY_PC_MR2_PRI_RP1_P1	0x8001C11E0301143F	3289
DPHY01.DDRPHY_PC_MR2_PRI_RP2_P0	0x8000C21E0301143F	2594
DPHY01.DDRPHY_PC_MR2_PRI_RP2_P1	0x8001C21E0301143F	3291
DPHY01.DDRPHY_PC_MR2_PRI_RP3_P0	0x8000C31E0301143F	2597
DPHY01.DDRPHY_PC_MR2_PRI_RP3_P1	0x8001C31E0301143F	3294
DPHY01.DDRPHY_PC_MR2_SEC_RP0_P0	0x8000C0220301143F	2589
DPHY01.DDRPHY_PC_MR2_SEC_RP0_P1	0x8001C0220301143F	3286
DPHY01.DDRPHY_PC_MR2_SEC_RP1_P0	0x8000C1220301143F	2593
DPHY01.DDRPHY_PC_MR2_SEC_RP1_P1	0x8001C1220301143F	3290
DPHY01.DDRPHY_PC_MR2_SEC_RP2_P0	0x8000C2220301143F	2596
DPHY01.DDRPHY_PC_MR2_SEC_RP2_P1	0x8001C2220301143F	3293
DPHY01.DDRPHY_PC_MR2_SEC_RP3_P0	0x8000C3220301143F	2598
DPHY01.DDRPHY_PC_MR2_SEC_RP3_P1	0x8001C3220301143F	3295
DPHY01.DDRPHY_PC_MR3_PRI_RP0_P0	0x8000C01F0301143F	2588
DPHY01.DDRPHY_PC_MR3_PRI_RP0_P1	0x8001C01F0301143F	3285
DPHY01.DDRPHY_PC_MR3_PRI_RP1_P0	0x8000C11F0301143F	2592
DPHY01.DDRPHY_PC_MR3_PRI_RP1_P1	0x8001C11F0301143F	3289
DPHY01.DDRPHY_PC_MR3_PRI_RP2_P0	0x8000C21F0301143F	2595
DPHY01.DDRPHY_PC_MR3_PRI_RP2_P1	0x8001C21F0301143F	3292
DPHY01.DDRPHY_PC_MR3_PRI_RP3_P0	0x8000C31F0301143F	2597
DPHY01.DDRPHY_PC_MR3_PRI_RP3_P1	0x8001C31F0301143F	3294
DPHY01.DDRPHY_PC_MR3_SEC_RP0_P0	0x8000C0230301143F	2589
DPHY01.DDRPHY_PC_MR3_SEC_RP0_P1	0x8001C0230301143F	3286
DPHY01.DDRPHY_PC_MR3_SEC_RP1_P0	0x8000C1230301143F	2593
DPHY01.DDRPHY_PC_MR3_SEC_RP1_P1	0x8001C1230301143F	3290
DPHY01.DDRPHY_PC_MR3_SEC_RP2_P0	0x8000C2230301143F	2596
DPHY01.DDRPHY_PC_MR3_SEC_RP2_P1	0x8001C2230301143F	3293
DPHY01.DDRPHY_PC_MR3_SEC_RP3_P0	0x8000C3230301143F	2598
DPHY01.DDRPHY_PC_MR3_SEC_RP3_P1	0x8001C3230301143F	3295
DPHY01.DDRPHY_PC_PER_CAL_CONFIG_P0	0x8000C00B0301143F	2576
DPHY01.DDRPHY_PC_PER_CAL_CONFIG_P1	0x8001C00B0301143F	3273
DPHY01.DDRPHY_PC_PER_ZCAL_CONFIG_P0	0x8000C00F0301143F	2579
DPHY01.DDRPHY_PC_PER_ZCAL_CONFIG_P1	0x8001C00F0301143F	3276
DPHY01.DDRPHY_PC_POWERDOWN_1_P0	0x8000C0100301143F	2580
DPHY01.DDRPHY_PC_POWERDOWN_1_P1	0x8001C0100301143F	3277
DPHY01.DDRPHY_PC_RANK_GROUP_EXT_P0	0x8000C0350301143F	2591
DPHY01.DDRPHY_PC_RANK_GROUP_EXT_P1	0x8001C0350301143F	3288
DPHY01.DDRPHY_PC_RANK_GROUP_P0	0x8000C0110301143F	2581
DPHY01.DDRPHY_PC_RANK_GROUP_P1	0x8001C0110301143F	3278
DPHY01.DDRPHY_PC_RANK_PAIR0_P0	0x8000C0020301143F	2573
DPHY01.DDRPHY_PC_RANK_PAIR0_P1	0x8001C0020301143F	3270
DPHY01.DDRPHY_PC_RANK_PAIR1_P0	0x8000C0030301143F	2573
DPHY01.DDRPHY_PC_RANK_PAIR1_P1	0x8001C0030301143F	3270
DPHY01.DDRPHY_PC_RANK_PAIR2_P0	0x8000C0300301143F	2589
DPHY01.DDRPHY_PC_RANK_PAIR2_P1	0x8001C0300301143F	3286
DPHY01.DDRPHY_PC_RANK_PAIR3_P0	0x8000C0310301143F	2590
DPHY01.DDRPHY_PC_RANK_PAIR3_P1	0x8001C0310301143F	3287
DPHY01.DDRPHY_PC_RELOAD_VALUE0_P0	0x8000C0050301143F	2574
DPHY01.DDRPHY_PC_RELOAD_VALUE0_P1	0x8001C0050301143F	3271

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DPHY01.DDRPHY_PC_RESETS_P0	0x8000C00E0301143F	2579
DPHY01.DDRPHY_PC_RESETS_P1	0x8001C00E0301143F	3276
DPHY01.DDRPHY_PC_VREF_DRV_CONTROL_P0	0x8000C0150301143F	2583
DPHY01.DDRPHY_PC_VREF_DRV_CONTROL_P1	0x8001C0150301143F	3280
DPHY01.DDRPHY_PC_ZCAL_TIMER_P0	0x8000C0090301143F	2576
DPHY01.DDRPHY_PC_ZCAL_TIMER_P1	0x8001C0090301143F	3273
DPHY01.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0	0x8000C00A0301143F	2576
DPHY01.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1	0x8001C00A0301143F	3273
DPHY01.DDRPHY_RC_CONFIG0_P0	0x8000C8000301143F	2610
DPHY01.DDRPHY_RC_CONFIG0_P1	0x8001C8000301143F	3307
DPHY01.DDRPHY_RC_CONFIG1_P0	0x8000C8010301143F	2611
DPHY01.DDRPHY_RC_CONFIG1_P1	0x8001C8010301143F	3308
DPHY01.DDRPHY_RC_CONFIG2_P0	0x8000C8020301143F	2611
DPHY01.DDRPHY_RC_CONFIG2_P1	0x8001C8020301143F	3308
DPHY01.DDRPHY_RC_CONFIG3_P0	0x8000C8070301143F	2612
DPHY01.DDRPHY_RC_CONFIG3_P1	0x8001C8070301143F	3309
DPHY01.DDRPHY_RC_ERROR_MASK0_P0	0x8000C8060301143F	2612
DPHY01.DDRPHY_RC_ERROR_MASK0_P1	0x8001C8060301143F	3309
DPHY01.DDRPHY_RC_ERROR_STATUS0_P0	0x8000C8050301143F	2612
DPHY01.DDRPHY_RC_ERROR_STATUS0_P1	0x8001C8050301143F	3309
DPHY01.DDRPHY_SEQ_CONFIG0_P0	0x8000C4020301143F	2600
DPHY01.DDRPHY_SEQ_CONFIG0_P1	0x8001C4020301143F	3297
DPHY01.DDRPHY_SEQ_ERROR_MASK0_P0	0x8000C4090301143F	2603
DPHY01.DDRPHY_SEQ_ERROR_MASK0_P1	0x8001C4090301143F	3300
DPHY01.DDRPHY_SEQ_ERROR_STATUS0_P0	0x8000C4080301143F	2602
DPHY01.DDRPHY_SEQ_ERROR_STATUS0_P1	0x8001C4080301143F	3299
DPHY01.DDRPHY_SEQ_LPT_ADDR2_P0	0x8000C4170301143F	2607
DPHY01.DDRPHY_SEQ_LPT_ADDR2_P1	0x8001C4170301143F	3304
DPHY01.DDRPHY_SEQ_LPT_ADDR3_P0	0x8000C4180301143F	2607
DPHY01.DDRPHY_SEQ_LPT_ADDR3_P1	0x8001C4180301143F	3304
DPHY01.DDRPHY_SEQ_LPT_ADDR4_P0	0x8000C4190301143F	2608
DPHY01.DDRPHY_SEQ_LPT_ADDR4_P1	0x8001C4190301143F	3305
DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM0_P0	0x8000C4120301143F	2606
DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM0_P1	0x8001C4120301143F	3303
DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM1_P0	0x8000C4130301143F	2606
DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM1_P1	0x8001C4130301143F	3303
DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM2_P0	0x8000C4140301143F	2606
DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM2_P1	0x8001C4140301143F	3303
DPHY01.DDRPHY_SEQ_ODT_DEFAULT_CFG_P0	0x8000C4240301143F	2609
DPHY01.DDRPHY_SEQ_ODT_DEFAULT_CFG_P1	0x8001C4240301143F	3306
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG0_P0	0x8000C40E0301143F	2604
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG0_P1	0x8001C40E0301143F	3301
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG1_P0	0x8000C40F0301143F	2605
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG1_P1	0x8001C40F0301143F	3302
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG2_P0	0x8000C4100301143F	2605
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG2_P1	0x8001C4100301143F	3302
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG3_P0	0x8000C4110301143F	2605
DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG3_P1	0x8001C4110301143F	3302
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG0_P0	0x8000C40A0301143F	2603
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG0_P1	0x8001C40A0301143F	3300
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG1_P0	0x8000C40B0301143F	2603

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DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG1_P1	0x8001C40B0301143F	3300
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG2_P0	0x8000C40C0301143F	2604
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG2_P1	0x8001C40C0301143F	3301
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG3_P0	0x8000C40D0301143F	2604
DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG3_P1	0x8001C40D0301143F	3301
DPHY01.DDRPHY_SEQ_RD_WR_DATA0_P0	0x8000C4000301143F	2599
DPHY01.DDRPHY_SEQ_RD_WR_DATA0_P1	0x8001C4000301143F	3296
DPHY01.DDRPHY_SEQ_RD_WR_DATA1_P0	0x8000C4010301143F	2599
DPHY01.DDRPHY_SEQ_RD_WR_DATA1_P1	0x8001C4010301143F	3296
DPHY01.DDRPHY_SEQ_RESERVED_ADDR0_P0	0x8000C4030301143F	2600
DPHY01.DDRPHY_SEQ_RESERVED_ADDR0_P1	0x8001C4030301143F	3297
DPHY01.DDRPHY_SEQ_RESERVED_ADDR1_P0	0x8000C4040301143F	2601
DPHY01.DDRPHY_SEQ_RESERVED_ADDR1_P1	0x8001C4040301143F	3298
DPHY01.DDRPHY_SEQ_RESERVED_ADDR2_P0	0x8000C4050301143F	2601
DPHY01.DDRPHY_SEQ_RESERVED_ADDR2_P1	0x8001C4050301143F	3298
DPHY01.DDRPHY_SEQ_RESERVED_ADDR3_P0	0x8000C4060301143F	2601
DPHY01.DDRPHY_SEQ_RESERVED_ADDR3_P1	0x8001C4060301143F	3298
DPHY01.DDRPHY_SEQ_RESERVED_ADDR4_P0	0x8000C4070301143F	2602
DPHY01.DDRPHY_SEQ_RESERVED_ADDR4_P1	0x8001C4070301143F	3299
DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0	0x8000C41A0301143F	2608
DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1	0x8001C41A0301143F	3305
DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0	0x8000C41B0301143F	2609
DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1	0x8001C41B0301143F	3306
DPHY01.DDRPHY_WC_CONFIG0_P0	0x8000CC000301143F	2613
DPHY01.DDRPHY_WC_CONFIG0_P1	0x8001CC000301143F	3310
DPHY01.DDRPHY_WC_CONFIG1_P0	0x8000CC010301143F	2613
DPHY01.DDRPHY_WC_CONFIG1_P1	0x8001CC010301143F	3310
DPHY01.DDRPHY_WC_CONFIG2_P0	0x8000CC020301143F	2614
DPHY01.DDRPHY_WC_CONFIG2_P1	0x8001CC020301143F	3311
DPHY01.DDRPHY_WC_CONFIG3_P0	0x8000CC050301143F	2615
DPHY01.DDRPHY_WC_CONFIG3_P1	0x8001CC050301143F	3312
DPHY01.DDRPHY_WC_ERROR_MASK0_P0	0x8000CC040301143F	2614
DPHY01.DDRPHY_WC_ERROR_MASK0_P1	0x8001CC040301143F	3311
DPHY01.DDRPHY_WC_ERROR_STATUS0_P0	0x8000CC030301143F	2614
DPHY01.DDRPHY_WC_ERROR_STATUS0_P1	0x8001CC030301143F	3311
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_0	0x800000380301143F	1943
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_1	0x800004380301143F	2062
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_2	0x800008380301143F	2182
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_3	0x80000C380301143F	2302
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_4	0x800010380301143F	2422
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_0	0x800100380301143F	2639
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_1	0x800104380301143F	2759
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_2	0x800108380301143F	2879
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_3	0x80010C380301143F	2999
DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_4	0x800110380301143F	3119
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_0	0x800001380301143F	1974
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_1	0x800005380301143F	2094
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_2	0x800009380301143F	2214
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_3	0x80000D380301143F	2334
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_4	0x800011380301143F	2454
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_0	0x800101380301143F	2671

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DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_1	0x8001053803011 43F	2791
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_2	0x8001093803011 43F	2911
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_3	0x80010D3803011 43F	3031
DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_4	0x8001113803011 43F	3151
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_0	0x8000023803011 43F	1998
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_1	0x8000063803011 43F	2118
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_2	0x80000A3803011 43F	2238
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_3	0x80000E3803011 43F	2358
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_4	0x8000123803011 43F	2478
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_0	0x8001023803011 43F	2695
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_1	0x8001063803011 43F	2815
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_2	0x80010A3803011 43F	2935
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_3	0x80010E3803011 43F	3055
DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_4	0x8001123803011 43F	3175
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_0	0x8000033803011 43F	2022
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_1	0x8000073803011 43F	2142
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_2	0x80000B3803011 43F	2262
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_3	0x80000F3803011 43F	2382
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_4	0x8000133803011 43F	2502
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_0	0x8001033803011 43F	2719
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_1	0x8001073803011 43F	2839
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_2	0x80010B3803011 43F	2959
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_3	0x80010F3803011 43F	3079
DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_4	0x8001133803011 43F	3199
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_0	0x8000042030114 3F	1946
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_1	0x8000442030114 3F	2066
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_2	0x8000842030114 3F	2186
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_3	0x80000C4203011 43F	2306
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_4	0x8000104203011 43F	2426
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_0	0x8001004203011 43F	2643
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_1	0x8001044203011 43F	2763
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_2	0x8001084203011 43F	2883
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_3	0x80010C4203011 43F	3003
DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_4	0x8001104203011 43F	3123
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_0	0x8000014203011 43F	1977
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_1	0x8000054203011 43F	2097
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_2	0x8000094203011 43F	2217
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_3	0x80000D4203011 43F	2337
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_4	0x8000114203011 43F	2457
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_0	0x8001014203011 43F	2674
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_1	0x8001054203011 43F	2794
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_2	0x8001094203011 43F	2914
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_3	0x80010D4203011 43F	3034
DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_4	0x8001114203011 43F	3154
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_0	0x8000024203011 43F	2001
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_1	0x8000064203011 43F	2121
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_2	0x80000A4203011 43F	2241
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_3	0x80000E4203011 43F	2361
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_4	0x8000124203011 43F	2481
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_0	0x8001024203011 43F	2698
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_1	0x8001064203011 43F	2818

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DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_2	0x80010A420301143F	2938
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_3	0x80010E420301143F	3058
DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_4	0x800112420301143F	3178
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_0	0x800003420301143F	2026
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_1	0x800007420301143F	2146
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_2	0x80000B420301143F	2266
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_3	0x80000F420301143F	2386
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_4	0x800013420301143F	2506
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_0	0x800103420301143F	2723
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_1	0x800107420301143F	2843
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_2	0x80010B420301143F	2963
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_3	0x80010F420301143F	3083
DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_4	0x800113420301143F	3203
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_0	0x800000430301143F	1946
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_1	0x800004430301143F	2066
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_2	0x800008430301143F	2186
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_3	0x80000C430301143F	2306
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_4	0x800010430301143F	2426
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_0	0x800100430301143F	2643
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_1	0x800104430301143F	2763
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_2	0x800108430301143F	2883
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_3	0x80010C430301143F	3003
DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_4	0x800110430301143F	3123
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_0	0x800001430301143F	1977
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_1	0x800005430301143F	2097
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_2	0x800009430301143F	2217
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_3	0x80000D430301143F	2337
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_4	0x800011430301143F	2457
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_0	0x800101430301143F	2674
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_1	0x800105430301143F	2794
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_2	0x800109430301143F	2914
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_3	0x80010D430301143F	3034
DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_4	0x800111430301143F	3154
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_0	0x800002430301143F	2002
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_1	0x800006430301143F	2122
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_2	0x80000A430301143F	2242
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_3	0x80000E430301143F	2362
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_4	0x800012430301143F	2482
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_0	0x800102430301143F	2699
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_1	0x800106430301143F	2819
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_2	0x80010A430301143F	2939
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_3	0x80010E430301143F	3059
DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_4	0x800112430301143F	3179
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_0	0x800003430301143F	2026
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_1	0x800007430301143F	2146
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_2	0x80000B430301143F	2266
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_3	0x80000F430301143F	2386
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_4	0x800013430301143F	2506
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_0	0x800103430301143F	2723
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_1	0x800107430301143F	2843
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_2	0x80010B430301143F	2963

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DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_3	0x80010F430301143F	3083
DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_4	0x800113430301143F	3203
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_0	0x800000440301143F	1947
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_1	0x800004440301143F	2066
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_2	0x800008440301143F	2186
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_3	0x80000C440301143F	2306
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_4	0x800010440301143F	2426
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_0	0x800100440301143F	2643
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_1	0x800104440301143F	2763
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_2	0x800108440301143F	2883
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_3	0x80010C440301143F	3003
DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_4	0x800110440301143F	3123
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_0	0x800001440301143F	1978
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_1	0x800005440301143F	2098
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_2	0x800009440301143F	2218
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_3	0x80000D440301143F	2338
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_4	0x800011440301143F	2458
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_0	0x800101440301143F	2675
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_1	0x800105440301143F	2795
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_2	0x800109440301143F	2915
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_3	0x80010D440301143F	3035
DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_4	0x800111440301143F	3155
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_0	0x800002440301143F	2002
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_1	0x800006440301143F	2122
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_2	0x80000A440301143F	2242
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_3	0x80000E440301143F	2362
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_4	0x800012440301143F	2482
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_0	0x800102440301143F	2699
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_1	0x800106440301143F	2819
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_2	0x80010A440301143F	2939
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_3	0x80010E440301143F	3059
DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_4	0x800112440301143F	3179
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_0	0x800003440301143F	2026
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_1	0x800007440301143F	2146
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_2	0x80000B440301143F	2266
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_3	0x80000F440301143F	2386
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_4	0x800013440301143F	2506
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_0	0x800103440301143F	2723
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_1	0x800107440301143F	2843
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_2	0x80010B440301143F	2963
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_3	0x80010F440301143F	3083
DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_4	0x800113440301143F	3203
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_0	0x800000450301143F	1947
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_1	0x800004450301143F	2067
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_2	0x800008450301143F	2187
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_3	0x80000C450301143F	2307
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_4	0x800010450301143F	2427
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_0	0x800100450301143F	2644
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_1	0x800104450301143F	2764
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_2	0x800108450301143F	2884
DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_3	0x80010C450301143F	3004

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DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_4	0x800110450301143F	3124
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_0	0x800001450301143F	1978
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_1	0x800005450301143F	2098
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_2	0x800009450301143F	2218
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_3	0x80000D450301143F	2338
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_4	0x800011450301143F	2458
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_0	0x800101450301143F	2675
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_1	0x800105450301143F	2795
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_2	0x800109450301143F	2915
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_3	0x80010D450301143F	3035
DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_4	0x800111450301143F	3155
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_0	0x800002450301143F	2002
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_1	0x800006450301143F	2122
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_2	0x80000A450301143F	2242
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_3	0x80000E450301143F	2362
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_4	0x800012450301143F	2482
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_0	0x800102450301143F	2699
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_1	0x800106450301143F	2819
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_2	0x80010A450301143F	2939
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_3	0x80010E450301143F	3059
DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_4	0x800112450301143F	3179
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_0	0x800003450301143F	2027
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_1	0x800007450301143F	2147
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_2	0x80000B450301143F	2267
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_3	0x80000F450301143F	2387
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_4	0x800013450301143F	2507
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_0	0x800103450301143F	2724
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_1	0x800107450301143F	2844
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_2	0x80010B450301143F	2964
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_3	0x80010F450301143F	3084
DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_4	0x800113450301143F	3204
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_0	0x800000460301143F	1947
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_1	0x800004460301143F	2067
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_2	0x800008460301143F	2187
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_3	0x80000C460301143F	2307
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_4	0x800010460301143F	2427
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_0	0x800100460301143F	2644
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_1	0x800104460301143F	2764
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_2	0x800108460301143F	2884
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_3	0x80010C460301143F	3004
DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_4	0x800110460301143F	3124
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_0	0x800001460301143F	1978
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_1	0x800005460301143F	2098
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_2	0x800009460301143F	2218
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_3	0x80000D460301143F	2338
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_4	0x800011460301143F	2458
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_0	0x800101460301143F	2675
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_1	0x800105460301143F	2795
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_2	0x800109460301143F	2915
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_3	0x80010D460301143F	3035
DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_4	0x800111460301143F	3155

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DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_0	0x8000024603011 43F	2003
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_1	0x8000064603011 43F	2123
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_2	0x80000A4603011 43F	2243
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_3	0x80000E4603011 43F	2363
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_4	0x8000124603011 43F	2483
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_0	0x8001024603011 43F	2700
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_1	0x8001064603011 43F	2820
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_2	0x80010A4603011 43F	2940
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_3	0x80010E4603011 43F	3060
DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_4	0x8001124603011 43F	3180
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_0	0x8000034603011 43F	2027
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_1	0x8000074603011 43F	2147
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_2	0x80000B4603011 43F	2267
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_3	0x80000F4603011 43F	2387
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_4	0x8000134603011 43F	2507
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_0	0x8001034603011 43F	2724
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_1	0x8001074603011 43F	2844
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_2	0x80010B4603011 43F	2964
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_3	0x80010F4603011 43F	3084
DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_4	0x8001134603011 43F	3204
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_0	0x8000004703011 43F	1948
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_1	0x8000044703011 43F	2067
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_2	0x8000084703011 43F	2187
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_3	0x80000C4703011 43F	2307
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_4	0x8000104703011 43F	2427
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_0	0x8001004703011 43F	2644
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_1	0x8001044703011 43F	2764
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_2	0x8001084703011 43F	2884
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_3	0x80010C4703011 43F	3004
DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_4	0x8001104703011 43F	3124
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_0	0x8000014703011 43F	1979
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_1	0x8000054703011 43F	2099
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_2	0x8000094703011 43F	2219
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_3	0x80000D4703011 43F	2339
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_4	0x8000114703011 43F	2459
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_0	0x8001014703011 43F	2676
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_1	0x8001054703011 43F	2796
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_2	0x8001094703011 43F	2916
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_3	0x80010D4703011 43F	3036
DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_4	0x8001114703011 43F	3156
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_0	0x8000024703011 43F	2003
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_1	0x8000064703011 43F	2123
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_2	0x80000A4703011 43F	2243
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_3	0x80000E4703011 43F	2363
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_4	0x8000124703011 43F	2483
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_0	0x8001024703011 43F	2700
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_1	0x8001064703011 43F	2820
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_2	0x80010A4703011 43F	2940
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_3	0x80010E4703011 43F	3060
DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_4	0x8001124703011 43F	3180
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_0	0x8000034703011 43F	2027

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DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_1	0x8000074703011 43F	2147
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_2	0x80000B4703011 43F	2267
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_3	0x80000F4703011 43F	2387
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_4	0x8000134703011 43F	2507
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_0	0x8001034703011 43F	2724
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_1	0x8001074703011 43F	2844
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_2	0x80010B4703011 43F	2964
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_3	0x80010F4703011 43F	3084
DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_4	0x8001134703011 43F	3204
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_0	0x8000004803011 43F	1948
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_1	0x8000044803011 43F	2068
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_2	0x8000084803011 43F	2188
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_3	0x80000C4803011 43F	2308
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_4	0x8000104803011 43F	2428
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_0	0x8001004803011 43F	2645
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_1	0x8001044803011 43F	2765
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_2	0x8001084803011 43F	2885
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_3	0x80010C4803011 43F	3005
DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_4	0x8001104803011 43F	3125
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_0	0x8000014803011 43F	1979
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_1	0x8000054803011 43F	2099
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_2	0x8000094803011 43F	2219
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_3	0x80000D4803011 43F	2339
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_4	0x8000114803011 43F	2459
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_0	0x8001014803011 43F	2676
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_1	0x8001054803011 43F	2796
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_2	0x8001094803011 43F	2916
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_3	0x80010D4803011 43F	3036
DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_4	0x8001114803011 43F	3156
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_0	0x8000024803011 43F	2003
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_1	0x8000064803011 43F	2123
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_2	0x80000A4803011 43F	2243
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_3	0x80000E4803011 43F	2363
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_4	0x8000124803011 43F	2483
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_0	0x8001024803011 43F	2700
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_1	0x8001064803011 43F	2820
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_2	0x80010A4803011 43F	2940
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_3	0x80010E4803011 43F	3060
DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_4	0x8001124803011 43F	3180
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_0	0x8000034803011 43F	2028
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_1	0x8000074803011 43F	2148
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_2	0x80000B4803011 43F	2268
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_3	0x80000F4803011 43F	2388
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_4	0x8000134803011 43F	2508
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_0	0x8001034803011 43F	2725
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_1	0x8001074803011 43F	2845
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_2	0x80010B4803011 43F	2965
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_3	0x80010F4803011 43F	3085
DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_4	0x8001134803011 43F	3205
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_0	0x8000004A0301143F	1948
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_1	0x8000044A0301143F	2068

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DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_2	0x8000084A0301143F	2188
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_3	0x80000C4A0301143F	2308
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_4	0x8000104A0301143F	2428
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_0	0x8001004A0301143F	2645
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_1	0x8001044A0301143F	2765
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_2	0x8001084A0301143F	2885
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_3	0x80010C4A0301143F	3005
DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_4	0x8001104A0301143F	3125
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_0	0x8000014A0301143F	1979
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_1	0x8000054A0301143F	2099
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_2	0x8000094A0301143F	2219
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_3	0x80000D4A0301143F	2339
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_4	0x8000114A0301143F	2459
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_0	0x8001014A0301143F	2676
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_1	0x8001054A0301143F	2796
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_2	0x8001094A0301143F	2916
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_3	0x80010D4A0301143F	3036
DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_4	0x8001114A0301143F	3156
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_0	0x8000024A0301143F	2004
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_1	0x8000064A0301143F	2124
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_2	0x80000A4A0301143F	2244
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_3	0x80000E4A0301143F	2364
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_4	0x8000124A0301143F	2484
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_0	0x8001024A0301143F	2701
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_1	0x8001064A0301143F	2821
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_2	0x80010A4A0301143F	2941
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_3	0x80010E4A0301143F	3061
DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_4	0x8001124A0301143F	3181
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_0	0x8000034A0301143F	2028
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_1	0x8000074A0301143F	2148
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_2	0x80000B4A0301143F	2268
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_3	0x80000F4A0301143F	2388
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_4	0x8000134A0301143F	2508
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_0	0x8001034A0301143F	2725
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_1	0x8001074A0301143F	2845
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_2	0x80010B4A0301143F	2965
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_3	0x80010F4A0301143F	3085
DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_4	0x8001134A0301143F	3205
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_0	0x800000390301143F	1943
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_1	0x800004390301143F	2063
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_2	0x800008390301143F	2183
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_3	0x80000C390301143F	2303
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_4	0x800010390301143F	2423
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_0	0x800100390301143F	2640
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_1	0x800104390301143F	2760
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_2	0x800108390301143F	2880
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_3	0x80010C390301143F	3000
DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_4	0x800110390301143F	3120
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_0	0x800001390301143F	1974
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_1	0x800005390301143F	2094
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_2	0x800009390301143F	2214

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DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_3	0x80000D390301143F	2334
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_4	0x800011390301143F	2454
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_0	0x800101390301143F	2671
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_1	0x800105390301143F	2791
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_2	0x800109390301143F	2911
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_3	0x80010D390301143F	3031
DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_4	0x800111390301143F	3151
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_0	0x800002390301143F	1998
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_1	0x800006390301143F	2118
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_2	0x80000A390301143F	2238
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_3	0x80000E390301143F	2358
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_4	0x800012390301143F	2478
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_0	0x800102390301143F	2695
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_1	0x800106390301143F	2815
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_2	0x80010A390301143F	2935
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_3	0x80010E390301143F	3055
DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_4	0x800112390301143F	3175
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_0	0x800003390301143F	2023
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_1	0x800007390301143F	2143
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_2	0x80000B390301143F	2263
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_3	0x80000F390301143F	2383
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_4	0x800013390301143F	2503
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_0	0x800103390301143F	2720
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_1	0x800107390301143F	2840
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_2	0x80010B390301143F	2960
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_3	0x80010F390301143F	3080
DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_4	0x800113390301143F	3200
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_0	0x8000004C0301143F	1949
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_1	0x8000044C0301143F	2068
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_2	0x8000084C0301143F	2188
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_3	0x80000C4C0301143F	2308
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_4	0x8000104C0301143F	2428
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_0	0x8001004C0301143F	2645
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_1	0x8001044C0301143F	2765
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_2	0x8001084C0301143F	2885
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_3	0x80010C4C0301143F	3005
DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_4	0x8001104C0301143F	3125
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_0	0x8000014C0301143F	1980
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_1	0x8000054C0301143F	2100
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_2	0x8000094C0301143F	2220
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_3	0x80000D4C0301143F	2340
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_4	0x8000114C0301143F	2460
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_0	0x8001014C0301143F	2677
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_1	0x8001054C0301143F	2797
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_2	0x8001094C0301143F	2917
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_3	0x80010D4C0301143F	3037
DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_4	0x8001114C0301143F	3157
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_0	0x8000024C0301143F	2004
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_1	0x8000064C0301143F	2124
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_2	0x80000A4C0301143F	2244
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_3	0x80000E4C0301143F	2364

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DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_4	0x8000124C0301143F	2484
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_0	0x8001024C0301143F	2701
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_1	0x8001064C0301143F	2821
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_2	0x80010A4C0301143F	2941
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_3	0x80010E4C0301143F	3061
DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_4	0x8001124C0301143F	3181
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_0	0x8000034C0301143F	2028
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_1	0x8000074C0301143F	2148
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_2	0x80000B4C0301143F	2268
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_3	0x80000F4C0301143F	2388
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_4	0x8000134C0301143F	2508
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_0	0x8001034C0301143F	2725
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_1	0x8001074C0301143F	2845
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_2	0x80010B4C0301143F	2965
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_3	0x80010F4C0301143F	3085
DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_4	0x8001134C0301143F	3205
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_0	0x8000004E0301143F	1949
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_1	0x8000044E0301143F	2069
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_2	0x8000084E0301143F	2189
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_3	0x80000C4E0301143F	2309
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_4	0x8000104E0301143F	2429
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_0	0x8001004E0301143F	2646
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_1	0x8001044E0301143F	2766
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_2	0x8001084E0301143F	2886
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_3	0x80010C4E0301143F	3006
DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_4	0x8001104E0301143F	3126
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_0	0x8000014E0301143F	1980
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_1	0x8000054E0301143F	2100
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_2	0x8000094E0301143F	2220
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_3	0x80000D4E0301143F	2340
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_4	0x8000114E0301143F	2460
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_0	0x8001014E0301143F	2677
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_1	0x8001054E0301143F	2797
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_2	0x8001094E0301143F	2917
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_3	0x80010D4E0301143F	3037
DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_4	0x8001114E0301143F	3157
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_0	0x8000024E0301143F	2004
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_1	0x8000064E0301143F	2124
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_2	0x80000A4E0301143F	2244
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_3	0x80000E4E0301143F	2364
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_4	0x8000124E0301143F	2484
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_0	0x8001024E0301143F	2701
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_1	0x8001064E0301143F	2821
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_2	0x80010A4E0301143F	2941
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_3	0x80010E4E0301143F	3061
DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_4	0x8001124E0301143F	3181
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_0	0x8000034E0301143F	2029
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_1	0x8000074E0301143F	2149
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_2	0x80000B4E0301143F	2269
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_3	0x80000F4E0301143F	2389
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_4	0x8000134E0301143F	2509

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DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_0	0x8001034E0301143F	2726
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_1	0x8001074E0301143F	2846
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_2	0x80010B4E0301143F	2966
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_3	0x80010F4E0301143F	3086
DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_4	0x8001134E0301143F	3206
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_0	0x8000003A0301143F	1943
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_1	0x8000043A0301143F	2063
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_2	0x8000083A0301143F	2183
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_3	0x80000C3A0301143F	2303
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_4	0x8000103A0301143F	2423
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_0	0x8001003A0301143F	2640
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_1	0x8001043A0301143F	2760
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_2	0x8001083A0301143F	2880
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_3	0x80010C3A0301143F	3000
DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_4	0x8001103A0301143F	3120
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_0	0x8000013A0301143F	1974
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_1	0x8000053A0301143F	2094
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_2	0x8000093A0301143F	2214
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_3	0x80000D3A0301143F	2334
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_4	0x8000113A0301143F	2454
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_0	0x8001013A0301143F	2671
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_1	0x8001053A0301143F	2791
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_2	0x8001093A0301143F	2911
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_3	0x80010D3A0301143F	3031
DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_4	0x8001113A0301143F	3151
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_0	0x8000023A0301143F	1999
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_1	0x8000063A0301143F	2119
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_2	0x80000A3A0301143F	2239
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_3	0x80000E3A0301143F	2359
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_4	0x8000123A0301143F	2479
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_0	0x8001023A0301143F	2696
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_1	0x8001063A0301143F	2816
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_2	0x80010A3A0301143F	2936
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_3	0x80010E3A0301143F	3056
DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_4	0x8001123A0301143F	3176
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_0	0x8000033A0301143F	2023
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_1	0x8000073A0301143F	2143
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_2	0x80000B3A0301143F	2263
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_3	0x80000F3A0301143F	2383
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_4	0x8000133A0301143F	2503
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_0	0x8001033A0301143F	2720
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_1	0x8001073A0301143F	2840
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_2	0x80010B3A0301143F	2960
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_3	0x80010F3A0301143F	3080
DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_4	0x8001133A0301143F	3200
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_0	0x8000003B0301143F	1944
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_1	0x8000043B0301143F	2063
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_2	0x8000083B0301143F	2183
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_3	0x80000C3B0301143F	2303
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_4	0x8000103B0301143F	2423
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_0	0x8001003B0301143F	2640

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DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_1	0x8001043B0301143F	2760
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_2	0x8001083B0301143F	2880
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_3	0x80010C3B0301143F	3000
DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_4	0x8001103B0301143F	3120
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_0	0x8000013B0301143F	1975
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_1	0x8000053B0301143F	2095
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_2	0x8000093B0301143F	2215
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_3	0x80000D3B0301143F	2335
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_4	0x8000113B0301143F	2455
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_0	0x8001013B0301143F	2672
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_1	0x8001053B0301143F	2792
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_2	0x8001093B0301143F	2912
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_3	0x80010D3B0301143F	3032
DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_4	0x8001113B0301143F	3152
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_0	0x8000023B0301143F	1999
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_1	0x8000063B0301143F	2119
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_2	0x80000A3B0301143F	2239
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_3	0x80000E3B0301143F	2359
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_4	0x8000123B0301143F	2479
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_0	0x8001023B0301143F	2696
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_1	0x8001063B0301143F	2816
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_2	0x80010A3B0301143F	2936
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_3	0x80010E3B0301143F	3056
DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_4	0x8001123B0301143F	3176
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_0	0x8000033B0301143F	2023
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_1	0x8000073B0301143F	2143
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_2	0x80000B3B0301143F	2263
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_3	0x80000F3B0301143F	2383
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_4	0x8000133B0301143F	2503
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_0	0x8001033B0301143F	2720
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_1	0x8001073B0301143F	2840
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_2	0x80010B3B0301143F	2960
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_3	0x80010F3B0301143F	3080
DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_4	0x8001133B0301143F	3200
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_0	0x8000003C0301143F	1944
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_1	0x8000043C0301143F	2064
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_2	0x8000083C0301143F	2184
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_3	0x80000C3C0301143F	2304
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_4	0x8000103C0301143F	2424
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_0	0x8001003C0301143F	2641
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_1	0x8001043C0301143F	2761
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_2	0x8001083C0301143F	2881
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_3	0x80010C3C0301143F	3001
DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_4	0x8001103C0301143F	3121
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_0	0x8000013C0301143F	1975
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_1	0x8000053C0301143F	2095
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_2	0x8000093C0301143F	2215
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_3	0x80000D3C0301143F	2335
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_4	0x8000113C0301143F	2455
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_0	0x8001013C0301143F	2672
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_1	0x8001053C0301143F	2792

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DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_2	0x8001093C0301143F	2912
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_3	0x80010D3C0301143F	3032
DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_4	0x8001113C0301143F	3152
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_0	0x8000023C0301143F	1999
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_1	0x8000063C0301143F	2119
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_2	0x80000A3C0301143F	2239
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_3	0x80000E3C0301143F	2359
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_4	0x8000123C0301143F	2479
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_0	0x8001023C0301143F	2696
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_1	0x8001063C0301143F	2816
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_2	0x80010A3C0301143F	2936
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_3	0x80010E3C0301143F	3056
DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_4	0x8001123C0301143F	3176
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_0	0x8000033C0301143F	2024
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_1	0x8000073C0301143F	2144
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_2	0x80000B3C0301143F	2264
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_3	0x80000F3C0301143F	2384
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_4	0x8000133C0301143F	2504
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_0	0x8001033C0301143F	2721
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_1	0x8001073C0301143F	2841
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_2	0x80010B3C0301143F	2961
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_3	0x80010F3C0301143F	3081
DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_4	0x8001133C0301143F	3201
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_0	0x8000003D0301143F	1944
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_1	0x8000043D0301143F	2064
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_2	0x8000083D0301143F	2184
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_3	0x80000C3D0301143F	2304
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_4	0x8000103D0301143F	2424
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_0	0x8001003D0301143F	2641
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_1	0x8001043D0301143F	2761
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_2	0x8001083D0301143F	2881
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_3	0x80010C3D0301143F	3001
DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_4	0x8001103D0301143F	3121
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_0	0x8000013D0301143F	1975
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_1	0x8000053D0301143F	2095
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_2	0x8000093D0301143F	2215
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_3	0x80000D3D0301143F	2335
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_4	0x8000113D0301143F	2455
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_0	0x8001013D0301143F	2672
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_1	0x8001053D0301143F	2792
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_2	0x8001093D0301143F	2912
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_3	0x80010D3D0301143F	3032
DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_4	0x8001113D0301143F	3152
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_0	0x8000023D0301143F	2000
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_1	0x8000063D0301143F	2120
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_2	0x80000A3D0301143F	2240
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_3	0x80000E3D0301143F	2360
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_4	0x8000123D0301143F	2480
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_0	0x8001023D0301143F	2697
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_1	0x8001063D0301143F	2817
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_2	0x80010A3D0301143F	2937

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DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_3	0x80010E3D0301143F	3057
DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_4	0x8001123D0301143F	3177
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_0	0x8000033D0301143F	2024
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_1	0x8000073D0301143F	2144
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_2	0x80000B3D0301143F	2264
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_3	0x80000F3D0301143F	2384
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_4	0x8000133D0301143F	2504
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_0	0x8001033D0301143F	2721
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_1	0x8001073D0301143F	2841
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_2	0x80010B3D0301143F	2961
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_3	0x80010F3D0301143F	3081
DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_4	0x8001133D0301143F	3201
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_0	0x8000003E0301143F	1945
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_1	0x8000043E0301143F	2064
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_2	0x8000083E0301143F	2184
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_3	0x80000C3E0301143F	2304
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_4	0x8000103E0301143F	2424
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_0	0x8001003E0301143F	2641
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_1	0x8001043E0301143F	2761
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_2	0x8001083E0301143F	2881
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_3	0x80010C3E0301143F	3001
DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_4	0x8001103E0301143F	3121
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_0	0x8000013E0301143F	1976
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_1	0x8000053E0301143F	2096
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_2	0x8000093E0301143F	2216
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_3	0x80000D3E0301143F	2336
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_4	0x8000113E0301143F	2456
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_0	0x8001013E0301143F	2673
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_1	0x8001053E0301143F	2793
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_2	0x8001093E0301143F	2913
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_3	0x80010D3E0301143F	3033
DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_4	0x8001113E0301143F	3153
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_0	0x8000023E0301143F	2000
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_1	0x8000063E0301143F	2120
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_2	0x80000A3E0301143F	2240
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_3	0x80000E3E0301143F	2360
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_4	0x8000123E0301143F	2480
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_0	0x8001023E0301143F	2697
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_1	0x8001063E0301143F	2817
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_2	0x80010A3E0301143F	2937
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_3	0x80010E3E0301143F	3057
DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_4	0x8001123E0301143F	3177
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_0	0x8000033E0301143F	2024
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_1	0x8000073E0301143F	2144
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_2	0x80000B3E0301143F	2264
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_3	0x80000F3E0301143F	2384
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_4	0x8000133E0301143F	2504
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_0	0x8001033E0301143F	2721
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_1	0x8001073E0301143F	2841
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_2	0x80010B3E0301143F	2961
DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_3	0x80010F3E0301143F	3081

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DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_4	0x8001133E0301143F	3201
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_0	0x8000003F0301143F	1945
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_1	0x8000043F0301143F	2065
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_2	0x8000083F0301143F	2185
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_3	0x80000C3F0301143F	2305
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_4	0x8000103F0301143F	2425
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_0	0x8001003F0301143F	2642
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_1	0x8001043F0301143F	2762
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_2	0x8001083F0301143F	2882
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_3	0x80010C3F0301143F	3002
DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_4	0x8001103F0301143F	3122
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_0	0x8000013F0301143F	1976
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_1	0x8000053F0301143F	2096
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_2	0x8000093F0301143F	2216
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_3	0x80000D3F0301143F	2336
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_4	0x8000113F0301143F	2456
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_0	0x8001013F0301143F	2673
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_1	0x8001053F0301143F	2793
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_2	0x8001093F0301143F	2913
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_3	0x80010D3F0301143F	3033
DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_4	0x8001113F0301143F	3153
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_0	0x8000023F0301143F	2000
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_1	0x8000063F0301143F	2120
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_2	0x80000A3F0301143F	2240
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_3	0x80000E3F0301143F	2360
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_4	0x8000123F0301143F	2480
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_0	0x8001023F0301143F	2697
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_1	0x8001063F0301143F	2817
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_2	0x80010A3F0301143F	2937
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_3	0x80010E3F0301143F	3057
DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_4	0x8001123F0301143F	3177
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_0	0x8000033F0301143F	2025
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_1	0x8000073F0301143F	2145
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_2	0x80000B3F0301143F	2265
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_3	0x80000F3F0301143F	2385
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_4	0x8000133F0301143F	2505
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_0	0x8001033F0301143F	2722
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_1	0x8001073F0301143F	2842
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_2	0x80010B3F0301143F	2962
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_3	0x80010F3F0301143F	3082
DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_4	0x8001133F0301143F	3202
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_0	0x800000400301143F	1945
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_1	0x800004400301143F	2065
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_2	0x800008400301143F	2185
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_3	0x80000C400301143F	2305
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_4	0x800010400301143F	2425
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_0	0x800100400301143F	2642
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_1	0x800104400301143F	2762
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_2	0x800108400301143F	2882
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_3	0x80010C400301143F	3002
DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_4	0x800110400301143F	3122

Mnemonic	Address	Page
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_0	0x8000014003011 43F	1976
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_1	0x8000054003011 43F	2096
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_2	0x8000094003011 43F	2216
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_3	0x80000D4003011 43F	2336
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_4	0x8000114003011 43F	2456
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_0	0x8001014003011 43F	2673
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_1	0x8001054003011 43F	2793
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_2	0x8001094003011 43F	2913
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_3	0x80010D4003011 43F	3033
DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_4	0x8001114003011 43F	3153
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_0	0x8000024003011 43F	2001
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_1	0x8000064003011 43F	2121
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_2	0x80000A4003011 43F	2241
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_3	0x80000E4003011 43F	2361
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_4	0x8000124003011 43F	2481
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_0	0x8001024003011 43F	2698
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_1	0x8001064003011 43F	2818
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_2	0x80010A4003011 43F	2938
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_3	0x80010E4003011 43F	3058
DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_4	0x8001124003011 43F	3178
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_0	0x8000034003011 43F	2025
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_1	0x8000074003011 43F	2145
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_2	0x80000B4003011 43F	2265
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_3	0x80000F4003011 43F	2385
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_4	0x8000134003011 43F	2505
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_0	0x8001034003011 43F	2722
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_1	0x8001074003011 43F	2842
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_2	0x80010B4003011 43F	2962
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_3	0x80010F4003011 43F	3082
DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_4	0x8001134003011 43F	3202
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_0	0x8000041030114 3F	1946
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_1	0x8000441030114 3F	2065
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_2	0x8000841030114 3F	2185
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_3	0x80000C4103011 43F	2305
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_4	0x8000104103011 43F	2425
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_0	0x8001004103011 43F	2642
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_1	0x8001044103011 43F	2762
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_2	0x8001084103011 43F	2882
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_3	0x80010C4103011 43F	3002
DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_4	0x8001104103011 43F	3122
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_0	0x8000014103011 43F	1977
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_1	0x8000054103011 43F	2097
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_2	0x8000094103011 43F	2217
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_3	0x80000D4103011 43F	2337
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_4	0x8000114103011 43F	2457
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_0	0x8001014103011 43F	2674
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_1	0x8001054103011 43F	2794
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_2	0x8001094103011 43F	2914
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_3	0x80010D4103011 43F	3034
DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_4	0x8001114103011 43F	3154
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_0	0x8000024103011 43F	2001

Mnemonic	Address	Page
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_1	0x8000064103011 43F	2121
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_2	0x80000A410301143F	2241
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_3	0x80000E410301143F	2361
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_4	0x8000124103011 43F	2481
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_0	0x8001024103011 43F	2698
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_1	0x8001064103011 43F	2818
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_2	0x80010A410301143F	2938
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_3	0x80010E410301143F	3058
DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_4	0x8001124103011 43F	3178
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_0	0x8000034103011 43F	2025
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_1	0x8000074103011 43F	2145
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_2	0x80000B410301143F	2265
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_3	0x80000F410301143F	2385
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_4	0x8000134103011 43F	2505
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_0	0x8001034103011 43F	2722
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_1	0x8001074103011 43F	2842
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_2	0x80010B410301143F	2962
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_3	0x80010F410301143F	3082
DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_4	0x8001134103011 43F	3202
DPHY01.PHY01_DDRPHY_FIR_ACTION0_REG	0x8002009603011 43F	3316
DPHY01.PHY01_DDRPHY_FIR_ACTION1_REG	0x8002009703011 43F	3317
DPHY01.PHY01_DDRPHY_FIR_MASK_REG	0x8002009303011 43F	3315
DPHY01.PHY01_DDRPHY_FIR_REG	0x8002009003011 43F	3315
DPHY01.PHY01_DDRPHY_FIR_WOF_REG	0x8002009803011 43F	3317

The memory buffer registers are listed in the following tables.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_0
Address	800000000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P0_DP18_0_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_0
Address	800000010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_HW_VALUE:
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_0
Address	800000020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P0_DP18_0_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_0
Address	800000030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_0
Address	800000040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_0
Address	800000050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_0
Address	800000060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers . '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers , staggered across DQ lanes as specified by the registers, and and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_0
Address	800000070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_0
Address	800000080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_0
Address	800000090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_0
Address	8000000A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_0_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_0_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_0
Address	8000000B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_0
Address	8000000C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_0
Address	8000000D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_0
Address	8000000E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P0_DP18_0_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_0
Address	8000000F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P0_DP18_0_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Centering Status 2*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_0
Address	800000100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P0_DP18_0_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_0
Address	800000110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P0_DP18_0_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_0
Address	800000120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_0
Address	800000130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P0_0
Address	800000140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.

Bits	SCOM	Field Mnemonic: Description
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.

Bits	SCOM	Field Mnemonic: Description
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register . The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register . The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_0
Address	800000150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_0
Address	800000170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_0
Address	800000180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_0
Address	800000190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P0_DP18_0_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_0
Address	8000001A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P0_DP18_0_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P0_0
Address	8000001B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	***DP18 Write Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_0
Address	8000001C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_0
Address	8000001D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_0_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_0_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B

Bits	SCOM	Field Mnemonic: Description
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_0_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_0
Address	800000300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_0
Address	800000310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_0
Address	800000320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD00_POS: MEMINTD00 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_0
Address	800000330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	*DP18 Pattern Position 2*
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_0
Address	800000340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	*DP18 DQSClk Offset*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_0
Address	800000370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P0_DP18_0_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_0
Address	800000380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_0
Address	800000390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_0
Address	8000003A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_0
Address	8000003B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_0
Address	8000003C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_0
Address	8000003D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_0
Address	8000003E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_0
Address	8000003F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_0
Address	800000400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_0
Address	800000410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_0
Address	800000420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_0
Address	800000430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_0
Address	800000440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_0
Address	800000450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_0
Address	800000460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_0
Address	800000470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_0
Address	800000480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_0
Address	8000004A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_0
Address	8000004C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_0
Address	8000004E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_0
Address	800000500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_0
Address	800000510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_0
Address	800000520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers in this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_0
Address	800000530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers , then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_0
Address	800000540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers , this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers , then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_0
Address	800000550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_0
Address	800000560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_0
Address	800000570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_0
Address	8000005C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_0
Address	8000005D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_0
Address	800000600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_0
Address	800000610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_0
Address	800000620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_0
Address	800000630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_0
Address	800000640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_0
Address	800000650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_0
Address	800000660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_0
Address	800000670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_0
Address	800000680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_0
Address	800000690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_0
Address	8000006A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_0
Address	8000006B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_0
Address	8000006D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_0_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_0_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0
Address	8000006F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.

Bits	SCOM	Field Mnemonic: Description
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_0
Address	800000700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_0_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_0_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_0
Address	800000710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_0_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_0_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_0
Address	800000720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P0_DP18_0_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.
56:63	RO	constant=0b00000000

Register Name	***DP18 SysClk Phase Rotator Value***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_0
Address	800000730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_0_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	***DP18 WrClk Phase Rotator Offset Value***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P0_0
Address	800000740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P0_DP18_0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	***DP18 IO TX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_0
Address	800000750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_0_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_0_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_0_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_0
Address	800000760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_0
Address	800000770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_0
Address	800000780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_0_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_0_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_0
Address	800000790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_0_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_0_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_0
Address	8000007A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_0_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_0_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_0
Address	8000007B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_0_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_0_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_0
Address	8000007C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_0
Address	8000007D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_0
Address	8000007E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_0
Address	800001040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_0
Address	800001050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_0
Address	800001090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_0
Address	8000010C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_0
Address	8000010D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_0
Address	800001130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_0
Address	800001300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_0
Address	800001310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_0
Address	800001380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_0
Address	800001390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_0
Address	8000013A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_0
Address	8000013B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_0
Address	8000013C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_0
Address	8000013D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_0
Address	8000013E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_0
Address	8000013F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_0
Address	800001400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_0
Address	800001410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_0
Address	800001420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_0
Address	800001430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_0
Address	800001440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_0
Address	800001450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_0
Address	800001460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_0
Address	800001470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_0
Address	800001480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_0
Address	8000014A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_0
Address	8000014C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_0
Address	8000014E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_0
Address	800001500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_0
Address	800001510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_0
Address	800001520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_0
Address	800001530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_0
Address	800001540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_0
Address	800001550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_0
Address	800001560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_0
Address	800001570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_0
Address	8000015C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_0
Address	8000015D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_0
Address	800001600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_0
Address	800001610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_0
Address	800001620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_0
Address	800001630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_0
Address	800001640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_0
Address	800001650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_0
Address	800001660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_0
Address	800001670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_0
Address	800001680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_0
Address	800001690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_0
Address	8000016A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_0
Address	8000016B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_0
Address	8000017C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_0
Address	8000017D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_0
Address	8000017E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_0
Address	800002040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_0
Address	800002050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_0
Address	800002090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_0
Address	8000020C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_0
Address	8000020D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_0
Address	800002130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_0
Address	800002300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_0
Address	800002310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_0
Address	800002380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_0
Address	800002390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_0
Address	8000023A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_0
Address	8000023B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_0
Address	8000023C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_0
Address	8000023D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_0
Address	8000023E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_0
Address	8000023F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_0
Address	800002400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_0
Address	800002410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_0
Address	800002420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_0
Address	800002430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_0
Address	800002440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_0
Address	800002450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_0
Address	800002460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_0
Address	800002470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_0
Address	800002480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_0
Address	8000024A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_0
Address	8000024C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_0
Address	8000024E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_0
Address	800002500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_0
Address	800002510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_0
Address	800002520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_0
Address	800002530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_0
Address	800002540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_0
Address	800002550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_0
Address	800002560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_0
Address	800002570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_0
Address	8000025C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_0
Address	8000025D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_0
Address	800002600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_0
Address	800002610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_0
Address	800002620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_0
Address	800002630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_0
Address	800002640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_0
Address	800002650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_0
Address	800002660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_0
Address	800002670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_0
Address	800002680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_0
Address	800002690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_0
Address	8000026A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_0
Address	8000026B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_0
Address	8000027C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_0
Address	8000027D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_0
Address	8000027E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_0
Address	800003040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_0
Address	800003050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_0
Address	800003090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_0
Address	8000030C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_0
Address	8000030D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_0
Address	800003130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_0
Address	800003300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_0
Address	800003310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_0
Address	800003380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_0
Address	800003390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_0
Address	8000033A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_0
Address	8000033B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_0
Address	8000033C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_0
Address	8000033D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_0
Address	8000033E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_0
Address	8000033F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_0
Address	800003400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_0
Address	800003410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_0
Address	800003420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_0
Address	800003430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_0
Address	800003440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_0
Address	800003450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_0
Address	800003460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_0
Address	800003470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_0
Address	800003480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_0
Address	8000034A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_0
Address	8000034C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_0
Address	8000034E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_0
Address	800003500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP3*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_0
Address	800003510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 2 RP3*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_0
Address	800003520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_0
Address	800003530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_0
Address	800003540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_0
Address	800003550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_0
Address	800003560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_0
Address	800003570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_0
Address	8000035C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_0
Address	8000035D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_0
Address	800003600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_0
Address	800003610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_0
Address	800003620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_0
Address	800003630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_0
Address	800003640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_0
Address	800003650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_0
Address	800003660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_0
Address	800003670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_0
Address	800003680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_0
Address	800003690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_0
Address	8000036A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_0
Address	8000036B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_0
Address	8000037C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_0
Address	8000037D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_0
Address	8000037E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_1
Address	800004000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P0_DP18_1_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_1
Address	800004010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_HW_VALUE:
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_1
Address	800004020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P0_DP18_1_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_1
Address	800004030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_1
Address	800004040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_1
Address	800004050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_1
Address	800004060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core. See for more information.
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers, rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_1
Address	800004070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_1
Address	800004080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_1
Address	800004090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_1
Address	8000040A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_1_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_1_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_1
Address	8000040B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_1
Address	8000040C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_1
Address	8000040D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_1
Address	8000040E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P0_DP18_1_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_1
Address	8000040F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P0_DP18_1_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_1
Address	800004100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P0_DP18_1_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_1
Address	800004110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P0_DP18_1_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_1
Address	800004120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_1
Address	800004130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P0_1
Address	800004140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_1
Address	800004150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_1
Address	800004170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_1
Address	800004180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_1
Address	800004190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P0_DP18_1_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_1
Address	8000041A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P0_DP18_1_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P0_1
Address	8000041B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_1
Address	8000041C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_1
Address	8000041D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_1_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_1_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_1_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_1
Address	800004300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_1
Address	800004310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_1
Address	800004320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_1
Address	800004330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_1
Address	800004340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_1
Address	800004370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P0_DP18_1_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_1
Address	800004380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_1
Address	800004390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_1
Address	8000043A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_1
Address	8000043B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_1
Address	8000043C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_1
Address	8000043D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_1
Address	8000043E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_1
Address	8000043F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_1
Address	800004400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_1
Address	800004410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_1
Address	800004420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_1
Address	800004430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_1
Address	800004440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_1
Address	800004450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_1
Address	800004460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_1
Address	800004470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_1
Address	800004480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_1
Address	8000044A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_1
Address	8000044C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_1
Address	8000044E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_1
Address	800004500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_1
Address	800004510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_1
Address	800004520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_1
Address	800004530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_1
Address	800004540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_1
Address	800004550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_1
Address	800004560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_1
Address	800004570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_1
Address	8000045C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_1
Address	8000045D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_1
Address	800004600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_1
Address	800004610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_1
Address	800004620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_1
Address	800004630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_1
Address	800004640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_1
Address	800004650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_1
Address	800004660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_1
Address	800004670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_1
Address	800004680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_1
Address	800004690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_1
Address	8000046A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_1
Address	8000046B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_1
Address	8000046D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_1_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_1_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1
Address	8000046F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_1
Address	800004700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_1_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_1_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_1
Address	800004710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_1_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_1_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_1
Address	800004720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P0_DP18_1_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_1
Address	800004730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_1_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P0_1
Address	800004740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P0_DP18_1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_1
Address	800004750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_1_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_1_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_1_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_1
Address	800004760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_1
Address	800004770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_1
Address	800004780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_1_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_1_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_1
Address	800004790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_1_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_1_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_1
Address	8000047A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_1_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_1_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_1
Address	8000047B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_1_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_1_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_1
Address	8000047C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_1
Address	8000047D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_1
Address	8000047E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_1
Address	800005040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_1
Address	800005050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_1
Address	800005090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_1
Address	8000050C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_1
Address	8000050D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_1
Address	800005130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_1
Address	800005300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_1
Address	800005310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_1
Address	800005380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_1
Address	800005390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_1
Address	8000053A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_1
Address	8000053B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_1
Address	8000053C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_1
Address	8000053D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_1
Address	8000053E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_1
Address	8000053F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_1
Address	800005400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_1
Address	800005410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_1
Address	800005420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_1
Address	800005430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_1
Address	800005440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_1
Address	800005450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_1
Address	800005460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_1
Address	800005470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_1
Address	800005480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_1
Address	8000054A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_1
Address	8000054C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_1
Address	8000054E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_1
Address	800005500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_1
Address	800005510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_1
Address	800005520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_1
Address	800005530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_1
Address	800005540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_1
Address	800005550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_1
Address	800005560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_1
Address	800005570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_1
Address	8000055C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_1
Address	8000055D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_1
Address	800005600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_1
Address	800005610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_1
Address	800005620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_1
Address	800005630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_1
Address	800005640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_1
Address	800005650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_1
Address	800005660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_1
Address	800005670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_1
Address	800005680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_1
Address	800005690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_1
Address	8000056A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_1
Address	8000056B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_1
Address	8000057C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_1
Address	8000057D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_1
Address	8000057E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_1
Address	800006040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_1
Address	800006050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_1
Address	800006090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_1
Address	8000060C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_1
Address	8000060D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_1
Address	800006130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_1
Address	800006300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_1
Address	800006310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_1
Address	800006380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_1
Address	800006390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_1
Address	8000063A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_1
Address	8000063B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_1
Address	8000063C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_1
Address	8000063D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_1
Address	8000063E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_1
Address	8000063F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_1
Address	800006400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_1
Address	800006410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_1
Address	800006420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_1
Address	800006430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_1
Address	800006440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_1
Address	800006450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_1
Address	800006460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_1
Address	800006470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_1
Address	800006480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_1
Address	8000064A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_1
Address	8000064C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_1
Address	8000064E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_1
Address	800006500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_1
Address	800006510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_1
Address	800006520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_1
Address	800006530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_1
Address	800006540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_1
Address	800006550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_1
Address	800006560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_1
Address	800006570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_1
Address	8000065C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_1
Address	8000065D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_1
Address	800006600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_1
Address	800006610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_1
Address	800006620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_1
Address	800006630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_1
Address	800006640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_1
Address	800006650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_1
Address	800006660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_1
Address	800006670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_1
Address	800006680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_1
Address	800006690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_1
Address	8000066A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_1
Address	8000066B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_1
Address	8000067C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_1
Address	8000067D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_1
Address	8000067E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_1
Address	800007040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_1
Address	800007050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_1
Address	800007090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_1
Address	8000070C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_1
Address	8000070D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_1
Address	800007130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_1
Address	800007300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_1
Address	800007310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_1
Address	800007380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_1
Address	800007390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_1
Address	8000073A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_1
Address	8000073B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_1
Address	8000073C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_1
Address	8000073D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_1
Address	8000073E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_1
Address	8000073F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_1
Address	800007400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_1
Address	800007410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_1
Address	800007420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_1
Address	800007430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_1
Address	800007440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_1
Address	800007450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_1
Address	800007460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_1
Address	800007470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_1
Address	800007480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_1
Address	8000074A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_1
Address	8000074C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_1
Address	8000074E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_1
Address	800007500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_1
Address	800007510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_1
Address	800007520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_1
Address	800007530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_1
Address	800007540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_1
Address	800007550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_1
Address	800007560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_1
Address	800007570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_1
Address	8000075C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_1
Address	8000075D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_1
Address	800007600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_1
Address	800007610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_1
Address	800007620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_1
Address	800007630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_1
Address	800007640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_1
Address	800007650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_1
Address	800007660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_1
Address	800007670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_1
Address	800007680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_1
Address	800007690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_1
Address	8000076A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_1
Address	8000076B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_1
Address	8000077C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_1
Address	8000077D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_1
Address	8000077E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_2
Address	800008000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P0_DP18_2_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_2
Address	800008010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_HW_VALUE:
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_2
Address	800008020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P0_DP18_2_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_2
Address	800008030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_2
Address	800008040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_2
Address	800008050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_2
Address	800008060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core. See for more information.
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core. See for more information.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field . For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_2
Address	800008070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_2
Address	800008080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_2
Address	800008090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_2
Address	8000080A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_2_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_2_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_2
Address	8000080B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_2
Address	8000080C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_2
Address	8000080D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_2
Address	8000080E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P0_DP18_2_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_2
Address	8000080F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P0_DP18_2_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_2
Address	800008100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P0_DP18_2_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_2
Address	800008110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P0_DP18_2_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_2
Address	800008120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_2
Address	800008130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P0_2
Address	800008140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_2
Address	800008150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_2
Address	800008170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_2
Address	800008180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_2
Address	800008190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P0_DP18_2_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_2
Address	8000081A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P0_DP18_2_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P0_2
Address	8000081B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_2
Address	8000081C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_2
Address	8000081D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_2_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_2_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_2_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_2
Address	800008300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_2
Address	800008310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_2
Address	800008320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_2
Address	800008330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_2
Address	800008340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_2
Address	800008370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P0_DP18_2_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_2
Address	800008380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_2
Address	800008390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_2
Address	8000083A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_2
Address	8000083B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_2
Address	8000083C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_2
Address	8000083D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_2
Address	8000083E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_2
Address	8000083F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_2
Address	800008400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_2
Address	800008410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_2
Address	800008420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_2
Address	800008430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_2
Address	800008440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_2
Address	800008450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_2
Address	800008460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_2
Address	800008470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_2
Address	800008480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_2
Address	8000084A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_2
Address	8000084C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_2
Address	8000084E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_2
Address	800008500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_2
Address	800008510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_2
Address	800008520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_2
Address	800008530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_2
Address	800008540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_2
Address	800008550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_2
Address	800008560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_2
Address	800008570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_2
Address	8000085C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_2
Address	8000085D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_2
Address	800008600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_2
Address	800008610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_2
Address	800008620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_2
Address	800008630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_2
Address	800008640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_2
Address	800008650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_2
Address	800008660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_2
Address	800008670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_2
Address	800008680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_2
Address	800008690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_2
Address	8000086A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_2
Address	8000086B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_2
Address	8000086D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_2_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_2_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2
Address	8000086F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_2
Address	800008700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_2_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_2_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_2
Address	800008710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_2_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_2_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_2
Address	800008720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P0_DP18_2_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_2
Address	800008730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_2_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_2_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field .
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P0_2
Address	800008740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P0_DP18_2_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_2
Address	800008750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_2_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_2_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_2_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_2
Address	800008760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_2
Address	800008770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_2
Address	800008780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_2_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_2_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_2
Address	800008790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_2_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_2_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_2
Address	8000087A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_2_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_2_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_2
Address	8000087B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_2_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_2_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_2
Address	8000087C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_2
Address	8000087D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_2
Address	8000087E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_2
Address	800009040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_2
Address	800009050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_2
Address	800090903011 43F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_2
Address	8000090C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_2
Address	8000090D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_2
Address	800009130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_2
Address	800009300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_2
Address	800009310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_2
Address	800009380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_2
Address	800009390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_2
Address	8000093A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_2
Address	8000093B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_2
Address	8000093C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_2
Address	8000093D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_2
Address	8000093E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_2
Address	8000093F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_2
Address	800009400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_2
Address	800009410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_2
Address	800009420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_2
Address	800009430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_2
Address	800009440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_2
Address	800009450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_2
Address	800009460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_2
Address	800009470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_2
Address	800009480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_2
Address	8000094A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_2
Address	8000094C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_2
Address	8000094E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP1*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_2
Address	800009500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_2
Address	800009510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_2
Address	800009520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_2
Address	800009530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_2
Address	800009540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_2
Address	800009550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_2
Address	800009560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_2
Address	800009570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_2
Address	8000095C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_2
Address	8000095D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_2
Address	800009600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_2
Address	800009610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_2
Address	800009620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_2
Address	800009630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_2
Address	800009640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_2
Address	800009650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_2
Address	800009660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_2
Address	800009670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_2
Address	800009680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_2
Address	800009690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_2
Address	8000096A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_2
Address	8000096B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_2
Address	8000097C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_2
Address	8000097D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_2
Address	8000097E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_2
Address	80000A040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_2
Address	80000A050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_2
Address	80000A090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_2
Address	80000A0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_2
Address	80000A0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_2
Address	80000A130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_2
Address	80000A300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_2
Address	80000A310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_2
Address	80000A380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_2
Address	80000A390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_2
Address	80000A3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_2
Address	80000A3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_2
Address	80000A3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_2
Address	80000A3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_2
Address	80000A3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_2
Address	80000A3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_2
Address	80000A400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_2
Address	80000A410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_2
Address	80000A420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_2
Address	80000A430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_2
Address	80000A440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_2
Address	80000A450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_2
Address	80000A460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_2
Address	80000A470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_2
Address	80000A480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_2
Address	80000A4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_2
Address	80000A4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_2
Address	80000A4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_2
Address	80000A500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_2
Address	80000A510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_2
Address	80000A520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_2
Address	80000A530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_2
Address	80000A540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_2
Address	80000A550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_2
Address	80000A560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_2
Address	80000A570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_2
Address	80000A5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_2
Address	80000A5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_2
Address	80000A600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_2
Address	80000A610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_2
Address	80000A620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_2
Address	80000A630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_2
Address	80000A640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_2
Address	80000A650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_2
Address	80000A660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_2
Address	80000A670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_2
Address	80000A680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_2
Address	80000A690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_2
Address	80000A6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_2
Address	80000A6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_2
Address	80000A7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_2
Address	80000A7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_2
Address	80000A7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_2
Address	80000B040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_2
Address	80000B050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_2
Address	80000B090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_2
Address	80000B0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_2
Address	80000B0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_2
Address	80000B130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_2
Address	80000B300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_2
Address	80000B310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_2
Address	80000B380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_2
Address	80000B390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_2
Address	80000B3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_2
Address	80000B3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_2
Address	80000B3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_2
Address	80000B3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_2
Address	80000B3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_2
Address	80000B3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_2
Address	80000B400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_2
Address	80000B410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_2
Address	80000B420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_2
Address	80000B430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_2
Address	80000B440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_2
Address	80000B450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_2
Address	80000B460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_2
Address	80000B470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_2
Address	80000B480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_2
Address	80000B4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_2
Address	80000B4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_2
Address	80000B4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_2
Address	80000B500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_2
Address	80000B510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_2
Address	80000B520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_2
Address	80000B530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_2
Address	80000B540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_2
Address	80000B550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_2
Address	80000B560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_2
Address	80000B570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_2
Address	80000B5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_2
Address	80000B5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_2
Address	80000B600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_2
Address	80000B610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_2
Address	80000B620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_2
Address	80000B630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_2
Address	80000B640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_2
Address	80000B650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_2
Address	80000B660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_2
Address	80000B670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_2
Address	80000B680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_2
Address	80000B690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_2
Address	80000B6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_2
Address	80000B6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_2
Address	80000B7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_2
Address	80000B7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_2
Address	80000B7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_3
Address	80000C000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P0_DP18_3_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_3
Address	80000C010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_HW_VALUE:
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_3
Address	80000C020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P0_DP18_3_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_3
Address	80000C030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_3
Address	80000C040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_3
Address	80000C050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_3
Address	80000C060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core. See for more information.
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core. See for more information.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field . For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_3
Address	80000C070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_3
Address	80000C080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_3
Address	80000C090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_3
Address	80000C0A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_3_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_3_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_3
Address	80000C0B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_3
Address	80000C0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_3
Address	80000C0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_3
Address	80000C0E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P0_DP18_3_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_3
Address	80000C0F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P0_DP18_3_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_3
Address	80000C100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P0_DP18_3_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_3
Address	80000C110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P0_DP18_3_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_3
Address	80000C120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_3
Address	80000C130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P0_3
Address	80000C140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_3
Address	80000C150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_3
Address	80000C170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_3
Address	80000C180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_3
Address	80000C190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P0_DP18_3_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_3
Address	80000C1A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P0_DP18_3_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P0_3
Address	80000C1B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_3
Address	80000C1C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_3
Address	80000C1D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_3_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_3_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_3_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_3
Address	80000C300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_3
Address	80000C310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_3
Address	80000C320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_3
Address	80000C330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_3
Address	80000C340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_3
Address	80000C370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P0_DP18_3_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_3
Address	80000C380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_3
Address	80000C390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_3
Address	80000C3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_3
Address	80000C3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_3
Address	80000C3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_3
Address	80000C3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_3
Address	80000C3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_3
Address	80000C3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_3
Address	80000C400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_3
Address	80000C410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_3
Address	80000C420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_3
Address	80000C430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_3
Address	80000C440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_3
Address	80000C450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_3
Address	80000C460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_3
Address	80000C470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_3
Address	80000C480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_3
Address	80000C4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_3
Address	80000C4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_3
Address	80000C4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_3
Address	80000C500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_3
Address	80000C510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_3
Address	80000C520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_3
Address	80000C530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_3
Address	80000C540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_3
Address	80000C550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_3
Address	80000C560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_3
Address	80000C570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_3
Address	80000C5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_3
Address	80000C5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_3
Address	80000C600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_3
Address	80000C610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_3
Address	80000C620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_3
Address	80000C630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_3
Address	80000C640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_3
Address	80000C650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_3
Address	80000C660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_3
Address	80000C670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_3
Address	80000C680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_3
Address	80000C690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_3
Address	80000C6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_3
Address	80000C6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_3
Address	80000C6D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_3_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_3_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3
Address	80000C6F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_3
Address	80000C700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_3_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_3_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_3
Address	80000C710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_3_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_3_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_3
Address	80000C720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P0_DP18_3_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_3
Address	80000C730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_3_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_3_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field .
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P0_3
Address	80000C740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P0_DP18_3_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_3
Address	80000C750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_3_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_3_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_3_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_3
Address	80000C760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_3
Address	80000C770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_3
Address	80000C780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_3_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_3_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_3
Address	80000C790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_3_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_3_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_3
Address	80000C7A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_3_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_3_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_3
Address	80000C7B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_3_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_3_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_3
Address	80000C7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_3
Address	80000C7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_3
Address	80000C7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_3
Address	80000D040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_3
Address	80000D050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_3
Address	80000D090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_3
Address	80000D0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_3
Address	80000D0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_3
Address	80000D130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_3
Address	80000D300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_3
Address	80000D310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_3
Address	80000D380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_3
Address	80000D390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_3
Address	80000D3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_3
Address	80000D3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_3
Address	80000D3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_3
Address	80000D3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_3
Address	80000D3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_3
Address	80000D3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_3
Address	80000D400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_3
Address	80000D410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_3
Address	80000D420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_3
Address	80000D430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_3
Address	80000D440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_3
Address	80000D450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_3
Address	80000D460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_3
Address	80000D470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_3
Address	80000D480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_3
Address	80000D4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_3
Address	80000D4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_3
Address	80000D4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_3
Address	80000D500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_3
Address	80000D510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_3
Address	80000D520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_3
Address	80000D530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_3
Address	80000D540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_3
Address	80000D550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_3
Address	80000D560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_3
Address	80000D570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_3
Address	80000D5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_3
Address	80000D5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_3
Address	80000D600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_3
Address	80000D610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_3
Address	80000D620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_3
Address	80000D630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_3
Address	80000D640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_3
Address	80000D650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_3
Address	80000D660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_3
Address	80000D670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_3
Address	80000D680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_3
Address	80000D690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_3
Address	80000D6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_3
Address	80000D6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_3
Address	80000D7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_3
Address	80000D7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_3
Address	80000D7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_3
Address	80000E040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_3
Address	80000E050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_3
Address	80000E090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_3
Address	80000E0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_3
Address	80000E0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_3
Address	80000E130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_3
Address	80000E300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 DQSClk Phase Rotator Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_3
Address	80000E310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Write Delay Value 0 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_3
Address	80000E380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_3
Address	80000E390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_3
Address	80000E3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_3
Address	80000E3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_3
Address	80000E3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_3
Address	80000E3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_3
Address	80000E3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_3
Address	80000E3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_3
Address	80000E400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_3
Address	80000E410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_3
Address	80000E420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_3
Address	80000E430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_3
Address	80000E440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_3
Address	80000E450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_3
Address	80000E460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_3
Address	80000E470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_3
Address	80000E480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_3
Address	80000E4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_3
Address	80000E4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_3
Address	80000E4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_3
Address	80000E500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_3
Address	80000E510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_3
Address	80000E520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_3
Address	80000E530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_3
Address	80000E540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_3
Address	80000E550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_3
Address	80000E560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_3
Address	80000E570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_3
Address	80000E5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_3
Address	80000E5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_3
Address	80000E600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_3
Address	80000E610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_3
Address	80000E620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_3
Address	80000E630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_3
Address	80000E640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_3
Address	80000E650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_3
Address	80000E660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_3
Address	80000E670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_3
Address	80000E680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_3
Address	80000E690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_3
Address	80000E6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_3
Address	80000E6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_3
Address	80000E7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Disable 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_3
Address	80000E7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	*DP18 Write DQ Offset Value RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_3
Address	80000E7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_3
Address	80000F040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_3
Address	80000F050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_3
Address	80000F090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_3
Address	80000F0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_3
Address	80000F0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_3
Address	80000F130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_3
Address	80000F300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_3
Address	80000F310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_3
Address	80000F380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_3
Address	80000F390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_3
Address	80000F3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_3
Address	80000F3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_3
Address	80000F3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_3
Address	80000F3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_3
Address	80000F3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_3
Address	80000F3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_3
Address	80000F400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_3
Address	80000F410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_3
Address	80000F420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_3
Address	80000F430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_3
Address	80000F440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_3
Address	80000F450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_3
Address	80000F460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_3
Address	80000F470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_3
Address	80000F480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_3
Address	80000F4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_3
Address	80000F4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_3
Address	80000F4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_3
Address	80000F500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_3
Address	80000F510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_3
Address	80000F520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_3
Address	80000F530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_3
Address	80000F540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_3
Address	80000F550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_3
Address	80000F560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_3
Address	80000F570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_3
Address	80000F5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_3
Address	80000F5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_3
Address	80000F600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_3
Address	80000F610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_3
Address	80000F620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_3
Address	80000F630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_3
Address	80000F640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_3
Address	80000F650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_3
Address	80000F660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_3
Address	80000F670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_3
Address	80000F680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_3
Address	80000F690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_3
Address	80000F6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_3
Address	80000F6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_3
Address	80000F7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_3
Address	80000F7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_3
Address	80000F7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_4
Address	800010000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE0_P0_DP18_4_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_4
Address	800010010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_HW_VALUE:
60	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P0_4
Address	800010020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DIR0_P0_DP18_4_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P0_4
Address	800010030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_4
Address	800010040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P0_4
Address	800010050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P0_4
Address	800010060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core. See for more information.
60	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core. See for more information.
61	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field . For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P0_4
Address	800010070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P0_4
Address	800010080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_4
Address	800010090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P0_4
Address	8000100A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P0_DP18_4_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P0_DP18_4_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P0_4
Address	8000100B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_4
Address	8000100C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_4
Address	8000100D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P0_4
Address	8000100E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS0_P0_DP18_4_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P0_4
Address	8000100F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS1_P0_DP18_4_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P0_4
Address	800010100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS2_P0_DP18_4_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P0_4
Address	800010110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS3_P0_DP18_4_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P0_4
Address	800010120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_4
Address	800010130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P0_4
Address	800010140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P0_4
Address	800010150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P0_4
Address	800010170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P0_4
Address	800010180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P0_4
Address	800010190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS1_P0_DP18_4_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P0_4
Address	8000101A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS2_P0_DP18_4_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P0_4
Address	8000101B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P0_4
Address	8000101C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P0_4
Address	8000101D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P0_DP18_4_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P0_DP18_4_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P0_DP18_4_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_4
Address	800010300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_4
Address	800010310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P0_4
Address	800010320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P0_4
Address	800010330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P0_4
Address	800010340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P0_4
Address	800010370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_OFFSET_P0_DP18_4_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_4
Address	800010380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_4
Address	800010390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_4
Address	8000103A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_4
Address	8000103B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_4
Address	8000103C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_4
Address	8000103D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_4
Address	8000103E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_4
Address	8000103F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_4
Address	800010400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_4
Address	800010410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_4
Address	800010420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_4
Address	800010430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_4
Address	800010440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_4
Address	800010450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_4
Address	800010460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_4
Address	800010470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_4
Address	800010480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_4
Address	8000104A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_4
Address	8000104C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_4
Address	8000104E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_4
Address	800010500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_4
Address	800010510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_4
Address	800010520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_4
Address	800010530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_4
Address	800010540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_4
Address	800010550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_4
Address	800010560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_4
Address	800010570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_4
Address	8000105C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_4
Address	8000105D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_4
Address	800010600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_4
Address	800010610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_4
Address	800010620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_4
Address	800010630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_4
Address	800010640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_4
Address	800010650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_4
Address	800010660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_4
Address	800010670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_4
Address	800010680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_4
Address	800010690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_4
Address	8000106A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_4
Address	8000106B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P0_4
Address	8000106D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_4_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_4_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4
Address	8000106F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_4
Address	800010700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P0_DP18_4_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P0_DP18_4_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_4
Address	800010710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P0_DP18_4_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P0_DP18_4_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_4
Address	800010720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DQS_TIMING_REFERENCE_P0_DP18_4_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_4
Address	800010730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P0_DP18_4_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P0_DP18_4_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field .
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P0_4
Address	800010740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_WRCLK_PR_P0_DP18_4_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P0_4
Address	800010750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P0_DP18_4_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P0_DP18_4_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P0_DP18_4_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P0_4
Address	800010760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P0_4
Address	800010770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_4
Address	800010780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P0_DP18_4_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P0_DP18_4_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_4
Address	800010790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P0_DP18_4_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P0_DP18_4_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P0_4
Address	8000107A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P0_DP18_4_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P0_DP18_4_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P0_4
Address	8000107B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P0_DP18_4_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P0_DP18_4_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_4
Address	8000107C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP0_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_4
Address	8000107D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP0_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_4
Address	8000107E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_4
Address	800011040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P0_4
Address	800011050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_4
Address	800011090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_4
Address	8000110C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_4
Address	8000110D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_4
Address	800011130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_4
Address	800011300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_4
Address	800011310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_4
Address	800011380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_4
Address	800011390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_4
Address	8000113A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_4
Address	8000113B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_4
Address	8000113C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_4
Address	8000113D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_4
Address	8000113E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_4
Address	8000113F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_4
Address	800011400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_4
Address	800011410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_4
Address	800011420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_4
Address	800011430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_4
Address	800011440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_4
Address	800011450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_4
Address	800011460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_4
Address	800011470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_4
Address	800011480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_4
Address	8000114A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_4
Address	8000114C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_4
Address	8000114E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_4
Address	800011500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_4
Address	800011510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_4
Address	800011520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_4
Address	800011530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_4
Address	800011540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_4
Address	800011550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_4
Address	800011560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_4
Address	800011570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_4
Address	8000115C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_4
Address	8000115D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_4
Address	800011600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_4
Address	800011610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_4
Address	800011620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_4
Address	800011630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_4
Address	800011640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_4
Address	800011650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_4
Address	800011660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_4
Address	800011670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_4
Address	800011680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_4
Address	800011690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_4
Address	8000116A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_4
Address	8000116B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_4
Address	8000117C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP1_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_4
Address	8000117D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP1_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_4
Address	8000117E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_4
Address	800012040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P0_4
Address	800012050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_4
Address	800012090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_4
Address	8000120C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_4
Address	8000120D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_4
Address	800012130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_4
Address	800012300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 DQSClk Phase Rotator Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_4
Address	800012310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Write Delay Value 0 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_4
Address	800012380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_4
Address	800012390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_4
Address	8000123A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_4
Address	8000123B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_4
Address	8000123C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_4
Address	8000123D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_4
Address	8000123E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_4
Address	8000123F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_4
Address	800012400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_4
Address	800012410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_4
Address	800012420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_4
Address	800012430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_4
Address	800012440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_4
Address	800012450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_4
Address	800012460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_4
Address	800012470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_4
Address	800012480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_4
Address	8000124A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_4
Address	8000124C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_4
Address	8000124E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_4
Address	800012500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_4
Address	800012510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_4
Address	800012520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_4
Address	800012530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_4
Address	800012540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_4
Address	800012550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_4
Address	800012560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_4
Address	800012570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_4
Address	8000125C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_4
Address	8000125D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_4
Address	800012600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_4
Address	800012610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_4
Address	800012620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_4
Address	800012630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_4
Address	800012640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_4
Address	800012650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_4
Address	800012660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_4
Address	800012670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_4
Address	800012680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_4
Address	800012690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_4
Address	8000126A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_4
Address	8000126B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_4
Address	8000127C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP2_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_4
Address	8000127D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP2_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_4
Address	8000127E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_4
Address	800013040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P0_4
Address	800013050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_4
Address	800013090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_4
Address	8000130C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_4
Address	8000130D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_4
Address	800013130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_4
Address	800013300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_4
Address	800013310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_4
Address	800013380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_4
Address	800013390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_4
Address	8000133A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_4
Address	8000133B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_4
Address	8000133C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_4
Address	8000133D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_4
Address	8000133E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_4
Address	8000133F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_4
Address	800013400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_4
Address	800013410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_4
Address	800013420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_4
Address	800013430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_4
Address	800013440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_4
Address	800013450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_4
Address	800013460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_4
Address	800013470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_4
Address	800013480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_4
Address	8000134A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_4
Address	8000134C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_4
Address	8000134E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_4
Address	800013500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_4
Address	800013510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_4
Address	800013520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_4
Address	800013530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_4
Address	800013540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_4
Address	800013550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_4
Address	800013560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_4
Address	800013570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_4
Address	8000135C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_4
Address	8000135D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_4
Address	800013600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_4
Address	800013610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_4
Address	800013620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_4
Address	800013630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_4
Address	800013640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_4
Address	800013650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_4
Address	800013660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_4
Address	800013670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_4
Address	800013680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_4
Address	800013690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_4
Address	8000136A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_4
Address	8000136B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_4
Address	8000137C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP3_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_4
Address	8000137D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP3_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_4
Address	8000137E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR0
Address	800040000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR0_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR0_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR0
Address	800040010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P0_ADR0
Address	800040040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P0_ADR0_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P0_ADR0_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P0_ADR0
Address	800040050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P0_ADR0_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P0_ADR0_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P0_ADR0
Address	800040060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY2_P0_ADR0_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P0_ADR0_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P0_ADR0
Address	800040070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P0_ADR0_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P0_ADR0_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 4***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P0_ADR0
Address	800040080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P0_ADR0_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P0_ADR0_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P0_ADR0
Address	800040090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P0_ADR0_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P0_ADR0_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P0_ADR0
Address	8000400A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY6_P0_ADR0_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P0_ADR0_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P0_ADR0
Address	8000400B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY7_P0_ADR0_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P0_ADR0_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR DFT Wrap Status And Control***
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR0
Address	8000400C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR0
Address	8000401A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	***ADR I/O FET Slice Enable Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR0
Address	800040200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR0
Address	800040210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0
Address	8000402A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0
Address	8000402B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR0
Address	8000402C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR0_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR0_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR1
Address	800044000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR1_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR1_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR1
Address	800044010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P0_ADR1
Address	800044040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P0_ADR1_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P0_ADR1_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P0_ADR1
Address	800044050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P0_ADR1_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P0_ADR1_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P0_ADR1
Address	800044060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY2_P0_ADR1_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P0_ADR1_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P0_ADR1
Address	800044070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P0_ADR1_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P0_ADR1_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 4***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P0_ADR1
Address	800044080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P0_ADR1_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P0_ADR1_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P0_ADR1
Address	800044090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P0_ADR1_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P0_ADR1_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P0_ADR1
Address	8000440A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY6_P0_ADR1_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P0_ADR1_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P0_ADR1
Address	8000440B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY7_P0_ADR1_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P0_ADR1_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR DFT Wrap Status And Control***
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR1
Address	8000440C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR1
Address	8000441A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	***ADR I/O FET Slice Enable Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR1
Address	800044200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR1
Address	800044210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1
Address	8000442A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1
Address	8000442B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR1
Address	8000442C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR1_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR1_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR2
Address	800048000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR2_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR2_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR2
Address	800048010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P0_ADR2
Address	800048040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P0_ADR2_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P0_ADR2_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P0_ADR2
Address	800048050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P0_ADR2_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P0_ADR2_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P0_ADR2
Address	800048060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY2_P0_ADR2_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P0_ADR2_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 3*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P0_ADR2
Address	800048070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P0_ADR2_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P0_ADR2_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P0_ADR2
Address	800048080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P0_ADR2_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P0_ADR2_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P0_ADR2
Address	800048090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P0_ADR2_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P0_ADR2_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P0_ADR2
Address	8000480A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY6_P0_ADR2_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P0_ADR2_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P0_ADR2
Address	8000480B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY7_P0_ADR2_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P0_ADR2_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR DFT Wrap Status And Control***
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR2
Address	8000480C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR2
Address	8000481A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	***ADR I/O FET Slice Enable Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR2
Address	800048200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR2
Address	800048210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2
Address	8000482A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2
Address	8000482B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR2
Address	8000482C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR2_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR2_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P0_ADR3
Address	80004C000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR3_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR3_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR3
Address	80004C010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P0_ADR3
Address	80004C040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P0_ADR3_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P0_ADR3_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P0_ADR3
Address	80004C050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P0_ADR3_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P0_ADR3_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P0_ADR3
Address	80004C060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY2_P0_ADR3_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P0_ADR3_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 3*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P0_ADR3
Address	80004C070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P0_ADR3_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P0_ADR3_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P0_ADR3
Address	80004C080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P0_ADR3_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P0_ADR3_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P0_ADR3
Address	80004C090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P0_ADR3_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P0_ADR3_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P0_ADR3
Address	80004C0A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY6_P0_ADR3_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P0_ADR3_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P0_ADR3
Address	80004C0B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY7_P0_ADR3_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P0_ADR3_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR DFT Wrap Status And Control***
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR3
Address	80004C0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR3
Address	80004C1A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	***ADR I/O FET Slice Enable Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR3
Address	80004C200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR3
Address	80004C210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3
Address	80004C2A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3
Address	80004C2B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	*ADR Power Down 2*
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P0_ADR3
Address	80004C2C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR3_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR3_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	*ADR PLL/VREG Configuration 0*
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S0
Address	800080300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***ADR PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S0
Address	800080310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S0
Address	800080320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field are asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.

Bits	SCOM	Field Mnemonic: Description
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S0
Address	800080330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	***ADR SysClk Phase Rotator Value***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S0
Address	800080340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.

Bits	SCOM	Field Mnemonic: Description
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field .
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	***ADR Output Driver Force And ATEST Control***
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S0
Address	800080350301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_FORCE_EN: Output Force Enable Bit.
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	***ADR Output Driver Force Value 0***
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S0
Address	800080360301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Output Driver Force Value 1***
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S0
Address	800080370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Slew Calibration Control***
Mnemonic	DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S0
Address	800080390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	

Bits	SCOM	Field Mnemonic: Description
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	***ADR PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S1
Address	800084300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***ADR PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S1
Address	800084310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S1
Address	800084320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field are asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S1
Address	800084330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	*ADR SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S1
Address	800084340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field .
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	*ADR Output Driver Force And ATEST Control*
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S1
Address	800084350301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_FORCE_EN: Output Force Enable Bit.
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	*ADR Output Driver Force Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S1
Address	800084360301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Output Driver Force Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S1
Address	800084370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Slew Calibration Control*
Mnemonic	DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S1
Address	800084390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	*PC DP18 PLL Lock Status*
Mnemonic	DPHY01.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P0
Address	8000C0000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:62	ROX	DDRPHY_PC_DP18_PLL_LOCK_STATUS_P0_DP18_PLL_LOCK: One bit for each DP18 in the DDR PHY Core. When the core contains less than 15 DP18s, then bits with an index value greater than NUM_DP18 - 1 are reserved. '0'b - PLL in the bit indexed DP18 is not locked. '1'b - PLL in the bit indexed DP18 is locked. When the PHY is configured in TDM Mode, this register reports the PLL Lock Status of all the DP18s in the PHY.
63	RO	constant=0b0

Register Name	*PC AD32S PLL Lock Status*
Mnemonic	DPHY01.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P0
Address	8000C0010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	ROX	DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P0_AD32S_PLL_LOCK: One bit for each ADR Support Block in the DDR PHY Core. When the core contains less than 2 AD32Ss, bits with an index value greater than NUM_AD32S-1 are reserved. '0'b - PLL in the bit indexed AD32S is not locked. '1'b - PLL in the bit indexed AD32S is locked.
50:63	RO	constant=0b00000000000000

Register Name	*PC Rank Pair 0*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR0_P0
Address	8000C0020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_PRI: Primary Rank of Rank Pair 0 When configured for a protocol that only supports a single rank system, this field must be set to 0.
51	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_PRI_V: Value in the RANK_PAIR0_PRI field is valid
52:54	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_SEC: Secondary Rank of Rank Pair 0
55	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_SEC_V: Value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_PRI: Primary Rank of Rank Pair 1
59	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_PRI_V: Value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_SEC: Secondary Rank of Rank Pair 1
63	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_SEC_V: Value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	*PC Rank Pair 1*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR1_P0
Address	8000C0030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_PRI: Primary Rank of Rank Pair 2

Bits	SCOM	Field Mnemonic: Description
51	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_PRI_V: Value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the register defined in.
52:54	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_SEC: Secondary Rank of Rank Pair 2
55	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_SEC_V: Value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_PRI: Primary Rank of Rank Pair 3
59	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_PRI_V: Value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_SEC: Secondary Rank of Rank Pair 3
63	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_SEC_V: Value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	***PC Periodic Base Counter 0***
Mnemonic	DPHY01.DDRPHY_PC_BASE_CNTR0_P0
Address	8000C0040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_BASE_CNTR0_P0_PERIODIC_BASE_CNTR0: Periodic Base Counter 0. When enabled via PERIODIC_CAL_REQ_EN , counter is free running (counts every dphy_nclk clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & '0'} from the register.

Register Name	***PC Periodic Reload Value 0***
Mnemonic	DPHY01.DDRPHY_PC_RELOAD_VALUE0_P0
Address	8000C0050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RELOAD_VALUE0_P0_PERIODIC_CAL_REQ_EN: '1'b - Enable Periodic Calibration request generation from the PHY. '0'b - Disable Periodic Calibration request generation from the PHY.
49:63	RW	DDRPHY_PC_RELOAD_VALUE0_P0_PERIODIC_RELOAD_VALUE0: Periodic Reload Value 0. This value is loaded into bits 0 through 14 of the when it rolls over. Bit 15 is always loaded with '0'b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to '1'b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	*PC Periodic Base Counter 1*
Mnemonic	DPHY01.DDRPHY_PC_BASE_CNTR1_P0
Address	8000C0060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_BASE_CNTR1_P0_PERIODIC_BASE_CNTR1: Periodic Base Counter 1. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set , it is reloaded with the value 'FFFF'h. This register enables the and the every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set , it is reloaded with the value '00FF'h. When the FAST_SIM_PER_CNTR bit is set , this register enables and the every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer*
Mnemonic	DPHY01.DDRPHY_PC_CAL_TIMER_P0
Address	8000C0070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_CAL_TIMER_P0_PERIODIC_CAL_TIMER: Periodic Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_TIMER_RELOAD_VALUE from the register. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set , this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer Reload Value*
Mnemonic	DPHY01.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0
Address	8000C0080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0_PERIODIC_TIMER_RELOAD_VALUE: Periodic Reload Value 0. This value is loaded into the when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Impedance Calibration Timer*
Mnemonic	DPHY01.DDRPHY_PC_ZCAL_TIMER_P0
Address	8000C0090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_ZCAL_TIMER_P0_PERIODIC_ZCAL_TIMER: Periodic Impedance Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the register. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set , this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Impedance Calibration Timer Reload Value*
Mnemonic	DPHY01.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0
Address	8000C00A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0_PERIODIC_TIMER_RELOAD_VALUE: Periodic Impedance Calibration Timer Reload Value. This value is loaded into the when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Calibration Configuration*
Mnemonic	DPHY01.DDRPHY_PC_PER_CAL_CONFIG_P0
Address	8000C00B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_ENA_RANK_PAIR: '1'b indicates periodic calibration is enabled '0'b indicates periodic calibration is disabled Bit 0 contains the enable bit for rank pair 0Bit 1 contains the enable bit for rank pair 1Bit 2 contains the enable bit for rank pair 2Bit 3 contains the enable bit for rank pair 3
52	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_ENA_ZCAL: Enables the periodic impedance calibration logic.
53	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SysClk with the Memory Controller Clock (dphy_nclkSysClk Alignment).
54	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ENA_PER_READ_CTR: '1'b - Enable the updating of the registers during periodic read centering. '0'b - Prevent the updating of the registers during periodic read centering.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ENA_PER_RDCLK_ALIGN: '1'b - Enable the updating of the register at the conclusion of periodic read centering on a nibble of DQ lanes. '0'b - Prevent the updating of the register at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS Alignment).
57:58	RWX	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.
59	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_FAST_SIM_PER_CNTR: This bit must be '0'b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. '1'b causes the register to roll over to '00FF'h. '0'b has no effect on the behavior of the register.
60	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_START_INIT_CAL: When this bit is written to '1'b, the DDR PHY initiates an initial calibration for all ranks enabled in the register defined in. When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_START_PER_CAL: When this bit is written to '1'b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ABORT_ON_ERR_EN: Periodic Calibration Abort on Error Enable. '1'b - Enable the detection of the pc_errn_in. '0'b - Disable the detection of the pc_errn_in.
63	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ZCAL_UPDATE_MODE: Reserved. See PC Config 0 ZCAL_NOT_CONT bit.

Register Name	***PC Configuration 0***
Mnemonic	DPHY01.DDRPHY_PC_CONFIG0_P0
Address	8000C00C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG0_P0_PROTOCOL: Values: DDR3=>0b0000 DDR4=>0b0001 RLDRAM2_CIO=>0b0010
52	RW	DDRPHY_PC_CONFIG0_P0_DATA_MUX4_1MODE: Data Multiplexer Mode 4:1 Enable. '0'b - Data Multiplexer Mode is 2:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) is two times as wide as the data and control signals (pins) on the Memory Interface (MEMINT) Interface. '1'b - Data Multiplexer Mode is 4:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to one half of the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) are four times as wide as the data and control signals (pins) on the Memory Interface (MEMINT Interface).
53	RW	DDRPHY_PC_CONFIG0_P0_SPAM_EN: '1'b - The PC only snoops read and write commands for primary ranks of each rank pair (ie reads and writes to secondary ranks are ignored). See for more information. '0'b - Split Access Mode is not enabled.
54	RW	DDRPHY_PC_CONFIG0_P0_DDR4_CMD_SIG_REDUCTION: Values: DDR3=>0b0 DDR4=>0b1

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_PC_CONFIG0_P0_SYSCLK_2X_MEMINTCLKO: Always write this bit to '0'b. This function is not supported. '0'b - The internal SysClk frequency equals the MEMINTCLKO (memory interface clock) frequency. '1'b - The internal SysClk frequency is 2* the MEMINTCLKO (memory interface clock) frequency. Support of this function requires this register to be written during the reset sequence when the PLL values are configured.
56	RW	DDRPHY_PC_CONFIG0_P0_RANK_OVERRIDE: Rank Override Mode '0'b - The DDR PHY uses the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface to determine the rank pair and hence the configuration registers for each read or write command. '1'b - The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all readwrite commands regardless of the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface. When this bit is '1'b, the following assumptionsrestrictions apply:
57:59	RW	DDRPHY_PC_CONFIG0_P0_RANK_OVERRIDE_VALUE: Rank Override Value
60	RW	DDRPHY_PC_CONFIG0_P0_LOW_LATENCY: '1'b - Force Early Read Start Mode (ERS Mode) off. '0'b - ERS Mode onoff determined by CL value. When CL = 5 or 6, ERS Mode is automatically off. Otherwise, ERS Mode is automatically on.
61	RW	
62	RW	DDRPHY_PC_CONFIG0_P0_DDR4_VLEVEL_BANK_GROUP: In DDR4: '1'b - enable Voltage Level and Bank Group Arch(DDR4 ballot 1716.23). '0'b - disable Voltage Level and Bank Group Arch. For all other protocols, this bit must be '0'b.
63	RW	DDRPHY_PC_CONFIG0_P0_ZCAL_NOT_CONT: '1'b - IO PVT values are only updated when an internal ZQ cal is requested. '0'b - IO PVT values are updated continuously.

Register Name	*PC Configuration 1*
Mnemonic	DPHY01.DDRPHY_PC_CONFIG1_P0
Address	8000C00D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG1_P0_WRITE_LATENCY_OFFSET: Write Latency Offset (WLO) is used to adjust the delay through the internal write command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipeling latches are added. This value is twos compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path. See for more details.
52:55	RW	DDRPHY_PC_CONFIG1_P0_READ_LATENCY_OFFSET: Read Latency Offset (RLO) is used to adjust the delay through the internal read command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipeling latches are added. This value is two's compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path. The value for this field must be: RLO less than equal min{RoundDown(System_Delay)} System_Delay and min{RoundDown(System_Delay)} is defined in the GLOBAL_PHY_OFFSET field description .
56	RW	DDRPHY_PC_CONFIG1_P0_MEMCTL_CIC_FAST: '0'b - memctl_cic_o is deasserted ('0'b) in response to memctl_cis_i being asserted ('1'b) and remains deasserted until the calibration completes. '1'b - memctl_cic_o is deasserted ('0'b) in response to memctl_cis_i being asserted ('1'b) and is asserted ('1'b) in response to memctl_cis_i being deasserted ('0'b).
57	RW	DDRPHY_PC_CONFIG1_P0_MEMCTL_CTRN_IGNORE: '0'b - DDR PHY responds to the memctl_ctrn_i input. '1'b - DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a 'don't care'.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_PC_CONFIG1_P0_DISABLE_MEMCTL_CAL: Reserved. This bit must be '0'b. When set to '1'b, the DFI request ack handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.
59:61	RW	DDRPHY_PC_CONFIG1_P0_MEMORY_TYPE: '001'b - DDR3 RDIMM '011'b - DDR3 LRDIMM '101'b - DDR4 RDIMM '111'b - DDR4 LRDIMM Other values are reserved.
62	RW	DDRPHY_PC_CONFIG1_P0_DDR4_LATENCY_SW: DDR4 Latency Debug Switch. Should be '1'b for normal operation.
63	RW	DDRPHY_PC_CONFIG1_P0_RETRAIN_PERCAL_SW: Retrain Percal Debug Switch. Affects behavior of memctl_cup_o during periodic read calibrations. '0'b - rank is requested rank and may not be the rank that was executed. '1'b - rank is next rank that requires calibration.

Register Name	***PC Resets***
Mnemonic	DPHY01.DDRPHY_PC_RESETS_P0
Address	8000C00E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RESETS_P0_PLL_RESET: '1'b - Resets the Internal PLLs
49	RW	DDRPHY_PC_RESETS_P0_SYSCLK_RESET: '1'b - Reset all logic in the internal sysclk domain.
50:63	RO	constant=0b00000000000000

Register Name	***PC Periodic Z-Cal Configuration***
Mnemonic	DPHY01.DDRPHY_PC_PER_ZCAL_CONFIG_P0
Address	8000C00F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P0_PER_ZCAL_ENA_RANK: '1'b indicates periodic external impedance calibration is enabled '0'b indicates periodic external impedance calibration is disabled Bit 0 contains the enable bit for rank 0Bit 1 contains the enable bit for rank 1Bit 2 contains the enable bit for rank 2Bit 3 contains the enable bit for rank 3Bit 4 contains the enable bit for rank 4Bit 5 contains the enable bit for rank 5Bit 6 contains the enable bit for rank 6Bit 7 contains the enable bit for rank 7
56:58	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P0_PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 next rank scheduled to run z cal001 = rank_1 next rank scheduled to run z cal010 = rank_2 next rank scheduled to run z cal011 = rank_3 next rank scheduled to run z cal100 = rank_4 next rank scheduled to run z cal101 = rank_5 next rank scheduled to run z cal110 = rank_6 next rank scheduled to run z cal111 = rank_7 next rank scheduled to run z cal
59	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P0_START_PER_ZCAL: When this bit is written to '1'b, the DDR PHY initiate a single periodic impedance calibration (equivalent to a periodic z cal timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	constant=0b0000

Register Name	***PC Power Down 1***
Mnemonic	DPHY01.DDRPHY_PC_POWERDOWN_1_P0
Address	8000C0100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_POWERDOWN_1_P0_MASTER_PD_CNTL: Master Powerdown Control '0'b - DDR port is in functional mode regardless of PDR1 bits {1:15} '1'b - Powerdown status of DDR port is determined by PDR bits {1:15}
49	RW	DDRPHY_PC_POWERDOWN_1_P0_ANALOG_INPUT_STAB2: Analog Input Stabilization #2 (Separate from bit 7 to allow for separation of behavior in PDS3) '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
50	RW	DDRPHY_PC_POWERDOWN_1_P0_EYEDAC_PD: EYEDAC powerdown '0'b - EYEDAC controlled by functional mode register '1'b - EYEDAC powered down
51	RW	DDRPHY_PC_POWERDOWN_1_P0_PHYTOP_CLK_GATE: Reserved.
52	RW	DDRPHY_PC_POWERDOWN_1_P0_EXT_VREF_PD: External VREF Powerdown '0'b - Functional Mode control of External VREF Drivers '1'b - External VREF Drivers Powered Down
53	RW	DDRPHY_PC_POWERDOWN_1_P0_RESET_STAB: RESET# Stabilization '0'b - Functional Mode Control of RESET# PHY IO '1'b - Powerdown Stabilization of RESET# Signals
54	RW	DDRPHY_PC_POWERDOWN_1_P0_ANALOG_OUTPUT_STAB: Analog Output Stabilization '0'b - Functional Mode Control of Analog Outputs '1'b - Analog Outputs Forced to Known Values Immediately on Digital Side of Boundary
55	RW	DDRPHY_PC_POWERDOWN_1_P0_ANALOG_INPUT_STAB1: Analog Input Stabilization #1 '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
56	RW	DDRPHY_PC_POWERDOWN_1_P0_SYSCLK_CLK_GATE: Reserved.
57	RW	DDRPHY_PC_POWERDOWN_1_P0_DELAY_LINE_CTL_OVERRIDE: '0'b - DP18 Delay Line Power Control register is read only and is updated by hardware. '1'b - DP18 Delay Line Power Control register is read/write and is not updated by hardware.
58	RW	DDRPHY_PC_POWERDOWN_1_P0_WR_FIFO_STAB: Write FIFO & Logic Circuit Stabilization '0'b - Write FIFO and Logic Circuits under Functional Control '1'b - Write FIFO clock disabled, Flush mode set
59	RW	DDRPHY_PC_POWERDOWN_1_P0_ADR_RX_PD: Reserved.
60:61	RW	DDRPHY_PC_POWERDOWN_1_P0_DP18_RX_PD: DP18 Receiver Powerdown Control '00'b - Functional Mode Control of DP Receivers '01'b - DP Receivers in Standby Mode (RG) '10'b - Reserved. '11'b - DP Receivers in Low Power Mode (RE)
62	RW	DDRPHY_PC_POWERDOWN_1_P0_TX_TRISTATE_CNTL: Driver Tristate Control '0'b - Functional Mode Control of Drivers '1'b - DP18 Drivers in Tristate, ADR Drivers selectively either in Tristate or Pulldown under control of PDR2 For the ADR12 and ADR16 cores, this bit operates in conjunction with the register to determine the state of the IO during powerdown.
63	RW	DDRPHY_PC_POWERDOWN_1_P0_VCC_REG_PD: VCC Domain Regulation Powerdown '0'b - Functional Mode: VCC Voltage Regulators are on '1'b - Powerdown Mode: Voltage Regulators powered down, VCC=0v

Register Name	*PC Rank Group*
Mnemonic	DPHY01.DDRPHY_PC_RANK_GROUP_P0
Address	8000C0110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP0_PRI: '1'b - Enable Address Mirroring Rank Pair 0 Primary
49	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP0_SEC: '1'b - Enable Address Mirroring Rank Pair 0 Secondary
50	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP1_PRI: '1'b - Enable Address Mirroring Rank Pair 1 Primary
51	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP1_SEC: '1'b - Enable Address Mirroring Rank Pair 1 Secondary
52	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP2_PRI: '1'b - Enable Address Mirroring Rank Pair 2 Primary
53	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP2_SEC: '1'b - Enable Address Mirroring Rank Pair 2 Secondary
54	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP3_PRI: '1'b - Enable Address Mirroring Rank Pair 3 Primary
55	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP3_SEC: '1'b - Enable Address Mirroring Rank Pair 3 Secondary
56:57	RW	DDRPHY_PC_RANK_GROUP_P0_RANK_GROUPING: Reserved.
58	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A3_A4: '1'b - mirror A3 & A4 signals on mirrored ranks.
59	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A5_A6: '1'b - mirror A5 & A6 signals on mirrored ranks.
60	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A7_A8: '1'b - mirror A7 & A8 signals on mirrored ranks.
61	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A11_A13: '1'b - mirror A11 & A13 signals on mirrored ranks.
62	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_BA0_BA1: '1'b - mirror BA0 & BA1 signals on mirrored ranks.
63	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_BG0_BG1: '1'b - mirror BG0 & BG1 signals on mirrored ranks.

Register Name	*PC Error Status 0*
Mnemonic	DPHY01.DDRPHY_PC_ERROR_STATUS0_P0
Address	8000C0120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_ERROR_STATUS0_P0_RC_ERROR: '1'b - Error in Read Control logic.

Bits	SCOM	Field Mnemonic: Description
49	ROX	DDRPHY_PC_ERROR_STATUS0_P0_WC_ERROR: '1'b - Error in Write Control logic.
50	ROX	DDRPHY_PC_ERROR_STATUS0_P0_SEQ_ERROR: '1'b - Error in Sequencer Control logic.
51	ROX	DDRPHY_PC_ERROR_STATUS0_P0_CC_ERROR: Reserved.
52	ROX	DDRPHY_PC_ERROR_STATUS0_P0_APB_ERROR: '1'b - Error in Register interface logic.
53	ROX	DDRPHY_PC_ERROR_STATUS0_P0_PC_ERROR: '1'b - Error in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	***PC Error Mask 0***
Mnemonic	DPHY01.DDRPHY_PC_ERROR_MASK0_P0
Address	8000C0130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_ERROR_MASK0_P0_RC_ERROR_MASK: '1'b - Mask errors in Read Control logic.
49	RW	DDRPHY_PC_ERROR_MASK0_P0_WC_ERROR_MASK: '1'b - Mask errors in Write Control logic.
50	RW	DDRPHY_PC_ERROR_MASK0_P0_SEQ_ERROR_MASK: '1'b - Mask errors in Sequencer Control logic.
51	RW	DDRPHY_PC_ERROR_MASK0_P0_CC_ERROR_MASK: Reserved.
52	RW	DDRPHY_PC_ERROR_MASK0_P0_APB_ERROR_MASK: '1'b - Mask errors in Register Interface logic.
53	RW	DDRPHY_PC_ERROR_MASK0_P0_PC_ERROR_MASK: '1'b - Mask errors in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	***PC IO PVT N/P FET Driver Control***
Mnemonic	DPHY01.DDRPHY_PC_IO_PVT_FET_CONTROL_P0
Address	8000C0140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_PVTP: PFET Driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
53:57	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_PVTN: NFET Driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
58	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_PVT_OVERRIDE: '1'b - All drivers are updated with the PVTP and PVTN values in this register immediately. '0'b - All drivers are updated with the PVTP and PVTN values from the impedance calibration state machine.
59	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_ENABLE_ZCAL: '1'b - Enable Impedance Controller. '0'b - Disable Impedance Controller.
60	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_RESET_ZCAL: Reset Impedance Controller. The value of this field is driven to the zcntl_reset_o output for optional connection to the reset of an Impedance Controller.

Bits	SCOM	Field Mnemonic: Description
61:63	RO	constant=0b000

Register Name	*PC VREF Driver Control*
Mnemonic	DPHY01.DDRPHY_PC_VREF_DRV_CONTROL_P0
Address	8000C0150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ0DSGN: VREF sign bit enable. This value is driven to the vrefdq0_dsign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
49:52	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ0D: VREF bit enables. This value is driven to the vrefdq0_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
53	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ1DSGN: VREF sign bit enable. This value is driven to the vrefdq1_dsign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
54:57	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ1D: VREF bit enables. This value is driven to the vrefdq1_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
58:63	RO	constant=0b000000

Register Name	*PC Initial Calibration Config0*
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_CONFIG0_P0
Address	8000C0160301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_WR_LEVEL: Enable Write Levelling during initial calibration
49	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_INITIAL_PAT_WR: Enable Initial Pattern Write during initial calibration. This bit must be set when performing Read Centering or Write Centering on memory devices that do not generate an MPR pattern. This bit must be set when performing Custom Read Centering or Custom Write Centering. If Custom Read Centering or Custom Write Centering was performed, an Initial Pattern Write of '5555' hex, the reset value of the SEQ Read/Write Data0-1 registers, must be performed before any periodic calibration routines are performed.
50	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_RDCLK_ALIGN: Enable the alignment of the internal SysClk to the Read clock during initial calibration. This calibration step requires the DQS (read) Alignment calibration step to have been performed.
52	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_READ_CTR: Enable Read Centering during initial calibration. This calibration step requires the SysClk to Read Clock alignment to have been performed.
53	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_WRITE_CTR: Enable Write Centering during initial calibration. This calibration step requires the Read Centering calibration step to have been performed.

Bits	SCOM	Field Mnemonic: Description
54	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_INITIAL_COARSE_WR: Enable Initial Coarse Pattern Write during initial calibration. This calibration step requires the Write Centering calibration step to have been performed.
55	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_COARSE_RD: Enable Coarse Read Centering during initial calibration. This calibration step requires the Initial Coarse Pattern Write calibration step to have been performed.
56	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0, 2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation
57	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0,2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation.
58	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes.
59	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_RANK_PAIR: Enable Rank Pair ('1'b = Enabled, '0'b = disabled) Bit 12 contains the enable for rank pair 0.Bit 13 contains the enable for rank pair 1.Bit 14 contains the enable for rank pair 2.Bit 15 contains the enable for rank pair 3.

Register Name	***PC Initial Calibration Config1***
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_CONFIG1_P0
Address	8000C0170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_COUNT: Refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: '00'b: Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. '01'b: Use the internal Refresh Interval timer to determine when refresh commands are sent; allow refreshes to occur between calibration routines. '10'b: Reserved '11'b: Use the internal Refresh Interval timer to determine when refresh commands should be sent; in addition to allowing refreshes commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_ALL_RANKS: '1'b Indicates that all ranks should be refreshed during initial calibration. When a refresh is generated by the DDR PHY all of the chip selects are asserted at the same time during one refresh command. '0'b indicates only the rank currently being calibrated should be refreshed. When a refresh is generated by the DDR PHY, only the chip select of the rank being calibrated are asserted during the refresh command.
55:56	RW	

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_INTERVAL: Refresh Interval - This value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (min. value) = 256 MEMINTCLKO cycles between refreshes 1111111 (max value) = 32512 MEMINTCLKO cycle between refreshes For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 ('0011000'b) provides a tREFI setting of 7.68 us (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 us).The minimum value for this field is 6. If a value less than 6 is written to this field, this field will be set to 6 by hardware. When the Refresh Interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes will be issued and the internal counter will be decremented to zero. The internal pending refresh counter is a 4 bit counter with a maximum value of '15'd. An error bit will be set in the register if the internal pending refresh counter overflows.

Register Name	***PC Initial Calibration Error***
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_ERROR_P0
Address	8000C0180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_WR_LEVEL: Write leveling error occurred during initial calibration.
49	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_INITIAL_PAT_WRITE: Initial Pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
50	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_DQS_ALIGN: DQS Alignment error occurred during initial calibration.
51	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_RDCLK_ALIGN: RDCLK to SysClk alignment error occurred during initial calibration.
52	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_READ_CTR: Read centering error occurred during initial calibration.
53	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_WRITE_CTR: Write centering error occurred during initial calibration.
54	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_INITIAL_COARSE_WR: Initial Coarse Pattern Write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
55	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_COARSE_RD: Coarse read centering error occurred during initial calibration.
56	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_CUSTOM_RD: Custom pattern read centering error occurred during initial calibration.
57	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_CUSTOM_WR: Custom pattern write centering error occurred during initial calibration.
58	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_DIGITAL_EYE: Digital eye error occurred during initial calibration.
59	RO	constant=0b0
60:63	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 12 reflects the status of rank pair 0.Bit 13 reflects the status of rank pair 1.Bit 14 reflects the status of rank pair 2.Bit 15 reflects the status of rank pair 3.

Register Name	*PC Initial Calibration Status*
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_STATUS_P0
Address	8000C0190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	ROX	DDRPHY_PC_INIT_CAL_STATUS_P0_INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration, '1'b indicates the rank pair has completed an initial calibration sequence. bit 0 reflects the status of rank pair 0bit 1 reflects the status of rank pair 1bit 2 reflects the status of rank pair 2bit 3 reflects the status of rank pair 3
52:56	ROX	
57	ROX	DDRPHY_PC_INIT_CAL_STATUS_P0_PER_CAL_ABORT: Reserved. This reserved field might contain information that is helpful for hardware debugging. Do not assume that it is read as zerosPeriodic Calibration Abort. Read Only. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress and the ABORT_ON_ERR_EN bit is set . This bit is reset at the start of every new calibration.
58:63	ROX	

Register Name	*PC Initial Calibration Mask*
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_MASK_P0
Address	8000C01A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_WR_LEVEL_MASK: Mask Write leveling error
49	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_INITIAL_PAT_WRITE_MASK: Mask Initial Pattern write error
50	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_DQS_ALIGN_MASK: Mask DQS Alignment error
51	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_RDCLK_ALIGN_MASK: Mask RDCLK to SysClk alignment error
52	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_READ_CTR_MASK: Mask Read centering error
53	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_WRITE_CTR_MASK: Mask Write centering error
54	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_INITIAL_COARSE_WR_MASK: Mask Initial Coarse Pattern Write centering error
55	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_COARSE_RD_MASK: Mask Coarse read centering error
56	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_CUSTOM_RD_MASK: Mask Custom pattern read centering error
57	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_CUSTOM_WR_MASK: Mask Custom pattern write centering error
58	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_DIGITAL_EYE_MASK: Mask Digital Eye error
59:63	RO	constant=0b00000

Register Name	*PC IO PVT N/P FET Driver Status*
Mnemonic	DPHY01.DDRPHY_PC_IO_PVT_FET_STATUS_P0
Address	8000C01B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P0_PVTP: PFET Driver PVTP value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.
53:57	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P0_PVTN: NFET Driver PVTN value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.
58:63	RO	constant=0b000000

Register Name	*PC Mode 0 Primary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP0_P0
Address	8000C01C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP0_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP0_P0
Address	8000C01D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP0_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP0_P0
Address	8000C01E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_PC_MR2_PRI_RP0_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	***PC Mode 3 Primary RP0***
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP0_P0
Address	8000C01F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP0_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	***PC Mode 0 Secondary RP0***
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP0_P0
Address	8000C0200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP0_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP0***
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP0_P0
Address	8000C0210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP0_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and.The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP0_P0
Address	8000C0220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP0_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP0_P0
Address	8000C0230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP0_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Rank Pair 2*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR2_P0
Address	8000C0300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_TER: Tertiary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_TER_V: Value in the RANK_PAIR0_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_QUA: Quaternary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_QUA_V: Value in the RANK_PAIR0_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_TER: Tertiary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_TER_V: Value in the RANK_PAIR1_TER field is valid.

Bits	SCOM	Field Mnemonic: Description
60:62	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_QUA: Quaternary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_QUA_V: Value in the RANK_PAIR1_QUA field is valid.

Register Name	*PC Rank Pair 3*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR3_P0
Address	8000C0310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_TER: Tertiary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_TER_V: Value in the RANK_PAIR2_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_QUA: Quaternary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_QUA_V: Value in the RANK_PAIR2_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_TER: Tertiary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_TER_V: Value in the RANK_PAIR3_TER field is valid.
60:62	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_QUA: Quaternary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_QUA_V: Value in the RANK_PAIR3_QUA field is valid.

Register Name	*PC Chip Select ID Configuration*
Mnemonic	DPHY01.DDRPHY_PC_CSID_CFG_P0
Address	8000C0330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_CSID_CFG_P0_CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair registers, then CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
49	RW	DDRPHY_PC_CSID_CFG_P0_CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair registers, then CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
50	RW	DDRPHY_PC_CSID_CFG_P0_CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair registers, then CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
51	RW	DDRPHY_PC_CSID_CFG_P0_CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair registers, then CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_PC_CSID_CFG_P0_CS4_INIT_CAL_VALUE: If CS4 is not selected by any of the Rank Pair registers, then CS4 is driven to this value during initial calibration. If CS4 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
53	RW	DDRPHY_PC_CSID_CFG_P0_CS5_INIT_CAL_VALUE: If CS5 is not selected by any of the Rank Pair registers, then CS5 is driven to this value during initial calibration. If CS5 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
54	RW	DDRPHY_PC_CSID_CFG_P0_CS6_INIT_CAL_VALUE: If CS6 is not selected by any of the Rank Pair registers, then CS6 is driven to this value during initial calibration. If CS6 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
55	RW	DDRPHY_PC_CSID_CFG_P0_CS7_INIT_CAL_VALUE: If CS7 is not selected by any of the Rank Pair registers, then CS7 is driven to this value during initial calibration. If CS7 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
56:63	RO	constant=0b00000000

Register Name	***PC Rank Group Extension***
Mnemonic	DPHY01.DDRPHY_PC_RANK_GROUP_EXT_P0
Address	8000C0350301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP0_TER: '1'b - Enable Address Mirroring Rank Pair 0 Tertiary
49	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP0_QUA: '1'b - Enable Address Mirroring Rank Pair 0 Quaternary
50	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP1_TER: '1'b - Enable Address Mirroring Rank Pair 1 Tertiary
51	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP1_QUA: '1'b - Enable Address Mirroring Rank Pair 1 Quaternary
52	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP2_TER: '1'b - Enable Address Mirroring Rank Pair 2 Tertiary
53	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP2_QUA: '1'b - Enable Address Mirroring Rank Pair 2 Quaternary
54	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP3_TER: '1'b - Enable Address Mirroring Rank Pair 3 Tertiary
55	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP3_QUA: '1'b - Enable Address Mirroring Rank Pair 3 Quaternary
56:63	RO	constant=0b00000000

Register Name	***PC Mode 0 Primary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP1_P0
Address	8000C11C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP1_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP1_P0
Address	8000C11D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP1_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP1_P0
Address	8000C11E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP1_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP1_P0
Address	8000C11F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP1_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP1_P0
Address	8000C1200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP1_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP1_P0
Address	8000C1210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP1_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and.The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP1_P0
Address	8000C1220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP1_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP1_P0
Address	8000C1230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP1_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP2_P0
Address	8000C21C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP2_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP2_P0
Address	8000C21D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP2_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP2_P0
Address	8000C21E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP2_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP2_P0
Address	8000C21F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP2_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP2_P0
Address	8000C2200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP2_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP2_P0
Address	8000C2210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP2_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and.The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP2_P0
Address	8000C2220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP2_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP2_P0
Address	8000C2230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP2_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP3_P0
Address	8000C31C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP3_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP3_P0
Address	8000C31D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP3_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP3_P0
Address	8000C31E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP3_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP3_P0
Address	8000C31F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP3_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP3_P0
Address	8000C3200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP3_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP3***
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP3_P0
Address	8000C3210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP3_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and.The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP3***
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP3_P0
Address	8000C3220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP3_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP3***
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP3_P0
Address	8000C3230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP3_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	***SEQ Read/Write Data 0***
Mnemonic	DPHY01.DDRPHY_SEQ_RD_WR_DATA0_P0
Address	8000C4000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA0_P0_RD_WR_DATA_REG0: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0are written to MPR0. - bits 8:15 of register 0 are written to MPR1. - bits 0:7 of register 1 are written to MPR2. - bits 8:15 of register 1 are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	***SEQ Read/Write Data 1***
Mnemonic	DPHY01.DDRPHY_SEQ_RD_WR_DATA1_P0
Address	8000C4010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA1_P0_RD_WR_DATA_REG1: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0are written to MPR0. - bits 8:15 of register 0 are written to MPR1. - bits 0:7 of register 1 are written to MPR2. - bits 8:15 of register 1 are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	*SEQ Configuration 0*
Mnemonic	DPHY01.DDRPHY_SEQ_CONFIG0_P0
Address	8000C4020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_CONFIG0_P0_MPR_PATTERN_BIT: Read and write calibration algorithms are based on eight-beat bursts. This register controls the readwrite burst data pattern. For Write data: The MPR_PATTERN_BIT value is available on all bit lanes of beat 1, 3, 5 and 7 and the inverse of the MPR_PATTERN_BIT on all bit lanes of beat 2, 3, 6 and 8, ensuring all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For Read data: Bit 0 is brought out as output of Sequencer and DP18 composes the expected pattern from this output.
49	RW	DDRPHY_SEQ_CONFIG0_P0_TWO_CYCLE_ADDR_EN: DDR3 and DDR4: '1'b - During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles while the appropriate chip selects are active only during the second memory clock cycle of the command. '0'b - During calibration, the address and command and chip selects are driven and active for one memory clock cycle. All other protocols: This bit must be set to '0'b. The address and command and chip selects are driven active for one memory clock cycle.
50:53	RW	DDRPHY_SEQ_CONFIG0_P0_MR_MASK_EN: Mode Register mask enable. This register masks, or disables, the mode register access by the calibration algorithms. Bits 0- 3 map to mode register 0 - 3.
54	RW	DDRPHY_SEQ_CONFIG0_P0_DELAYED_PAR: '0'b - DDR4 PAR signal is generated coincident with addresscommand signals during init cal '1'b - DDR4 PAR signal is generated one clock cycle later than addresscommand signals during init cal Bit applies to DDR4 only and is don't care for DDR3
55	RW	DDRPHY_SEQ_CONFIG0_P0_LRDIMM_CONTEXT: Value of context bit to be used during F[0]RC12 LRDIMM Control Word commands.
56	RW	DDRPHY_SEQ_CONFIG0_P0_FORCE_RESERVED: '0'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will use the DDR4 MPR registers. '1'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory. If the PROTOCOL field does not equal DDR4, this bit is not used and is a 'don't care'.
57	RW	DDRPHY_SEQ_CONFIG0_P0_HALT_ROTATION: '0'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will rotate through the use of all 4 MPR registers by changing BA[0:1] during the calibration. '1'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will set BA[0:1] = '00'b. The same 8 beats will be read repeatedly on a particular DQ lane and the expect data will not be rotated through the 4 bytes of the register every 8 beats. If the PROTOCOL field does not equal DDR4, this bit is not used and is a 'don't care'.
58	RW	DDRPHY_SEQ_CONFIG0_P0_FORCE_MPR: '0'b - When the PROTOCOL field equals DDR3, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory, allowing a custom 8 bit repeating pattern to be compared during read centering. '1'b - When the PROTOCOL field equals DDR3, Custom Read Centering and Initial Pattern Write will use 4 DRAM MPR registers, allowing Custom Read Centering to read the 4 MPR registers. This is not a mode described by the DDR3 JEDEC standard. If the PROTOCOL field does not equal DDR3, this bit is not used and is a 'don't care'.
59:63	RW	

Register Name	*SEQ Reserved Address 0*
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR0_P0
Address	8000C4030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR0_P0_RESERVED_ADDR0: Reserved Address Field 0. Exact definition is protocol dependant. DDR3DDR4: Bits 0-15 map to A0-A15. The lower 2 bytes of row address are used. RLDRAM2RLDRAM3: Bits 0-15 map to A0-A15. Lower 2 bytes of the row and column address are used.

Register Name	***SEQ Reserved Address 1***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR1_P0
Address	8000C4040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR1_P0_RESERVED_ADDR1: Reserved Address Field 1. The exact definition is protocol dependant. For DDR3: bits 0 - 15 are reserved. For DDR4: Bits 0 - 4 map to A16 - A20; bits 5 - 15 are reserved. This protocol uses the upper bit of the row address. For RLDRAM2 and RLDRAM3: Bits 0 - 6 map to A16 - A22; bits 7 - 15 are reserved. This protocol uses the upper bits of the row and column address.

Register Name	***SEQ Reserved Address 2***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR2_P0
Address	8000C4050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR2_P0_RESERVED_ADDR2: Reserved Address Field 2. This register controls the lower 2 bytes of the column address. Exact definition is protocol and command dependant. Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION . DDR3 writes with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR3 reads with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 writes with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '1'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR4 reads with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '0'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 Refresh: A11:A15 = bits 11:15 A10 (AP) = '1'b A0:A9 = bits 0:9 DDR3 Refresh: A0:A15 = bits 0:15

Register Name	***SEQ Reserved Address 3***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR3_P0
Address	8000C4060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR3_P0_RESERVED_ADDR3: Reserved Address Field 3. The exact definition is protocol dependant. For DDR3DDR4RLDRAM2RLDRAM3: bits 0-15 are reserved

Register Name	*SEQ Reserved Address 4*
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR4_P0
Address	8000C4070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR4_P0_RESERVED_ADDR4: Reserved Address Field 4. Bank Address. The exact definition is protocol dependant. For DDR3RLDRAM2: Bits 0 - 2 map to BA0-BA2. Bits 3 - 15 are reserved. For DDR4: Bits 0 - 1 map to BA0-BA1 and bits 2 - 3 map to BG0 - BG1. Bits 4 - 15 are reserved. MPR Reads performed by the internal calibration routines: BA0-BA1 are forced to '00'b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0-BA1 addressed used/reserved). For RLDRAM2: Bits 0 - 2 map to BA0 - BA2. Bits 3 - 15 are reserved. For RLDRAM3: Bits 0 - 3 map to BA0 - BA3. Bits 4 - 15 are reserved.

Register Name	*SEQ Error Status 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ERROR_STATUS0_P0
Address	8000C4080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_MULTIPLE_REQ_ERROR: '1'b - Error: Multiple requests received at same time.
49	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_INVALID_REQTYPE_ERROR: '1'b - Error: In the current state, this request is not expected.
50	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_EARLY_REQ_ERROR: '1'b - Error: A new request arrived before acknowledge of previous request.
51:53	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 3:5 = {PC_REQ, RC_REQ, WC_REQ}
54:57	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register. See functional description section of Sequence generator for request types from each source.
58:60	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 10:12 = {PC_REQ, RC_REQ, WC_REQ}
61:63	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 13:15 = {PC_REQ, RC_REQ, WC_REQ}

Register Name	*SEQ Error Mask 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ERROR_MASK0_P0
Address	8000C4090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ERROR_MASK0_P0_MULT_REQ_ERR_MASK: '1'b - Prevent the MULTIPLE_REQ_ERROR bit from being set in the register. '0'b - Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	DDRPHY_SEQ_ERROR_MASK0_P0_INVALID_REQTYPE_ERR_MASK: '1'b - Prevent the INVALID_REQTYPE_ERROR bit from being set in the register. '0'b - Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	DDRPHY_SEQ_ERROR_MASK0_P0_EARLY_REQ_ERR_MASK: '1'b - Prevent the EARLY_REQ_ERROR bit from being set in the register. '0'b - Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	

Register Name	*SEQ ODT Write Configuration 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG0_P0
Address	8000C40A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P0_ODT_WR_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P0_ODT_WR_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Write Configuration 1*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG1_P0
Address	8000C40B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P0_ODT_WR_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P0_ODT_WR_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Write Configuration 2*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG2_P0
Address	8000C40C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P0_ODT_WR_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P0_ODT_WR_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Write Configuration 3*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG3_P0
Address	8000C40D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P0_ODT_WR_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P0_ODT_WR_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG0_P0
Address	8000C40E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P0_ODT_RD_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P0_ODT_RD_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 1*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG1_P0
Address	8000C40F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P0_ODT_RD_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P0_ODT_RD_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 2*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG2_P0
Address	8000C4100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P0_ODT_RD_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P0_ODT_RD_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 3*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG3_P0
Address	8000C4110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P0_ODT_RD_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P0_ODT_RD_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ Memory Timing Parameter 0*
Mnemonic	DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM0_P0
Address	8000C4120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TMOD_CYCLES: For DDR3 and DDR4: max(tMRD, tMOD) For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TRCD_CYCLES: For DDR3 and DDR4: tRCD For RLD2 and RLD3: reserved
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TRP_CYCLES: For DDR3 and DDR4 tRP For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TRFC_CYCLES: For DDR3 and DDR4: tRFC For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 1*
Mnemonic	DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM1_P0
Address	8000C4130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TZQINIT_CYCLES: For DDR3, DDR4, RLD2, and RLD3: max(tZQINIT,tZQOPER)
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TZQCS_CYCLES: For DDR3, DDR4, RLD2, and RLD3: tZQCS
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TWLDQSEN_CYCLES: For DDR3 and DDR4: tWLDQSEN For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TWRMRD_CYCLES: For DDR3 and DDR4: tWLMRD For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 2*
Mnemonic	DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM2_P0
Address	8000C4140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P0_TODTLON_OFF_CYCLES: For DDR3 and DDR4: max(ODTLon, ODTLoff) When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES ^ 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change or a change from read ODT values to write ODT values, or because an MRS command is issued. See sections and for more information. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window and waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued and the DDR PHY waits for tMOD cycles and then restores the ODT pins to their prior state. For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P0_TRC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tRC
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P0_TMRSC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tMRSC
60:63	RW	

Register Name	*SEQ Low Power Termination Address 2*
Mnemonic	DPHY01.DDRPHY_SEQ_LPT_ADDR2_P0
Address	8000C4170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR2_P0_LPT_ADDR2: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	*SEQ Low Power Termination Address 3*
Mnemonic	DPHY01.DDRPHY_SEQ_LPT_ADDR3_P0
Address	8000C4180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_SEQ_LPT_ADDR3_P0_LPT_ADDR3: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ Low Power Termination Address 4***
Mnemonic	DPHY01.DDRPHY_SEQ_LPT_ADDR4_P0
Address	8000C4190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR4_P0_LPT_ADDR4: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ ZQCal Encoded Rank Control 0***
Mnemonic	DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0
Address	8000C41A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ZQCal Encoded Rank Control 1***
Mnemonic	DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0
Address	8000C41B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ODT Default Configuration***
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_DEFAULT_CFG_P0
Address	8000C4240301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_DEFAULT_CFG_P0_ODT_DEF_VALUES: The eight ODT values in this register are driven to the ODT pins during MRS commands. Typically the PDT value should be set to 0 during MRS commands. However if the ODT is an ODTCID function pin, then the corresponding bit in this register should be set to the desired CID value, and the corresponding bits in the ODT Write and Read Configuration registers should be set to similar values. Where: bit 0 - ODT value for ODT pin 0 during MRS command bit 1 - ODT value for ODT pin 1 during MRS command bit 2 - ODT value for ODT pin 2 during MRS command ... bit 7 - ODT value for ODT pin 7 during MRS command
56:63	RW	

Register Name	***RC Configuration 0***
Mnemonic	DPHY01.DDRPHY_RC_CONFIG0_P0
Address	8000C8000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_RC_CONFIG0_P0_GLOBAL_PHY_OFFSET: Global PHY Offset, GPO. This field is the number of memory clock cycles added to the total read latency in the PHY. See for more details. Minimum Value: When ADVANCE_RD_VALID = '0'b, the minimum value for this field is 5 + max{RoundUp(System_Delay)} - RLO. When ADVANCE_RD_VALID = '1'b, the minimum value for this field is 6 + max{RoundUp(System_Delay)} - RLO. When SPAM_EN = '1'b , the minimum value calculated for this field is increased by 1. Where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1128th of a MEMINTCLKO clock cycle}) 128) + {number of pipeline stages in the addrcmd path} + {number of pipeline stages in the read data path} max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. RLO is the READ_LATENCY_OFFSET field . Maximum Value: In 2:1 mode, the maximum value for this field is 'B'h. In 4:1 mode, the maximum value for this field is 'D'h.
52	RW	DDRPHY_RC_CONFIG0_P0_ADVANCE_RD_VALID: Number of MEMCTLCLKI clock cycles MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted before the associated read data. '0'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted during the same MEMCTLCLKI clock cycle the associated read data is valid. '1'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted one MEMCTLCLKI clock cycle before the associated read data is valid. In 4:1 Data Multiplexer mode, this field must be '0'b.
53	RW	DDRPHY_RC_CONFIG0_P0_PER_DUTY_CYCLE_SW: Set to '0' for nomral function. Read commands are generated during periodic cal with a 50% duty cycle. When set to '1', periodic cal issues read commands continuously.
54:56	RW	DDRPHY_RC_CONFIG0_P0_PER_REPEAT_COUNT: If this field is 000 then the number of additional periodic cals performed per request is zero. A nonzero value in this field will preform additional periodic calibrations for each request per below: 000 is No additional periodic cal iterations are performed per request. 001 is One additional periodic cal iteration is performed per request. 010 is Two additional periodic cal iterations are performed per request. .... 111 is Seven additional periodic cal iterations are performed per request.
57	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP0: '1'b - Single bit MPR pattern memory devices in Rank Pair 0. '0'b - All bit MPR pattern memory devices in Rank Pair 0.
58	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP1: '1'b - Single bit MPR pattern memory devices in Rank Pair 1. '0'b - All bit MPR pattern memory devices in Rank Pair 1.
59	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP2: '1'b - Single bit MPR pattern memory devices in Rank Pair 2. '0'b - All bit MPR pattern memory devices in Rank Pair 2.
60	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP3: '1'b - Single bit MPR pattern memory devices in Rank Pair 3. '0'b - All bit MPR pattern memory devices in Rank Pair 3.
61	RW	DDRPHY_RC_CONFIG0_P0_ALIGN_ON_EVEN_CYCLES: This bit is only valid in 4:1 Data Multiplexer Mode. In 2:1 Data Multiplexer Mode it must be '0'b. When set, latency is added, if required, to have the read data returned on the MEMCTL Interface with the first four beats of read data returned in the same dphy_nclk cycle on the R, F, RX, and FX pins. '1'b = The first beat of a read data burst is always returned on the R pin, second beat on the F pin, third beat on the RX pin, and fourth beat on the FX pin. '0'b = The first beat of a read data burst may be returned on the R or RX pin, second beat on the F or FX pin, third beat on the RX or R pin, and fourth beat on the FX or F pin. This bit must be '0'b when a burst length that is not a multiple of four is used.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_RC_CONFIG0_P0_PERFORM_RDCLK_ALIGN: This bit must be set to '1'b in hardware. This bit is a method for behavioral simulations to skip the calibration step. '1'b - The calibration must be performed for correct operation. '0'b - In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClkRdClk Alignment. Register values have no effect. The calibration fails if it is run.
63	RW	DDRPHY_RC_CONFIG0_P0_STAGGERED_PATTERN: '0'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Serial mode by the DDR PHY during Custom Read Centering. '1'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Staggered mode by the DDR PHY during Custom Read Centering.

Register Name	*RC Configuration 1*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG1_P0
Address	8000C8010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:61	RW	DDRPHY_RC_CONFIG1_P0_OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. Outer loop iteration count for digital eye. This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	constant=0b00

Register Name	*RC Configuration 2*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG2_P0
Address	8000C8020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_RC_CONFIG2_P0_CONSEQ_PASS: The number of consecutive passes required when determining the left edge of the data eye when stepping the read strobeclock through the phase rotator. When DIGITAL_EYE_EN is '1'b , this field, DIGEYE_MIN_SPACING, specifies the minimum number of cycles between outer loop iterations of digital eye (0-31 tCK cycles). This field must be set to minimum value of 6 when sampling 8 beats of data, and a minimum value of 12 when sampling 4 beats of data.
53:56	RW	
57:58	RW	DDRPHY_RC_CONFIG2_P0_BURST_WINDOW: Beats of data used for INIT and Periodic Read Eye Centering
59	RW	DDRPHY_RC_CONFIG2_P0_ALLOW_RD_FIFO_AUTO_RESET: Automatic Reset Control for RD FIFO
60:63	RO	constant=0b0000

Register Name	*RC Error Status 0*
Mnemonic	DPHY01.DDRPHY_RC_ERROR_STATUS0_P0
Address	8000C8050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	ROX	DDRPHY_RC_ERROR_STATUS0_P0_RD_CNTL_ERROR: '1'b - Read Control Error. See the register defined in for more information.
49:63	RO	constant=0b000000000000000

Register Name	*RC Error Mask 0*
Mnemonic	DPHY01.DDRPHY_RC_ERROR_MASK0_P0
Address	8000C8060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_RC_ERROR_MASK0_P0_RD_CNTL_ERROR_MASK: '1'b - Mask RD_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*RC Configuration 3*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG3_P0
Address	8000C8070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_RC_CONFIG3_P0_FINE_CAL_STEP_SIZE: Fine Calibration step size:000 = 1128, 001 = 164, 010 = 3128, 011 = 132100 = 5128, 101 = 364, 110 = 7128, 111 = 116
51:54	RW	DDRPHY_RC_CONFIG3_P0_COARSE_CAL_STEP_SIZE: Coarse Calibration step size:0000 = 1128, 0001 =164, 0010 = 3128, 0011 = 1320100 = 5128, 0101 = 364, 0110 = 7128, 0111 = 1161000 through 1111 = Reserved. When DIGITAL_EYE_EN is '1'b : bit 3:4 Reserved. bit 5: DIGEYE_16_NOT_1: '1'b - Block of 16 BL8 is issued during each outer loop iteration of digital eye. '0'b - One BL8 read is issued during each outer loop iteration of digital eye. bit 6: DIGEYE_REFRESH: '1' b - Issues a precharge and refresh during every outer loop iteration of digital eye. '0'b - Issues a precharge and refresh at least once every 16 outer loop iteration of digital eye.
55:56	RWX	DDRPHY_RC_CONFIG3_P0_DQ_SEL_QUAD: The quadrant within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that will automatically increment during some types of calibrations.
57:59	RWX	DDRPHY_RC_CONFIG3_P0_DQ_SEL_LANE: The data bit within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that automatically increments during some types of calibrations.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant=0b0000

Register Name	*WC Configuration 0*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG0_P0
Address	8000CC000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_WC_CONFIG0_P0_TWLO_TWLOE: Number of memory clock cycles which equals: 12 + {The greater of (Twldqsen - Tmod) converted to and rounded up to the nearest integer number of memory clock cycles or (Twlo + Twloe) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {Plus: The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} Used during Write Leveling.
56	RW	DDRPHY_WC_CONFIG0_P0_WL_ONE_DQS_PULSE: '0'b - continuous DQS pulses during Write Leveling. In 2:1 mode, 32 continuous pulses are sent. In 4:1 mode, 64 continuous pulses are sent. '1'b - one DQS pulse during each Write Leveling adjustment.
57:62	RW	DDRPHY_WC_CONFIG0_P0_FW_WR_RD: Number of memory clock cycles to wait between the write and read command pairs during Write Centering.
63	RW	DDRPHY_WC_CONFIG0_P0_CUSTOM_INIT_WRITE: '1'b - Write the data pattern in the registers during the Initial Pattern Write algorithm. '0'b - Write the MPR like pattern defined by the field MPR_PATTERN_BIT in the register defined in during the Initial Pattern Write algorithm.

Register Name	*WC Configuration 1*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG1_P0
Address	8000CC010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG1_P0_BIG_STEP: The amount the phase rotator value is adjusted during a big step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (BIG_STEP + 1) 128th of a memory clock.
52:54	RW	DDRPHY_WC_CONFIG1_P0_SMALL_STEP: The amount the phase rotator value is adjusted during a small step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (SMALL_STEP + 1)128th of a memory clock. Note: The Write Leveling and Write Centering algorithms will achieve the most accurate results when this field is set to zero.
55:60	RW	DDRPHY_WC_CONFIG1_P0_WR_PRE_DLY: The number of dphy_nclk cycles between a write command and a precharge command in the Coarse Initial Pattern Write, Initial Write, and Write Centering calibration algorithms.
61:63	RO	constant=0b000

Register Name	*WC Configuration 2*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG2_P0
Address	8000CC020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG2_P0_NUM_VALID_SAMPLES: The Write Leveling and Write Centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The Write Leveling algorithm performs the second to last sample at the current sample point plus 12 UI to ensure that the current sample point is at the '0'b to '1'b transition.
52:57	RW	DDRPHY_WC_CONFIG2_P0_FW_RD_WR: This delay value is used in two places in the write centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as AL + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3)
58:62	RW	
63	RW	DDRPHY_WC_CONFIG2_P0_EN_RESET_WR_DELAY_WL: '1'b - The registers are reset at the start of the Write Leveling Calibration algorithm for rank pair 0. '0'b - The registers are not reset at the start of the Write Leveling Calibration algorithm.

Register Name	*WC Error Status 0*
Mnemonic	DPHY01.DDRPHY_WC_ERROR_STATUS0_P0
Address	8000CC030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_WC_ERROR_STATUS0_P0_WR_CNTL_ERROR: '1'b - Write Control Error. See the register defined in for more information.
49:63	RO	constant=0b000000000000000

Register Name	*WC Error Mask 0*
Mnemonic	DPHY01.DDRPHY_WC_ERROR_MASK0_P0
Address	8000CC040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_ERROR_MASK0_P0_WR_CNTL_ERROR_MASK: '1'b - Mask WR_CNTL_ERROR.

Bits	SCOM	Field Mnemonic: Description
49:63	RO	constant=0b000000000000000

Register Name	*WC Configuration 3*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG3_P0
Address	8000CC050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_CONFIG3_P0_DDR4_MRS_CMD_DQ_EN: In DDR4: '1'b - When a DDR4 MRS command is detected passing through the DDR PHY, the values in the MRS_CMD_DATA_N{0,1,2,3} fields will be driven out on the DQ pins. '0'b - DQ pins are not driven when an MRS command passes through the DDR PHY. (DDR4 ballot 1716.52) For all other protocols, this bit must be '0'b.
49:54	RW	DDRPHY_WC_CONFIG3_P0_MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. WL_per_DRAM_addr = 10 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode WL_per_DRAM_addr = 18 + 2 * MRS_CMD_DQ_ON memory clock cycles in 4:1 mode
55:60	RW	DDRPHY_WC_CONFIG3_P0_MRS_CMD_DQ_OFF: MRS_CMD_DQ_OFF = the number of dphy_nclks after the DQ pin are driven the DQ pins are not set to high impedance.
61:63	RO	constant=0b000

Register Name	*APB Configuration 0*
Mnemonic	DPHY01.DDRPHY_APB_CONFIG0_P0
Address	8000D0000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_CONFIG0_P0_DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = False), this bit is reserved. If the core was configured for parity (APB_PARITY = True), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers and the PSLVERRO is not asserted due to bad write data parity.
49	RW	DDRPHY_APB_CONFIG0_P0_RESET_ERR_RPT: Write this bit to '1'b then write this bit to '0'b (toggle) to reset the registers defined in and.
50	RW	DDRPHY_APB_CONFIG0_P0_FORCE_ON_CLK_GATE: When set to '1'b, the clock gate in the APB Control Logic Block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB Control Logic Block to go to other logic blocks when the PHY is active.
51	RW	DDRPHY_APB_CONFIG0_P0_DEBUG_BUS_SEL_LO: Reserved.
52:55	RW	DDRPHY_APB_CONFIG0_P0_DEBUG__BUS_SEL_HI: Selects DP18 driving the high order half (bits 0:43) of the debugbus_o outputs.
56:63	RO	constant=0b00000000

Register Name	*APB Error Status 0*
Mnemonic	DPHY01.DDRPHY_APB_ERROR_STATUS0_P0
Address	8000D0010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_ERROR_STATUS0_P0_INVALID_ADDRESS: '1'b - Register read or write to an invalid, undefined, or unused address.
49	ROX	DDRPHY_APB_ERROR_STATUS0_P0_WR_PAR_ERR: '1'b - Write data during a write operation on the APB Interface did not have odd parity (parity error).
50:63	RO	constant=0b00000000000000

Register Name	*APB Error Mask 0*
Mnemonic	DPHY01.DDRPHY_APB_ERROR_MASK0_P0
Address	8000D0020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_ERROR_MASK0_P0_INVALID_ADDRESS_MASK: '1'b - Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	DDRPHY_APB_ERROR_MASK0_P0_WR_PAR_ERR_MASK: '1'b - Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	constant=0b00000000000000

Register Name	*APB ATEST Multiplexer Select*
Mnemonic	DPHY01.DDRPHY_APB_ATEST_MUX_SEL_P0
Address	8000D0050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:53	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_ATEST_CNTL: bit 0: Enable ATEST1 bits 1:2: Select ATEST1 source: '00'b - DP18 #0 '01'b - DP18 #1 '10'b - DP18 #2 '11'b - Reserved bit 3: Enable ATEST2 bits 4:5: Select ATEST2 source '00'b - DP18 #3 '01'b - DP18 #4 '10'b - ADR52S '11'b - Reserved
54	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR0: Inject error on FIR bit 0 (ports 02) or 32 (ports 13).
55	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR1: Inject error on FIR bit 1 (ports 02) or 33 (ports 13).
56	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR2: Inject error on FIR bit 2 (ports 02) or 34 (ports 13).

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR3: Inject error on FIR bit 3 (ports 02) or 35 (ports 13).
58	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR4: Inject error on FIR bit 4 (ports 02) or 36 (ports 13).
59:63	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_VPROTH_CTL: VPROTH ATEST Register Control used during manufacturing test. Set to 0 for normal function.

Register Name	***APB FIR Error 0***
Mnemonic	DPHY01.DDRPHY_APB_FIR_ERR0_P0
Address	8000D0060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET0: Indicates a non-recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 48 on ports 0 or 2; FIR bit 56 on ports 1 or 3. Reset by RESET_ERR_RPT in.
49	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET1: Indicates a non-recoverable register parity error in PHYTOP logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
50	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET2: Indicates a recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 51 on ports 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
51	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET3: Indicates a recoverable register parity error in PHYTOP logic. Sets FIR bit 52 on ports 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.
52	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET4: Indicates a non-recoverable register parity error in ADR52 master side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
53	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET5: Indicates a non-recoverable register parity error in ADR52 slave side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
54:58	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_FSM_DP18: Indicates a recoverable FSM state checker error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 51 on port 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
59:63	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_REG_DP18: Indicates a recoverable register parity error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 52 on port 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***APB FIR Error 1***
Mnemonic	DPHY01.DDRPHY_APB_FIR_ERR1_P0
Address	8000D0070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_APB_FIR_ERR1_P0_PC_ERR_STATUS0: Indicates a calibration error was latched in bits 0:2, 4:5 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Bits	SCOM	Field Mnemonic: Description
53:63	ROX	DDRPHY_APB_FIR_ERR1_P0_PC_INIT_CAL_ERR: Indicates a calibration error was latched in bits 0:10 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_0
Address	800100000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P1_DP18_0_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_0
Address	800100010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_HW_VALUE:
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_0
Address	800100020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P1_DP18_0_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_0
Address	800100030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	

Bits	SCOM	Field Mnemonic: Description
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_0
Address	800100040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_0
Address	800100050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_0
Address	800100060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers , staggered across DQ lanes as specified by the registers, and and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_0
Address	800100070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_0
Address	800100080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	*DP18 DQS Read Phase Select RP0*
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_0
Address	800100090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	*DP18 Drift Limits*
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_0
Address	8001000A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_0_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_0_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_0
Address	8001000B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_0
Address	8001000C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_0
Address	8001000D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_0
Address	8001000E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P1_DP18_0_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_0
Address	8001000F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P1_DP18_0_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_0
Address	800100100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P1_DP18_0_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_0
Address	800100110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P1_DP18_0_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_0
Address	800100120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_0
Address	800100130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P1_0
Address	800100140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_0
Address	800100150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_0
Address	800100170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_0
Address	800100180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_0
Address	800100190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P1_DP18_0_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_0
Address	8001001A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P1_DP18_0_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P1_0
Address	8001001B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_0
Address	8001001C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_0
Address	8001001D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_0_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_0_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_0_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_0
Address	800100300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_0
Address	800100310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_0
Address	800100320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_0
Address	800100330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_0
Address	800100340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_0
Address	800100370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P1_DP18_0_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_0
Address	800100380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_0
Address	800100390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_0
Address	8001003A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_0
Address	8001003B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_0
Address	8001003C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_0
Address	8001003D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_0
Address	8001003E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_0
Address	8001003F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_0
Address	800100400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_0
Address	800100410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_0
Address	800100420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_0
Address	800100430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_0
Address	800100440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_0
Address	800100450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_0
Address	800100460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_0
Address	800100470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_0
Address	800100480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_0
Address	8001004A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_0
Address	8001004C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_0
Address	8001004E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_0
Address	800100500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_0
Address	800100510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_0
Address	800100520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_0
Address	800100530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_0
Address	800100540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_0
Address	800100550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_0
Address	800100560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_0
Address	800100570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_0
Address	8001005C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_0
Address	8001005D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_0
Address	800100600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_0
Address	800100610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_0
Address	800100620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_0
Address	800100630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_0
Address	800100640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_0
Address	800100650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_0
Address	800100660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_0
Address	800100670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_0
Address	800100680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_0
Address	800100690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_0
Address	8001006A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_0
Address	8001006B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_0
Address	8001006D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_0_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_0_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0
Address	8001006F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	*DP18 Read Timing Reference 0*
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_0
Address	800100700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_0_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_0_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read Timing Reference 1*
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_0
Address	800100710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_0_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_0_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read DQS Timing Reference*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_0
Address	800100720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P1_DP18_0_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_0
Address	800100730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_0_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P1_0
Address	800100740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P1_DP18_0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_0
Address	800100750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_0_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_0_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_0_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_0
Address	800100760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_0
Address	800100770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_0
Address	800100780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_0_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_0_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_0
Address	800100790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_0_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_0_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_0
Address	8001007A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_0_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_0_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_0
Address	8001007B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_0_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_0_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_0
Address	8001007C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_0
Address	8001007D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_0
Address	8001007E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_0
Address	800101040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_0
Address	800101050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_0
Address	800101090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_0
Address	8001010C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_0
Address	8001010D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_0
Address	800101130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_0
Address	800101300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_0
Address	800101310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_0
Address	800101380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_0
Address	800101390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_0
Address	8001013A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_0
Address	8001013B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_0
Address	8001013C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_0
Address	8001013D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_0
Address	8001013E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_0
Address	8001013F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_0
Address	800101400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_0
Address	800101410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_0
Address	800101420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_0
Address	800101430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_0
Address	800101440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_0
Address	800101450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_0
Address	800101460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_0
Address	800101470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_0
Address	800101480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_0
Address	8001014A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_0
Address	8001014C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_0
Address	8001014E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_0
Address	800101500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_0
Address	800101510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_0
Address	800101520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_0
Address	800101530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_0
Address	800101540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_0
Address	800101550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_0
Address	800101560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_0
Address	800101570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_0
Address	8001015C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_0
Address	8001015D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_0
Address	800101600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_0
Address	800101610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_0
Address	800101620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_0
Address	800101630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_0
Address	800101640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_0
Address	800101650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_0
Address	800101660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_0
Address	800101670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_0
Address	800101680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_0
Address	800101690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_0
Address	8001016A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_0
Address	8001016B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_0
Address	8001017C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_0
Address	8001017D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_0
Address	8001017E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_0
Address	800102040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_0
Address	800102050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_0
Address	800102090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_0
Address	8001020C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_0
Address	8001020D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_0
Address	800102130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_0
Address	800102300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 DQSClk Phase Rotator Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_0
Address	800102310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Write Delay Value 0 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_0
Address	800102380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_0
Address	800102390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_0
Address	8001023A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_0
Address	8001023B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_0
Address	8001023C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_0
Address	8001023D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_0
Address	8001023E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_0
Address	8001023F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_0
Address	800102400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_0
Address	800102410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_0
Address	800102420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_0
Address	800102430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_0
Address	800102440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_0
Address	800102450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_0
Address	800102460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_0
Address	800102470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_0
Address	800102480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_0
Address	8001024A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_0
Address	8001024C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_0
Address	8001024E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_0
Address	800102500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_0
Address	800102510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_0
Address	800102520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_0
Address	800102530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_0
Address	800102540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_0
Address	800102550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_0
Address	800102560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_0
Address	800102570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_0
Address	8001025C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_0
Address	8001025D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_0
Address	800102600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_0
Address	800102610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_0
Address	800102620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_0
Address	800102630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_0
Address	800102640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_0
Address	800102650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_0
Address	800102660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_0
Address	800102670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_0
Address	800102680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_0
Address	800102690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_0
Address	8001026A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_0
Address	8001026B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_0
Address	8001027C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Disable 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_0
Address	8001027D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	*DP18 Write DQ Offset Value RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_0
Address	8001027E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_0
Address	800103040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_0
Address	800103050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_0
Address	800103090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_0
Address	8001030C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_0
Address	8001030D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_0
Address	800103130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_0
Address	800103300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_0
Address	800103310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_0
Address	800103380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_0
Address	800103390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_0
Address	8001033A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_0
Address	8001033B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_0
Address	8001033C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_0
Address	8001033D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_0
Address	8001033E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_0
Address	8001033F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_0
Address	800103400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_0
Address	800103410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_0
Address	800103420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_0
Address	800103430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_0
Address	800103440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_0
Address	800103450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_0
Address	800103460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_0
Address	800103470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_0
Address	800103480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_0
Address	8001034A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_0
Address	8001034C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_0
Address	8001034E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_0
Address	800103500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_0
Address	800103510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_0
Address	800103520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_0
Address	800103530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_0
Address	800103540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_0
Address	800103550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_0
Address	800103560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_0
Address	800103570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_0
Address	8001035C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_0
Address	8001035D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_0
Address	800103600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_0
Address	800103610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_0
Address	800103620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_0
Address	800103630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_0
Address	800103640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_0
Address	800103650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_0
Address	800103660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_0
Address	800103670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_0
Address	800103680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_0
Address	800103690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_0
Address	8001036A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_0
Address	8001036B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_0
Address	8001037C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_0
Address	8001037D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_0
Address	8001037E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_1
Address	800104000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P1_DP18_1_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_1
Address	800104010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_HW_VALUE:
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_1
Address	800104020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P1_DP18_1_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_1
Address	800104030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_1
Address	800104040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_1
Address	800104050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_1
Address	800104060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core. See for more information.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_1
Address	800104070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_1
Address	800104080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_1
Address	800104090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_1
Address	8001040A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_1_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_1_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_1
Address	8001040B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_1
Address	8001040C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_1
Address	8001040D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_1
Address	8001040E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P1_DP18_1_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_1
Address	8001040F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P1_DP18_1_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Centering Status 2*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_1
Address	800104100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P1_DP18_1_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_1
Address	800104110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P1_DP18_1_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_1
Address	800104120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_1
Address	800104130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P1_1
Address	800104140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_1
Address	800104150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_1
Address	800104170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_1
Address	800104180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_1
Address	800104190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P1_DP18_1_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_1
Address	8001041A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P1_DP18_1_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P1_1
Address	8001041B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_1
Address	8001041C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_1
Address	8001041D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_1_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_1_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_1_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_1
Address	800104300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_1
Address	800104310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_1
Address	800104320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_1
Address	800104330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_1
Address	800104340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_1
Address	800104370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P1_DP18_1_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_1
Address	800104380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_1
Address	800104390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_1
Address	8001043A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_1
Address	8001043B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_1
Address	8001043C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_1
Address	8001043D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_1
Address	8001043E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_1
Address	8001043F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_1
Address	800104400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_1
Address	800104410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_1
Address	800104420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_1
Address	800104430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_1
Address	800104440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_1
Address	800104450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_1
Address	800104460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_1
Address	800104470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_1
Address	800104480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_1
Address	8001044A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_1
Address	8001044C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_1
Address	8001044E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_1
Address	800104500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_1
Address	800104510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_1
Address	800104520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_1
Address	800104530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_1
Address	800104540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_1
Address	800104550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_1
Address	800104560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_1
Address	800104570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_1
Address	8001045C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_1
Address	8001045D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_1
Address	800104600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_1
Address	800104610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_1
Address	800104620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_1
Address	800104630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_1
Address	800104640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_1
Address	800104650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_1
Address	800104660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_1
Address	800104670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_1
Address	800104680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_1
Address	800104690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_1
Address	8001046A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_1
Address	8001046B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_1
Address	8001046D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_1_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_1_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1
Address	8001046F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_1
Address	800104700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_1_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_1_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_1
Address	800104710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_1_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_1_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_1
Address	800104720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P1_DP18_1_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_1
Address	800104730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_1_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field .
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P1_1
Address	800104740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P1_DP18_1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_1
Address	800104750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_1_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_1_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_1_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_1
Address	800104760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_1
Address	800104770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_1
Address	800104780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_1_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_1_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_1
Address	800104790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_1_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_1_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_1
Address	8001047A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_1_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_1_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_1
Address	8001047B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_1_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_1_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_1
Address	8001047C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_1
Address	8001047D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_1
Address	8001047E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_1
Address	800105040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_1
Address	800105050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_1
Address	800105090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_1
Address	8001050C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_1
Address	8001050D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_1
Address	800105130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_1
Address	800105300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_1
Address	800105310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b00000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_1
Address	800105380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_1
Address	800105390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_1
Address	8001053A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_1
Address	8001053B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_1
Address	8001053C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_1
Address	8001053D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_1
Address	8001053E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_1
Address	8001053F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_1
Address	800105400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_1
Address	800105410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_1
Address	800105420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_1
Address	800105430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_1
Address	800105440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_1
Address	800105450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_1
Address	800105460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_1
Address	800105470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_1
Address	800105480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_1
Address	8001054A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_1
Address	8001054C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_1
Address	8001054E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_1
Address	800105500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_1
Address	800105510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_1
Address	800105520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_1
Address	800105530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_1
Address	800105540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_1
Address	800105550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_1
Address	800105560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_1
Address	800105570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_1
Address	8001055C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_1
Address	8001055D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_1
Address	800105600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_1
Address	800105610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_1
Address	800105620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_1
Address	800105630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_1
Address	800105640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_1
Address	800105650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_1
Address	800105660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_1
Address	800105670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_1
Address	800105680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_1
Address	800105690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_1
Address	8001056A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_1
Address	8001056B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_1
Address	8001057C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_1
Address	8001057D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_1
Address	8001057E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_1
Address	800106040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_1
Address	800106050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_1
Address	800106090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_1
Address	8001060C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_1
Address	8001060D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_1
Address	800106130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_1
Address	800106300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 DQSClk Phase Rotator Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_1
Address	800106310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Write Delay Value 0 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_1
Address	800106380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_1
Address	800106390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_1
Address	8001063A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_1
Address	8001063B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_1
Address	8001063C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_1
Address	8001063D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_1
Address	8001063E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_1
Address	8001063F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_1
Address	800106400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_1
Address	800106410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_1
Address	800106420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_1
Address	800106430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_1
Address	800106440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_1
Address	800106450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_1
Address	800106460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_1
Address	800106470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_1
Address	800106480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_1
Address	8001064A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_1
Address	8001064C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_1
Address	8001064E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_1
Address	800106500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_1
Address	800106510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_1
Address	800106520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_1
Address	800106530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_1
Address	800106540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_1
Address	800106550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_1
Address	800106560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_1
Address	800106570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_1
Address	8001065C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_1
Address	8001065D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_1
Address	800106600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_1
Address	800106610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_1
Address	800106620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_1
Address	800106630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_1
Address	800106640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_1
Address	800106650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_1
Address	800106660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_1
Address	800106670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_1
Address	800106680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_1
Address	800106690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_1
Address	8001066A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_1
Address	8001066B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_1
Address	8001067C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_1
Address	8001067D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_1
Address	8001067E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_1
Address	800107040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_1
Address	800107050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_1
Address	800107090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_1
Address	8001070C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_1
Address	8001070D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_1
Address	800107130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_1
Address	800107300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_1
Address	800107310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_1
Address	800107380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_1
Address	800107390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_1
Address	8001073A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_1
Address	8001073B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_1
Address	8001073C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_1
Address	8001073D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_1
Address	8001073E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_1
Address	8001073F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_1
Address	800107400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_1
Address	800107410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_1
Address	800107420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_1
Address	800107430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_1
Address	800107440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_1
Address	800107450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_1
Address	800107460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_1
Address	800107470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_1
Address	800107480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_1
Address	8001074A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_1
Address	8001074C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_1
Address	8001074E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_1
Address	800107500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_1
Address	800107510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_1
Address	800107520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_1
Address	800107530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_1
Address	800107540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_1
Address	800107550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_1
Address	800107560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 7 RP3*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_1
Address	800107570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_1
Address	8001075C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_1
Address	8001075D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_1
Address	800107600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_1
Address	800107610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_1
Address	800107620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_1
Address	800107630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_1
Address	800107640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_1
Address	800107650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_1
Address	800107660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_1
Address	800107670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_1
Address	800107680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_1
Address	800107690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_1
Address	8001076A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_1
Address	8001076B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_1
Address	8001077C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_1
Address	8001077D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_1
Address	8001077E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_2
Address	800108000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P1_DP18_2_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_2
Address	800108010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_HW_VALUE:
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_2
Address	800108020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P1_DP18_2_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_2
Address	800108030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_2
Address	800108040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_2
Address	800108050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_2
Address	800108060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT field.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_2
Address	800108070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_2
Address	800108080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_2
Address	800108090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_2
Address	8001080A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_2_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_2_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_2
Address	8001080B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_2
Address	8001080C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_2
Address	8001080D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_2
Address	8001080E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P1_DP18_2_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_2
Address	8001080F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P1_DP18_2_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Centering Status 2*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_2
Address	800108100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P1_DP18_2_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_2
Address	800108110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P1_DP18_2_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_2
Address	800108120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_2
Address	800108130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P1_2
Address	800108140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_2
Address	800108150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_2
Address	800108170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_2
Address	800108180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_2
Address	800108190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P1_DP18_2_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_2
Address	8001081A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P1_DP18_2_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P1_2
Address	8001081B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_2
Address	8001081C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_2
Address	8001081D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_2_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_2_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_2_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_2
Address	800108300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_2
Address	800108310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_2
Address	800108320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_2
Address	800108330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_2
Address	800108340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_2
Address	800108370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P1_DP18_2_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_2
Address	800108380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_2
Address	800108390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_2
Address	8001083A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_2
Address	8001083B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_2
Address	8001083C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_2
Address	8001083D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_2
Address	8001083E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_2
Address	8001083F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_2
Address	800108400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_2
Address	800108410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_2
Address	800108420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_2
Address	800108430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_2
Address	800108440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_2
Address	800108450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_2
Address	800108460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_2
Address	800108470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_2
Address	800108480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_2
Address	8001084A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_2
Address	8001084C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_2
Address	8001084E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_2
Address	800108500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_2
Address	800108510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_2
Address	800108520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_2
Address	800108530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_2
Address	800108540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_2
Address	800108550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_2
Address	800108560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_2
Address	800108570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_2
Address	8001085C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_2
Address	8001085D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_2
Address	800108600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_2
Address	800108610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_2
Address	800108620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_2
Address	800108630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_2
Address	800108640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_2
Address	800108650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_2
Address	800108660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_2
Address	800108670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_2
Address	800108680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_2
Address	800108690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_2
Address	8001086A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_2
Address	8001086B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_2
Address	8001086D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_2_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_2_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2
Address	8001086F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	*DP18 Read Timing Reference 0*
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_2
Address	800108700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_2_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_2_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read Timing Reference 1*
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_2
Address	800108710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_2_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_2_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read DQS Timing Reference*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_2
Address	800108720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P1_DP18_2_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_2
Address	800108730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_2_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_2_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P1_2
Address	800108740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P1_DP18_2_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_2
Address	800108750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_2_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_2_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_2_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_2
Address	800108760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_2
Address	800108770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_2
Address	800108780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_2_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_2_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_2
Address	800108790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_2_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_2_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_2
Address	8001087A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_2_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_2_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_2
Address	8001087B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_2_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_2_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_2
Address	8001087C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_2
Address	8001087D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_2
Address	8001087E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_2
Address	800109040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_2
Address	800109050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_2
Address	800109090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_2
Address	8001090C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_2
Address	8001090D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_2
Address	800109130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_2
Address	800109300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_2
Address	800109310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_2
Address	800109380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_2
Address	800109390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_2
Address	8001093A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_2
Address	8001093B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_2
Address	8001093C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_2
Address	8001093D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_2
Address	8001093E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_2
Address	8001093F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_2
Address	800109400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_2
Address	800109410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_2
Address	800109420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_2
Address	800109430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_2
Address	800109440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_2
Address	800109450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_2
Address	800109460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_2
Address	800109470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_2
Address	800109480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_2
Address	8001094A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_2
Address	8001094C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_2
Address	8001094E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_2
Address	800109500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_2
Address	800109510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_2
Address	800109520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_2
Address	800109530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_2
Address	800109540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_2
Address	800109550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_2
Address	800109560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_2
Address	800109570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_2
Address	8001095C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_2
Address	8001095D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_2
Address	800109600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_2
Address	800109610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_2
Address	800109620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_2
Address	800109630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_2
Address	800109640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_2
Address	800109650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_2
Address	800109660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_2
Address	800109670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_2
Address	800109680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_2
Address	800109690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_2
Address	8001096A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_2
Address	8001096B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_2
Address	8001097C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_2
Address	8001097D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_2
Address	8001097E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_2
Address	80010A040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_2
Address	80010A050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_2
Address	80010A090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_2
Address	80010A0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_2
Address	80010A0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_2
Address	80010A130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_2
Address	80010A300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_2
Address	80010A310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_2
Address	80010A380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_2
Address	80010A390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_2
Address	80010A3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_2
Address	80010A3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_2
Address	80010A3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_2
Address	80010A3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_2
Address	80010A3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_2
Address	80010A3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_2
Address	80010A400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_2
Address	80010A410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_2
Address	80010A420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_2
Address	80010A430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_2
Address	80010A440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_2
Address	80010A450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_2
Address	80010A460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_2
Address	80010A470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_2
Address	80010A480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_2
Address	80010A4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_2
Address	80010A4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_2
Address	80010A4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_2
Address	80010A500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_2
Address	80010A510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_2
Address	80010A520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_2
Address	80010A530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_2
Address	80010A540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_2
Address	80010A550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_2
Address	80010A560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_2
Address	80010A570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_2
Address	80010A5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_2
Address	80010A5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_2
Address	80010A600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_2
Address	80010A610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_2
Address	80010A620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_2
Address	80010A630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_2
Address	80010A640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_2
Address	80010A650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_2
Address	80010A660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_2
Address	80010A670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_2
Address	80010A680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_2
Address	80010A690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_2
Address	80010A6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_2
Address	80010A6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_2
Address	80010A7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_2
Address	80010A7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_2
Address	80010A7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_2
Address	80010B040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_2
Address	80010B050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_2
Address	80010B090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_2
Address	80010B0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_2
Address	80010B0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_2
Address	80010B130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_2
Address	80010B300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_2
Address	80010B310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_2
Address	80010B380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_2
Address	80010B390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_2
Address	80010B3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_2
Address	80010B3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_2
Address	80010B3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_2
Address	80010B3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_2
Address	80010B3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_2
Address	80010B3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_2
Address	80010B400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_2
Address	80010B410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_2
Address	80010B420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_2
Address	80010B430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_2
Address	80010B440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_2
Address	80010B450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_2
Address	80010B460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_2
Address	80010B470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_2
Address	80010B480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_2
Address	80010B4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_2
Address	80010B4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_2
Address	80010B4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_2
Address	80010B500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_2
Address	80010B510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_2
Address	80010B520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_2
Address	80010B530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_2
Address	80010B540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_2
Address	80010B550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_2
Address	80010B560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_2
Address	80010B570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_2
Address	80010B5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_2
Address	80010B5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_2
Address	80010B600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_2
Address	80010B610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_2
Address	80010B620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_2
Address	80010B630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_2
Address	80010B640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_2
Address	80010B650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_2
Address	80010B660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_2
Address	80010B670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_2
Address	80010B680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_2
Address	80010B690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_2
Address	80010B6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_2
Address	80010B6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_2
Address	80010B7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_2
Address	80010B7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_2
Address	80010B7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_3
Address	80010C000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P1_DP18_3_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_3
Address	80010C010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_HW_VALUE:
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_3
Address	80010C020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P1_DP18_3_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. See. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_3
Address	80010C030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_3
Address	80010C040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_3
Address	80010C050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_3
Address	80010C060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers,, and and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field . For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_3
Address	80010C070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_3
Address	80010C080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_3
Address	80010C090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_3
Address	80010C0A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_3_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_3_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_3
Address	80010C0B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_3
Address	80010C0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_3
Address	80010C0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_3
Address	80010C0E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P1_DP18_3_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_3
Address	80010C0F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P1_DP18_3_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Centering Status 2*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_3
Address	80010C100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P1_DP18_3_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_3
Address	80010C110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P1_DP18_3_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_3
Address	80010C120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_3
Address	80010C130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P1_3
Address	80010C140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_3
Address	80010C150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_3
Address	80010C170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_3
Address	80010C180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_3
Address	80010C190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P1_DP18_3_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_3
Address	80010C1A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P1_DP18_3_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P1_3
Address	80010C1B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_3
Address	80010C1C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_3
Address	80010C1D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_3_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_3_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_3_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_3
Address	80010C300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_3
Address	80010C310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_3
Address	80010C320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_3
Address	80010C330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_3
Address	80010C340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_3
Address	80010C370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P1_DP18_3_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_3
Address	80010C380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_3
Address	80010C390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_3
Address	80010C3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_3
Address	80010C3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_3
Address	80010C3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_3
Address	80010C3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_3
Address	80010C3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_3
Address	80010C3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_3
Address	80010C400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_3
Address	80010C410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_3
Address	80010C420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_3
Address	80010C430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_3
Address	80010C440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_3
Address	80010C450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_3
Address	80010C460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_3
Address	80010C470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_3
Address	80010C480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_3
Address	80010C4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_3
Address	80010C4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_3
Address	80010C4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_3
Address	80010C500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_3
Address	80010C510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_3
Address	80010C520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_3
Address	80010C530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_3
Address	80010C540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_3
Address	80010C550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_3
Address	80010C560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_3
Address	80010C570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_3
Address	80010C5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_3
Address	80010C5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_3
Address	80010C600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_3
Address	80010C610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_3
Address	80010C620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_3
Address	80010C630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_3
Address	80010C640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_3
Address	80010C650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_3
Address	80010C660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_3
Address	80010C670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_3
Address	80010C680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_3
Address	80010C690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_3
Address	80010C6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_3
Address	80010C6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_3
Address	80010C6D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_3_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_3_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to impove jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3
Address	80010C6F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	*DP18 Read Timing Reference 0*
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_3
Address	80010C700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_3_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_3_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read Timing Reference 1*
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_3
Address	80010C710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_3_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_3_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read DQS Timing Reference*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_3
Address	80010C720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P1_DP18_3_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_3
Address	80010C730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_3_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_3_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P1_3
Address	80010C740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P1_DP18_3_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_3
Address	80010C750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_3_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_3_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_3_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	*DP18 PLL/VREG Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_3
Address	80010C760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_3
Address	80010C770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_3
Address	80010C780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_3_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_3_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_3
Address	80010C790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_3_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_3_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_3
Address	80010C7A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_3_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_3_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_3
Address	80010C7B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_3_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_3_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_3
Address	80010C7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_3
Address	80010C7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_3
Address	80010C7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_3
Address	80010D040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_3
Address	80010D050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_3
Address	80010D090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_3
Address	80010D0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_3
Address	80010D0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_3
Address	80010D130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_3
Address	80010D300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_3
Address	80010D310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_3
Address	80010D380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_3
Address	80010D390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_3
Address	80010D3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_3
Address	80010D3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_3
Address	80010D3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_3
Address	80010D3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_3
Address	80010D3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_3
Address	80010D3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_3
Address	80010D400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_3
Address	80010D410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_3
Address	80010D420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_3
Address	80010D430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_3
Address	80010D440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_3
Address	80010D450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_3
Address	80010D460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_3
Address	80010D470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_3
Address	80010D480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_3
Address	80010D4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_3
Address	80010D4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_3
Address	80010D4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_3
Address	80010D500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_3
Address	80010D510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_3
Address	80010D520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_3
Address	80010D530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_3
Address	80010D540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_3
Address	80010D550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_3
Address	80010D560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_3
Address	80010D570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_3
Address	80010D5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_3
Address	80010D5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_3
Address	80010D600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_3
Address	80010D610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_3
Address	80010D620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_3
Address	80010D630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_3
Address	80010D640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_3
Address	80010D650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_3
Address	80010D660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_3
Address	80010D670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_3
Address	80010D680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_3
Address	80010D690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_3
Address	80010D6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_3
Address	80010D6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_3
Address	80010D7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_3
Address	80010D7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_3
Address	80010D7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_3
Address	80010E040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_3
Address	80010E050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_3
Address	80010E090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_3
Address	80010E0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_3
Address	80010E0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_3
Address	80010E130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_3
Address	80010E300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 DQSClk Phase Rotator Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_3
Address	80010E310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Write Delay Value 0 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_3
Address	80010E380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_3
Address	80010E390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_3
Address	80010E3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_3
Address	80010E3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_3
Address	80010E3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_3
Address	80010E3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_3
Address	80010E3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_3
Address	80010E3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_3
Address	80010E400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_3
Address	80010E410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_3
Address	80010E420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_3
Address	80010E430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_3
Address	80010E440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_3
Address	80010E450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_3
Address	80010E460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_3
Address	80010E470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_3
Address	80010E480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_3
Address	80010E4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_3
Address	80010E4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_3
Address	80010E4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_3
Address	80010E500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_3
Address	80010E510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_3
Address	80010E520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_3
Address	80010E530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_3
Address	80010E540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_3
Address	80010E550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_3
Address	80010E560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_3
Address	80010E570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_3
Address	80010E5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_3
Address	80010E5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_3
Address	80010E600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_3
Address	80010E610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_3
Address	80010E620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_3
Address	80010E630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_3
Address	80010E640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_3
Address	80010E650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_3
Address	80010E660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_3
Address	80010E670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_3
Address	80010E680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_3
Address	80010E690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_3
Address	80010E6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_3
Address	80010E6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_3
Address	80010E7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_3
Address	80010E7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_3
Address	80010E7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_3
Address	80010F040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_3
Address	80010F050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_3
Address	80010F090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_3
Address	80010F0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_3
Address	80010F0D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_3
Address	80010F130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_3
Address	80010F300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_3
Address	80010F310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_3
Address	80010F380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_3
Address	80010F390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_3
Address	80010F3A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_3
Address	80010F3B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_3
Address	80010F3C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_3
Address	80010F3D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_3
Address	80010F3E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_3
Address	80010F3F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_3
Address	80010F400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_3
Address	80010F410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_3
Address	80010F420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_3
Address	80010F430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_3
Address	80010F440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_3
Address	80010F450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_3
Address	80010F460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_3
Address	80010F470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_3
Address	80010F480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_3
Address	80010F4A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_3
Address	80010F4C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_3
Address	80010F4E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_3
Address	80010F500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_3
Address	80010F510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_3
Address	80010F520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_3
Address	80010F530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_3
Address	80010F540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_3
Address	80010F550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_3
Address	80010F560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_3
Address	80010F570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_3
Address	80010F5C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_3
Address	80010F5D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_3
Address	80010F600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_3
Address	80010F610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_3
Address	80010F620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_3
Address	80010F630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_3
Address	80010F640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_3
Address	80010F650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_3
Address	80010F660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_3
Address	80010F670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_3
Address	80010F680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_3
Address	80010F690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_3
Address	80010F6A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_3
Address	80010F6B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_3
Address	80010F7C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_3
Address	80010F7D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_3
Address	80010F7E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_4
Address	800110000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE0_P1_DP18_4_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_4
Address	800110010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_HW_VALUE:
60	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR0_P1_4
Address	800110020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DIR0_P1_DP18_4_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DIR1_P1_4
Address	800110030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_4
Address	800110040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP0_P1_4
Address	800110050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_RX_PEAK_AMP_P1_4
Address	800110060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.
60	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers, staggered across DQ lanes as specified by the registers and rotated through the four bytes of the registers every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT.

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_P1_4
Address	800110070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register resets to zero.
57	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_DIG_EYE_P1_4
Address	800110080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_4
Address	800110090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY01.DDRPHY_DP18_DRIFT_LIMITS_P1_4
Address	8001100A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P1_DP18_4_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P1_DP18_4_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY01.DDRPHY_DP18_DEBUG_SEL_P1_4
Address	8001100B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_4
Address	8001100C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_4
Address	8001100D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS0_P1_4
Address	8001100E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS0_P1_DP18_4_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS1_P1_4
Address	8001100F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS1_P1_DP18_4_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS2_P1_4
Address	800110100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS2_P1_DP18_4_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_LVL_STATUS3_P1_4
Address	800110110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS3_P1_DP18_4_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG5_P1_4
Address	800110120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_4
Address	800110130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_STATUS0_P1_4
Address	800110140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_RD_ERROR_MASK0_P1_4
Address	800110150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_LVL_STATUS0_P1_4
Address	800110170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS0_P1_4
Address	800110180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS1_P1_4
Address	800110190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS1_P1_DP18_4_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY01.DDRPHY_DP18_WR_CNTR_STATUS2_P1_4
Address	8001101A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS2_P1_DP18_4_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR0_P1_4
Address	8001101B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	***DP18 Write Error Mask 0***
Mnemonic	DPHY01.DDRPHY_DP18_WR_ERROR_MASK0_P1_4
Address	8001101C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY01.DDRPHY_DP18_DFT_WRAP_STATUS_P1_4
Address	8001101D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P1_DP18_4_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P1_DP18_4_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P1_DP18_4_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_4
Address	800110300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_4
Address	800110310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_0_P1_4
Address	800110320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_1_P1_4
Address	800110330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY01.DDRPHY_DP18_PATTERN_POS_2_P1_4
Address	800110340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_OFFSET_P1_4
Address	800110370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_OFFSET_P1_DP18_4_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_4
Address	800110380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_4
Address	800110390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_4
Address	8001103A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_4
Address	8001103B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_4
Address	8001103C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_4
Address	8001103D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_4
Address	8001103E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_4
Address	8001103F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_4
Address	800110400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_4
Address	800110410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_4
Address	800110420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_4
Address	800110430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_4
Address	800110440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_4
Address	800110450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_4
Address	800110460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_4
Address	800110470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_4
Address	800110480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_4
Address	8001104A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_4
Address	8001104C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_4
Address	8001104E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_4
Address	800110500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_4
Address	800110510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_4
Address	800110520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_4
Address	800110530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_4
Address	800110540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_4
Address	800110550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_4
Address	800110560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_4
Address	800110570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_4
Address	8001105C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_4
Address	8001105D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_4
Address	800110600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_4
Address	800110610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_4
Address	800110620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_4
Address	800110630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_4
Address	800110640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_4
Address	800110650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_4
Address	800110660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_4
Address	800110670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_4
Address	800110680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_4
Address	800110690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_4
Address	8001106A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_4
Address	8001106B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY01.DDRPHY_DP18_RD_DIA_CONFIG3_P1_4
Address	8001106D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_4_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_4_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes it simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY01.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4
Address	8001106F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_4
Address	800110700301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P1_DP18_4_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P1_DP18_4_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_4
Address	800110710301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P1_DP18_4_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P1_DP18_4_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_4
Address	800110720301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DQS_TIMING_REFERENCE_P1_DP18_4_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY01.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_4
Address	800110730301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P1_DP18_4_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P1_DP18_4_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_PR_P1_4
Address	800110740301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_WRCLK_PR_P1_DP18_4_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_CONFIG0_P1_4
Address	800110750301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P1_DP18_4_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P1_DP18_4_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P1_DP18_4_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG0_P1_4
Address	800110760301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_DP18_PLL_CONFIG1_P1_4
Address	800110770301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_4
Address	800110780301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P1_DP18_4_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P1_DP18_4_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_4
Address	800110790301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P1_DP18_4_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P1_DP18_4_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_NFET_TERM_P1_4
Address	8001107A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P1_DP18_4_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P1_DP18_4_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY01.DDRPHY_DP18_IO_TX_PFET_TERM_P1_4
Address	8001107B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P1_DP18_4_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P1_DP18_4_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_4
Address	8001107C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP0_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_4
Address	8001107D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP0_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_4
Address	8001107E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_4
Address	800111040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP1_P1_4
Address	800111050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_4
Address	800111090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_4
Address	8001110C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_4
Address	8001110D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_4
Address	800111130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_4
Address	800111300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_4
Address	800111310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_4
Address	800111380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_4
Address	800111390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_4
Address	8001113A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_4
Address	8001113B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_4
Address	8001113C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_4
Address	8001113D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_4
Address	8001113E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_4
Address	8001113F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_4
Address	800111400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_4
Address	800111410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_4
Address	800111420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP1*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_4
Address	800111430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_4
Address	800111440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_4
Address	800111450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_4
Address	800111460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_4
Address	800111470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_4
Address	800111480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_4
Address	8001114A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_4
Address	8001114C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_4
Address	8001114E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_4
Address	800111500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_4
Address	800111510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_4
Address	800111520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_4
Address	800111530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_4
Address	800111540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_4
Address	800111550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_4
Address	800111560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_4
Address	800111570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_4
Address	8001115C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_4
Address	8001115D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_4
Address	800111600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_4
Address	800111610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_4
Address	800111620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_4
Address	800111630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_4
Address	800111640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_4
Address	800111650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_4
Address	800111660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_4
Address	800111670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_4
Address	800111680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_4
Address	800111690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_4
Address	8001116A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_4
Address	8001116B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_4
Address	8001117C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP1_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_4
Address	8001117D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP1_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_4
Address	8001117E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_4
Address	800112040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP2_P1_4
Address	800112050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_4
Address	800112090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_4
Address	8001120C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_4
Address	8001120D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_4
Address	800112130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_4
Address	800112300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 DQSClk Phase Rotator Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_4
Address	800112310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Write Delay Value 0 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_4
Address	800112380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_4
Address	800112390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_4
Address	8001123A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_4
Address	8001123B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_4
Address	8001123C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_4
Address	8001123D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_4
Address	8001123E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_4
Address	8001123F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_4
Address	800112400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_4
Address	800112410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_4
Address	800112420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_4
Address	800112430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_4
Address	800112440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_4
Address	800112450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_4
Address	800112460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_4
Address	800112470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_4
Address	800112480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_4
Address	8001124A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_4
Address	8001124C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP2*
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_4
Address	8001124E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.

Bits	SCOM	Field Mnemonic: Description
58:63	RO	constant=0b000000

Register Name	*DP18 Read Delay Value 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_4
Address	800112500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_4
Address	800112510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_4
Address	800112520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_4
Address	800112530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_4
Address	800112540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_4
Address	800112550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_4
Address	800112560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_4
Address	800112570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_4
Address	8001125C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_4
Address	8001125D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP2*
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_4
Address	800112600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_4
Address	800112610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_4
Address	800112620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_4
Address	800112630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_4
Address	800112640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_4
Address	800112650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_4
Address	800112660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_4
Address	800112670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_4
Address	800112680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_4
Address	800112690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_4
Address	8001126A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_4
Address	8001126B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_4
Address	8001127C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP2_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_4
Address	8001127D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP2_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_4
Address	8001127E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_4
Address	800113040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY01.DDRPHY_DP18_WRCLK_EN_RP3_P1_4
Address	800113050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_4
Address	800113090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_4
Address	8001130C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_4
Address	8001130D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_4
Address	800113130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_4
Address	800113300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_4
Address	800113310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_4
Address	800113380301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_4
Address	800113390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_4
Address	8001133A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_4
Address	8001133B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_4
Address	8001133C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_4
Address	8001133D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_4
Address	8001133E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_4
Address	8001133F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_4
Address	800113400301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_4
Address	800113410301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_4
Address	800113420301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_4
Address	800113430301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_4
Address	800113440301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_4
Address	800113450301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_4
Address	800113460301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_4
Address	800113470301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_4
Address	800113480301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_4
Address	8001134A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_4
Address	8001134C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY01.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_4
Address	8001134E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_4
Address	800113500301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_4
Address	800113510301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_4
Address	800113520301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_4
Address	800113530301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_4
Address	800113540301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_4
Address	800113550301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_4
Address	800113560301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_4
Address	800113570301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_4
Address	8001135C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_4
Address	8001135D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_4
Address	800113600301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_4
Address	800113610301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_4
Address	800113620301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_4
Address	800113630301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_4
Address	800113640301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_4
Address	800113650301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_4
Address	800113660301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_4
Address	800113670301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_4
Address	800113680301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_4
Address	800113690301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_4
Address	8001136A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_4
Address	8001136B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field , determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_4
Address	8001137C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP3_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_4
Address	8001137D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP3_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY01.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_4
Address	8001137E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR0
Address	800140000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR0_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR0_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR0
Address	800140010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P1_ADR0
Address	800140040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P1_ADR0_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P1_ADR0_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P1_ADR0
Address	800140050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P1_ADR0_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P1_ADR0_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P1_ADR0
Address	800140060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY2_P1_ADR0_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P1_ADR0_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P1_ADR0
Address	800140070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P1_ADR0_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P1_ADR0_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 4***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P1_ADR0
Address	800140080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P1_ADR0_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P1_ADR0_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P1_ADR0
Address	800140090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P1_ADR0_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P1_ADR0_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P1_ADR0
Address	8001400A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY6_P1_ADR0_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P1_ADR0_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P1_ADR0
Address	8001400B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY7_P1_ADR0_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P1_ADR0_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR0
Address	8001400C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR0
Address	8001401A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	***ADR I/O FET Slice Enable Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR0
Address	800140200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR0
Address	800140210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0
Address	8001402A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0
Address	8001402B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR0
Address	8001402C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR0_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR0_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR1
Address	800144000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR1_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR1_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR1
Address	800144010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P1_ADR1
Address	800144040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P1_ADR1_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P1_ADR1_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P1_ADR1
Address	800144050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P1_ADR1_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P1_ADR1_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P1_ADR1
Address	800144060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY2_P1_ADR1_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P1_ADR1_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P1_ADR1
Address	800144070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P1_ADR1_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P1_ADR1_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 4***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P1_ADR1
Address	800144080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P1_ADR1_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P1_ADR1_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P1_ADR1
Address	800144090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P1_ADR1_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P1_ADR1_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P1_ADR1
Address	8001440A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY6_P1_ADR1_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P1_ADR1_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P1_ADR1
Address	8001440B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY7_P1_ADR1_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P1_ADR1_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR1
Address	8001440C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	*ADR I/O Slew Control Value*
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR1
Address	8001441A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR1
Address	800144200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR1
Address	800144210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1
Address	8001442A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1
Address	8001442B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	*ADR Power Down 2*
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR1
Address	8001442C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR1_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR1_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	*ADR Bit Enable*
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR2
Address	800148000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR2_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR2_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	*ADR Differential Pair Enable*
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR2
Address	800148010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P1_ADR2
Address	800148040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P1_ADR2_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P1_ADR2_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P1_ADR2
Address	800148050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P1_ADR2_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P1_ADR2_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P1_ADR2
Address	800148060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY2_P1_ADR2_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P1_ADR2_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P1_ADR2
Address	800148070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P1_ADR2_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P1_ADR2_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 4***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P1_ADR2
Address	800148080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P1_ADR2_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P1_ADR2_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P1_ADR2
Address	800148090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P1_ADR2_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P1_ADR2_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P1_ADR2
Address	8001480A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY6_P1_ADR2_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P1_ADR2_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P1_ADR2
Address	8001480B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY7_P1_ADR2_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P1_ADR2_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR2
Address	8001480C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	*ADR I/O Slew Control Value*
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR2
Address	8001481A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR2
Address	800148200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR2
Address	800148210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2
Address	8001482A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2
Address	8001482B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR2
Address	8001482C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR2_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR2_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY01.DDRPHY_ADR_BIT_ENABLE_P1_ADR3
Address	80014C000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR3_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR3_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY01.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR3
Address	80014C010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	*ADR Delay Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY0_P1_ADR3
Address	80014C040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P1_ADR3_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P1_ADR3_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY1_P1_ADR3
Address	80014C050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P1_ADR3_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P1_ADR3_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 2*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY2_P1_ADR3
Address	80014C060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY2_P1_ADR3_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P1_ADR3_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY3_P1_ADR3
Address	80014C070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P1_ADR3_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P1_ADR3_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 4***
Mnemonic	DPHY01.DDRPHY_ADR_DELAY4_P1_ADR3
Address	80014C080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P1_ADR3_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P1_ADR3_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY5_P1_ADR3
Address	80014C090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P1_ADR3_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P1_ADR3_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY6_P1_ADR3
Address	80014C0A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY6_P1_ADR3_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P1_ADR3_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY01.DDRPHY_ADR_DELAY7_P1_ADR3
Address	80014C0B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY7_P1_ADR3_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P1_ADR3_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY01.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR3
Address	80014C0C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.

Bits	SCOM	Field Mnemonic: Description
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	*ADR I/O Slew Control Value*
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR3
Address	80014C1A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR3
Address	80014C200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR I/O FET Slice Enable Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR3
Address	80014C210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3
Address	80014C2A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY01.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3
Address	80014C2B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY01.DDRPHY_ADR_POWERDOWN_2_P1_ADR3
Address	80014C2C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR3_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR3_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S0
Address	800180300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***ADR PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S0
Address	800180310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S0
Address	800180320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field are asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.

Bits	SCOM	Field Mnemonic: Description
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S0
Address	800180330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	***ADR SysClk Phase Rotator Value***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S0
Address	800180340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.

Bits	SCOM	Field Mnemonic: Description
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field .
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	***ADR Output Driver Force And ATEST Control***
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S0
Address	800180350301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_FORCE_EN: Output Force Enable Bit.
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	***ADR Output Driver Force Value 0***
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S0
Address	800180360301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Output Driver Force Value 1***
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S0
Address	800180370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Slew Calibration Control***
Mnemonic	DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S0
Address	800180390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	

Bits	SCOM	Field Mnemonic: Description
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	***ADR PLL/VREG Configuration 0***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S1
Address	800184300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***ADR PLL/VREG Configuration 1***
Mnemonic	DPHY01.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S1
Address	800184310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S1
Address	800184320301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field are asserted. '1'b - Selects the sticky lock to the BB_LOCK field . The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY01.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S1
Address	800184330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	***ADR SysClk Phase Rotator Value***
Mnemonic	DPHY01.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S1
Address	800184340301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field .
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	*ADR Output Driver Force And ATEST Control*
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S1
Address	800184350301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_FORCE_EN: Output Force Enable Bit.
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	*ADR Output Driver Force Value 0*
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S1
Address	800184360301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Output Driver Force Value 1*
Mnemonic	DPHY01.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S1
Address	800184370301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Slew Calibration Control*
Mnemonic	DPHY01.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S1
Address	800184390301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	*PC DP18 PLL Lock Status*
Mnemonic	DPHY01.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P1
Address	8001C0000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:62	ROX	DDRPHY_PC_DP18_PLL_LOCK_STATUS_P1_DP18_PLL_LOCK: One bit for each DP18 in the DDR PHY Core. When the core contains less than 15 DP18s, then bits with an index value greater than NUM_DP18 - 1 are reserved. '0'b - PLL in the bit indexed DP18 is not locked. '1'b - PLL in the bit indexed DP18 is locked. When the PHY is configured in TDM Mode, this register reports the PLL Lock Status of all the DP18s in the PHY.
63	RO	constant=0b0

Register Name	*PC AD32S PLL Lock Status*
Mnemonic	DPHY01.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P1
Address	8001C0010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	ROX	DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P1_AD32S_PLL_LOCK: One bit for each ADR Support Block in the DDR PHY Core. When the core contains less than 2 AD32Ss, bits with an index value greater than NUM_AD32S-1 are reserved. '0'b - PLL in the bit indexed AD32S is not locked. '1'b - PLL in the bit indexed AD32S is locked.
50:63	RO	constant=0b00000000000000

Register Name	*PC Rank Pair 0*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR0_P1
Address	8001C0020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_PRI: Primary Rank of Rank Pair 0 When configured for a protocol that only supports a single rank system, this field must be set to 0.
51	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_PRI_V: Value in the RANK_PAIR0_PRI field is valid
52:54	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_SEC: Secondary Rank of Rank Pair 0
55	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_SEC_V: Value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_PRI: Primary Rank of Rank Pair 1
59	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_PRI_V: Value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_SEC: Secondary Rank of Rank Pair 1
63	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_SEC_V: Value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	*PC Rank Pair 1*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR1_P1
Address	8001C0030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_PRI: Primary Rank of Rank Pair 2

Bits	SCOM	Field Mnemonic: Description
51	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_PRI_V: Value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the register defined in.
52:54	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_SEC: Secondary Rank of Rank Pair 2
55	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_SEC_V: Value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_PRI: Primary Rank of Rank Pair 3
59	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_PRI_V: Value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_SEC: Secondary Rank of Rank Pair 3
63	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_SEC_V: Value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	***PC Periodic Base Counter 0***
Mnemonic	DPHY01.DDRPHY_PC_BASE_CNTR0_P1
Address	8001C0040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_BASE_CNTR0_P1_PERIODIC_BASE_CNTR0: Periodic Base Counter 0. When enabled via PERIODIC_CAL_REQ_EN , counter is free running (counts every dphy_nclk clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & '0'} from the register.

Register Name	***PC Periodic Reload Value 0***
Mnemonic	DPHY01.DDRPHY_PC_RELOAD_VALUE0_P1
Address	8001C0050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RELOAD_VALUE0_P1_PERIODIC_CAL_REQ_EN: '1'b - Enable Periodic Calibration request generation from the PHY. '0'b - Disable Periodic Calibration request generation from the PHY.
49:63	RW	DDRPHY_PC_RELOAD_VALUE0_P1_PERIODIC_RELOAD_VALUE0: Periodic Reload Value 0. This value is loaded into bits 0 through 14 of the when it rolls over. Bit 15 is always loaded with '0'b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to '1'b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	*PC Periodic Base Counter 1*
Mnemonic	DPHY01.DDRPHY_PC_BASE_CNTR1_P1
Address	8001C0060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_BASE_CNTR1_P1_PERIODIC_BASE_CNTR1: Periodic Base Counter 1. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set , it is reloaded with the value 'FFFF'h. This register enables the and the every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set , it is reloaded with the value '00FF'h. When the FAST_SIM_PER_CNTR bit is set , this register enables and the every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer*
Mnemonic	DPHY01.DDRPHY_PC_CAL_TIMER_P1
Address	8001C0070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_CAL_TIMER_P1_PERIODIC_CAL_TIMER: Periodic Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_TIMER_RELOAD_VALUE from the register. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set , this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer Reload Value*
Mnemonic	DPHY01.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1
Address	8001C0080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1_PERIODIC_TIMER_RELOAD_VALUE: Periodic Reload Value 0. This value is loaded into the when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Impedance Calibration Timer*
Mnemonic	DPHY01.DDRPHY_PC_ZCAL_TIMER_P1
Address	8001C0090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_ZCAL_TIMER_P1_PERIODIC_ZCAL_TIMER: Periodic Impedance Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the register. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set , this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Impedance Calibration Timer Reload Value*
Mnemonic	DPHY01.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1
Address	8001C00A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1_PERIODIC_TIMER_RELOAD_VALUE: Periodic Impedance Calibration Timer Reload Value. This value is loaded into the when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Calibration Configuration*
Mnemonic	DPHY01.DDRPHY_PC_PER_CAL_CONFIG_P1
Address	8001C00B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_ENA_RANK_PAIR: '1'b indicates periodic calibration is enabled '0'b indicates periodic calibration is disabled Bit 0 contains the enable bit for rank pair 0Bit 1 contains the enable bit for rank pair 1Bit 2 contains the enable bit for rank pair 2Bit 3 contains the enable bit for rank pair 3
52	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_ENA_ZCAL: Enables the periodic impedance calibration logic.
53	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SysClk with the Memory Controller Clock (dphy_nclkSysClk Alignment).
54	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ENA_PER_READ_CTR: '1'b - Enable the updating of the registers during periodic read centering. '0'b - Prevent the updating of the registers during periodic read centering.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ENA_PER_RDCLK_ALIGN: '1'b - Enable the updating of the register at the conclusion of periodic read centering on a nibble of DQ lanes. '0'b - Prevent the updating of the register at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS Alignment).
57:58	RWX	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.
59	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_FAST_SIM_PER_CNTR: This bit must be '0'b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. '1'b causes the register to roll over to '00FF'h. '0'b has no effect on the behavior of the register .
60	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_START_INIT_CAL: When this bit is written to '1'b, the DDR PHY initiates an initial calibration for all ranks enabled in the register defined in. When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_START_PER_CAL: When this bit is written to '1'b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ABORT_ON_ERR_EN: Periodic Calibration Abort on Error Enable. '1'b - Enable the detection of the pc_errn_in. '0'b - Disable the detection of the pc_errn_in.
63	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ZCAL_UPDATE_MODE: Reserved. See PC Config 0 ZCAL_NOT_CONT bit.

Register Name	*PC Configuration 0*
Mnemonic	DPHY01.DDRPHY_PC_CONFIG0_P1
Address	8001C00C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG0_P1_PROTOCOL: Values: DDR3=>0b0000 DDR4=>0b0001 RLDRAM2_CIO=>0b0010
52	RW	DDRPHY_PC_CONFIG0_P1_DATA_MUX4_1MODE: Data Multiplexer Mode 4:1 Enable. '0'b - Data Multiplexer Mode is 2:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) is two times as wide as the data and control signals (pins) on the Memory Interface (MEMINT) Interface. '1'b - Data Multiplexer Mode is 4:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to one half of the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) are four times as wide as the data and control signals (pins) on the Memory Interface (MEMINT Interface).
53	RW	DDRPHY_PC_CONFIG0_P1_SPAM_EN: '1'b - The PC only snoops read and write commands for primary ranks of each rank pair (that is, reads and writes to secondary ranks are ignored). '0'b - Split Access Mode is not enabled.
54	RW	DDRPHY_PC_CONFIG0_P1_DDR4_CMD_SIG_REDUCTION: Values: DDR3=>0b0 DDR4=>0b1

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_PC_CONFIG0_P1_SYSCLK_2X_MEMINTCLKO: Always write this bit to '0'b. This function is not supported. '0'b - The internal SysClk frequency equals the MEMINTCLKO (memory interface clock) frequency. '1'b - The internal SysClk frequency is 2* the MEMINTCLKO (memory interface clock) frequency. Support of this function requires this register to be written during the reset sequence when the PLL values are configured.
56	RW	DDRPHY_PC_CONFIG0_P1_RANK_OVERRIDE: Rank Override Mode '0'b - The DDR PHY uses the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface to determine the rank pair and hence the configuration registers for each read or write command. '1'b - The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all readwrite commands regardless of the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface. When this bit is '1'b, the following assumptions/restrictions apply:
57:59	RW	DDRPHY_PC_CONFIG0_P1_RANK_OVERRIDE_VALUE: Rank Override Value
60	RW	DDRPHY_PC_CONFIG0_P1_LOW_LATENCY: '1'b - Force Early Read Start Mode (ERS Mode) off. '0'b - ERS Mode on/off determined by CL value. When CL = 5 or 6, ERS Mode is automatically off. Otherwise, ERS Mode is automatically on.
61	RW	
62	RW	DDRPHY_PC_CONFIG0_P1_DDR4_VLEVEL_BANK_GROUP: In DDR4: '1'b - enable Voltage Level and Bank Group Arch(DDR4 ballot 1716.23). '0'b - disable Voltage Level and Bank Group Arch. For all other protocols, this bit must be '0'b.
63	RW	DDRPHY_PC_CONFIG0_P1_ZCAL_NOT_CONT: '1'b - IO PVT values are only updated when an internal ZQ cal is requested. '0'b - IO PVT values are updated continuously.

Register Name	*PC Configuration 1*
Mnemonic	DPHY01.DDRPHY_PC_CONFIG1_P1
Address	8001C00D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG1_P1_WRITE_LATENCY_OFFSET: Write Latency Offset (WLO) is used to adjust the delay through the internal write command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipelining latches are added. This value is twos compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path.
52:55	RW	DDRPHY_PC_CONFIG1_P1_READ_LATENCY_OFFSET: Read Latency Offset (RLO) is used to adjust the delay through the internal read command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipelining latches are added. This value is two's compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path. The value for this field must be: RLO less than equal min{Round Down(System_Delay)} System_Delay and min{Round Down(System_Delay)} is defined in the GLOBAL_PHY_OFFSET field description .
56	RW	DDRPHY_PC_CONFIG1_P1_MEMCTL_CIC_FAST: '0'b - mettle_cc_o is deasserted ('0'b) in response to mettle_cis_i being asserted ('1'b) and remains deasserted until the calibration completes. '1'b - mettle_cic_o is deasserted ('0'b) in response to mettle_cis_i being asserted ('1'b) and is asserted ('1'b) in response to mettle_cis_i being deasserted ('0'b).
57	RW	DDRPHY_PC_CONFIG1_P1_MEMCTL_CTRN_IGNORE: '0'b - DDR PHY responds to the mettle_ctr_i input. '1'b - DDR PHY does not respond to the mettle_ctr_i input. The mettle_ctr_i input value is a 'don't care'.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_PC_CONFIG1_P1_DISABLE_MEMCTL_CAL: Reserved. This bit must be '0'b. When set to '1'b, the DFI request ac handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.
59:61	RW	DDRPHY_PC_CONFIG1_P1_MEMORY_TYPE: '001'b - DDR3 RDIMM '011'b - DDR3 LRDIMM '101'b - DDR4 RDIMM '111'b - DDR4 LRDIMM Other values are reserved.
62	RW	DDRPHY_PC_CONFIG1_P1_DDR4_LATENCY_SW: DDR4 Latency Debug Switch. Should be '1'b for normal operation.
63	RW	DDRPHY_PC_CONFIG1_P1_RETRAIN_PERCAL_SW: Retrain Parcel Debug Switch. Affects behavior of mettle_cup_o during periodic read calibrations. '0'b - rank is requested rank and may not be the rank that was executed. '1'b - rank is next rank that requires calibration.

Register Name	*PC Resets*
Mnemonic	DPHY01.DDRPHY_PC_RESETS_P1
Address	8001C00E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RESETS_P1_PLL_RESET: '1'b - Resets the Internal PLLs
49	RW	DDRPHY_PC_RESETS_P1_SYSCLK_RESET: '1'b - Reset all logic in the internal systolic domain.
50:63	RO	constant=0b00000000000000

Register Name	*PC Periodic Z-Cal Configuration*
Mnemonic	DPHY01.DDRPHY_PC_PER_ZCAL_CONFIG_P1
Address	8001C00F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P1_PER_ZCAL_ENA_RANK: '1'b indicates periodic external impedance calibration is enabled '0'b indicates periodic external impedance calibration is disabled Bit 0 contains the enable bit for rank 0Bit 1 contains the enable bit for rank 1Bit 2 contains the enable bit for rank 2Bit 3 contains the enable bit for rank 3Bit 4 contains the enable bit for rank 4Bit 5 contains the enable bit for rank 5Bit 6 contains the enable bit for rank 6Bit 7 contains the enable bit for rank 7
56:58	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P1_PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 next rank scheduled to run z cal001 = rank_1 next rank scheduled to run z cal010 = rank_2 next rank scheduled to run z cal011 = rank_3 next rank scheduled to run z cal100 = rank_4 next rank scheduled to run z cal101 = rank_5 next rank scheduled to run z cal110 = rank_6 next rank scheduled to run z cal111 = rank_7 next rank scheduled to run z cal
59	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P1_START_PER_ZCAL: When this bit is written to '1'b, the DDR PHY initiate a single periodic impedance calibration (equivalent to a periodic z cal timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	constant=0b0000

Register Name	*PC Power Down 1*
Mnemonic	DPHY01.DDRPHY_PC_POWERDOWN_1_P1
Address	8001C0100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_POWERDOWN_1_P1_MASTER_PD_CNTL: Master Power down Control '0'b - DDR port is in functional mode regardless of PDR1 bits {1:15} '1'b - Power down status of DDR port is determined by PDR bits {1:15}
49	RW	DDRPHY_PC_POWERDOWN_1_P1_ANALOG_INPUT_STAB2: Analog Input Stabilization #2 (Separate from bit 7 to allow for separation of behavior in PDS3) '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
50	RW	DDRPHY_PC_POWERDOWN_1_P1_EYEDAC_PD: EYEDAC power down '0'b - EYEDAC controlled by functional mode register '1'b - EYEDAC powered down
51	RW	DDRPHY_PC_POWERDOWN_1_P1_PHYTOP_CLK_GATE: Reserved.
52	RW	DDRPHY_PC_POWERDOWN_1_P1_EXT_VREF_PD: External VREF Power down '0'b - Functional Mode control of External VREF Drivers '1'b - External VREF Drivers Powered Down
53	RW	DDRPHY_PC_POWERDOWN_1_P1_RESET_STAB: RESET# Stabilization '0'b - Functional Mode Control of RESET# PHY IO '1'b - Power down Stabilization of RESET# Signals
54	RW	DDRPHY_PC_POWERDOWN_1_P1_ANALOG_OUTPUT_STAB: Analog Output Stabilization '0'b - Functional Mode Control of Analog Outputs '1'b - Analog Outputs Forced to Known Values Immediately on Digital Side of Boundary
55	RW	DDRPHY_PC_POWERDOWN_1_P1_ANALOG_INPUT_STAB1: Analog Input Stabilization #1 '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
56	RW	DDRPHY_PC_POWERDOWN_1_P1_SYSCLK_CLK_GATE: Reserved.
57	RW	DDRPHY_PC_POWERDOWN_1_P1_DELAY_LINE_CTL_OVERRIDE: '0'b - DP18 Delay Line Power Control register is read only and is updated by hardware. '1'b - DP18 Delay Line Power Control register is read/write and is not updated by hardware.
58	RW	DDRPHY_PC_POWERDOWN_1_P1_WR_FIFO_STAB: Write FIFO & Logic Circuit Stabilization '0'b - Write FIFO and Logic Circuits under Functional Control '1'b - Write FIFO clock disabled, Flush mode set
59	RW	DDRPHY_PC_POWERDOWN_1_P1_ADR_RX_PD: Reserved.
60:61	RW	DDRPHY_PC_POWERDOWN_1_P1_DP18_RX_PD: DP18 Receiver Power down Control '00'b - Functional Mode Control of DP Receivers '01'b - DP Receivers in Standby Mode (RG) '10'b - Reserved. '11'b - DP Receivers in Low Power Mode (RE)
62	RW	DDRPHY_PC_POWERDOWN_1_P1_TX_TRISTATE_CNTL: Driver Tristan Control '0'b - Functional Mode Control of Drivers '1'b - DP18 Drivers in Tristan, ADR Drivers selectively either in Tristan or Pull down under control of PDR2 For the ADR12 and ADR16 cores, this bit operates in conjunction with the register to determine the state of the IO during power down
63	RW	DDRPHY_PC_POWERDOWN_1_P1_VCC_REG_PD: VCC Domain Regulation Power down '0'b - Functional Mode: VCC Voltage Regulators are on '1'b - Power down Mode: Voltage Regulators powered down, VCC=0v

Register Name	*PC Rank Group*
Mnemonic	DPHY01.DDRPHY_PC_RANK_GROUP_P1
Address	8001C0110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP0_PRI: '1'b - Enable Address Mirroring Rank Pair 0 Primary
49	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP0_SEC: '1'b - Enable Address Mirroring Rank Pair 0 Secondary
50	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP1_PRI: '1'b - Enable Address Mirroring Rank Pair 1 Primary
51	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP1_SEC: '1'b - Enable Address Mirroring Rank Pair 1 Secondary
52	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP2_PRI: '1'b - Enable Address Mirroring Rank Pair 2 Primary
53	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP2_SEC: '1'b - Enable Address Mirroring Rank Pair 2 Secondary
54	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP3_PRI: '1'b - Enable Address Mirroring Rank Pair 3 Primary
55	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP3_SEC: '1'b - Enable Address Mirroring Rank Pair 3 Secondary
56:57	RW	DDRPHY_PC_RANK_GROUP_P1_RANK_GROUPING: Reserved.
58	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A3_A4: '1'b - mirror A3 & A4 signals on mirrored ranks.
59	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A5_A6: '1'b - mirror A5 & A6 signals on mirrored ranks.
60	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A7_A8: '1'b - mirror A7 & A8 signals on mirrored ranks.
61	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A11_A13: '1'b - mirror A11 & A13 signals on mirrored ranks.
62	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_BA0_BA1: '1'b - mirror BA0 & BA1 signals on mirrored ranks.
63	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_BG0_BG1: '1'b - mirror BG0 & BG1 signals on mirrored ranks.

Register Name	*PC Error Status 0*
Mnemonic	DPHY01.DDRPHY_PC_ERROR_STATUS0_P1
Address	8001C0120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_ERROR_STATUS0_P1_RC_ERROR: '1'b - Error in Read Control logic.

Bits	SCOM	Field Mnemonic: Description
49	ROX	DDRPHY_PC_ERROR_STATUS0_P1_WC_ERROR: '1'b - Error in Write Control logic.
50	ROX	DDRPHY_PC_ERROR_STATUS0_P1_SEQ_ERROR: '1'b - Error in Sequencer Control logic.
51	ROX	DDRPHY_PC_ERROR_STATUS0_P1_CC_ERROR: Reserved.
52	ROX	DDRPHY_PC_ERROR_STATUS0_P1_APB_ERROR: '1'b - Error in Register interface logic.
53	ROX	DDRPHY_PC_ERROR_STATUS0_P1_PC_ERROR: '1'b - Error in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	*PC Error Mask 0*
Mnemonic	DPHY01.DDRPHY_PC_ERROR_MASK0_P1
Address	8001C0130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_ERROR_MASK0_P1_RC_ERROR_MASK: '1'b - Mask errors in Read Control logic.
49	RW	DDRPHY_PC_ERROR_MASK0_P1_WC_ERROR_MASK: '1'b - Mask errors in Write Control logic.
50	RW	DDRPHY_PC_ERROR_MASK0_P1_SEQ_ERROR_MASK: '1'b - Mask errors in Sequencer Control logic.
51	RW	DDRPHY_PC_ERROR_MASK0_P1_CC_ERROR_MASK: Reserved.
52	RW	DDRPHY_PC_ERROR_MASK0_P1_APB_ERROR_MASK: '1'b - Mask errors in Register Interface logic.
53	RW	DDRPHY_PC_ERROR_MASK0_P1_PC_ERROR_MASK: '1'b - Mask errors in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	*PC IO PVT N/P FET Driver Control*
Mnemonic	DPHY01.DDRPHY_PC_IO_PVT_FET_CONTROL_P1
Address	8001C0140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_PVTP: PFET Driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
53:57	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_PVTN: NFET Driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
58	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_PVT_OVERRIDE: '1'b - All drivers are updated with the PVTP and PVTN values in this register immediately. '0'b - All drivers are updated with the PVTP and PVTN values from the impedance calibration state machine.
59	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_ENABLE_ZCAL: '1'b - Enable Impedance Controller. '0'b - Disable Impedance Controller.
60	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_RESET_ZCAL: Reset Impedance Controller. The value of this field is driven to the Clint_reset_o output for optional connection to the reset of an Impedance Controller.

Bits	SCOM	Field Mnemonic: Description
61:63	RO	constant=0b000

Register Name	*PC VREF Driver Control*
Mnemonic	DPHY01.DDRPHY_PC_VREF_DRV_CONTROL_P1
Address	8001C0150301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ0DSGN: VREF sign bit enable. This value is driven to the vrefdq0_dsign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
49:52	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ0D: VREF bit enables. This value is driven to the vrefdq0_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
53	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ1DSGN: VREF sign bit enable. This value is driven to the vrefdq1_dsign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
54:57	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ1D: VREF bit enables. This value is driven to the vrefdq1_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
58:63	RO	constant=0b000000

Register Name	*PC Initial Calibration Config0*
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_CONFIG0_P1
Address	8001C0160301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_WR_LEVEL: Enable Write Leveling during initial calibration
49	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_INITIAL_PAT_WR: Enable Initial Pattern Write during initial calibration. This bit must be set when performing Read Centering or Write Centering on memory devices that do not generate an MPR pattern. This bit must be set when performing Custom Read Centering or Custom Write Centering. If Custom Read Centering or Custom Write Centering was performed, an Initial Pattern Write of '5555' hex, the reset value of the SEQ Read/Write Data0-1 registers, must be performed before any periodic calibration routines are performed.
50	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_RDCLK_ALIGN: Enable the alignment of the internal SysClk to the Read clock during initial calibration. This calibration step requires the DQS (read) Alignment calibration step to have been performed.
52	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_READ_CTR: Enable Read Centering during initial calibration. This calibration step requires the SysClk to Read Clock alignment to have been performed.
53	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_WRITE_CTR: Enable Write Centering during initial calibration. This calibration step requires the Read Centering calibration step to have been performed.

Bits	SCOM	Field Mnemonic: Description
54	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_INITIAL_COARSE_WR: Enable Initial Coarse Pattern Write during initial calibration. This calibration step requires the Write Centering calibration step to have been performed.
55	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_COARSE_RD: Enable Coarse Read Centering during initial calibration. This calibration step requires the Initial Coarse Pattern Write calibration step to have been performed.
56	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0, 2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation
57	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0,2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation.
58	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes.
59	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_RANK_PAIR: Enable Rank Pair ('1'b = Enabled, '0'b = disabled) Bit 12 contains the enable for rank pair 0.Bit 13 contains the enable for rank pair 1.Bit 14 contains the enable for rank pair 2.Bit 15 contains the enable for rank pair 3.

Register Name	***PC Initial Calibration Config1***
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_CONFIG1_P1
Address	8001C0170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_COUNT: Refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: '00'b: Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. '01'b: Use the internal Refresh Interval timer to determine when refresh commands are sent; allow refreshes to occur between calibration routines. '10'b: Reserved '11'b: Use the internal Refresh Interval timer to determine when refresh commands should be sent; in addition to allowing refreshes commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_ALL_RANKS: '1'b Indicates that all ranks should be refreshed during initial calibration. When a refresh is generated by the DDR PHY all of the chip selects are asserted at the same time during one refresh command. '0'b indicates only the rank currently being calibrated should be refreshed. When a refresh is generated by the DDR PHY, only the chip select of the rank being calibrated are asserted during the refresh command.
55:56	RW	

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_INTERVAL: Refresh Interval - This value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (min. value) = 256 MEMINTCLKO cycles between refreshes 1111111 (max value) = 32512 MEMINTCLKO cycle between refreshes For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 ('0011000'b) provides a tREFI setting of 7.68 us (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 us).The minimum value for this field is 6. If a value less than 6 is written to this field, this field will be set to 6 by hardware. When the Refresh Interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes will be issued and the internal counter will be decremented to zero. The internal pending refresh counter is a 4 bit counter with a maximum value of '15'd. An error bit will be set in the register if the internal pending refresh counter overflows.

Register Name	***PC Initial Calibration Error***
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_ERROR_P1
Address	8001C0180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_WR_LEVEL: Write leveling error occurred during initial calibration.
49	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_INITIAL_PAT_WRITE: Initial Pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
50	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_DQS_ALIGN: DQS Alignment error occurred during initial calibration.
51	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_RDCLK_ALIGN: RDCLK to SysClk alignment error occurred during initial calibration.
52	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_READ_CTR: Read centering error occurred during initial calibration.
53	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_WRITE_CTR: Write centering error occurred during initial calibration.
54	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_INITIAL_COARSE_WR: Initial Coarse Pattern Write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
55	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_COARSE_RD: Coarse read centering error occurred during initial calibration.
56	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_CUSTOM_RD: Custom pattern read centering error occurred during initial calibration.
57	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_CUSTOM_WR: Custom pattern write centering error occurred during initial calibration.
58	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_DIGITAL_EYE: Digital eye error occurred during initial calibration.
59	RO	constant=0b0
60:63	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 12 reflects the status of rank pair 0.Bit 13 reflects the status of rank pair 1.Bit 14 reflects the status of rank pair 2.Bit 15 reflects the status of rank pair 3.

Register Name	*PC Initial Calibration Status*
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_STATUS_P1
Address	8001C0190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	ROX	DDRPHY_PC_INIT_CAL_STATUS_P1_INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration, '1'b indicates the rank pair has completed an initial calibration sequence. bit 0 reflects the status of rank pair 0bit 1 reflects the status of rank pair 1bit 2 reflects the status of rank pair 2bit 3 reflects the status of rank pair 3
52:56	ROX	
57	ROX	DDRPHY_PC_INIT_CAL_STATUS_P1_PER_CAL_ABORT: Reserved. This reserved field might contain information that is helpful for hardware debugging. Do not assume that it is read as zeros. Periodic Calibration Abort. Read Only. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress and the ABORT_ON_ERR_EN bit is set . This bit is reset at the start of every new calibration.
58:63	ROX	

Register Name	*PC Initial Calibration Mask*
Mnemonic	DPHY01.DDRPHY_PC_INIT_CAL_MASK_P1
Address	8001C01A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_WR_LEVEL_MASK: Mask Write leveling error
49	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_INITIAL_PAT_WRITE_MASK: Mask Initial Pattern write error
50	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_DQS_ALIGN_MASK: Mask DQS Alignment error
51	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_RDCLK_ALIGN_MASK: Mask RDCLK to SysClk alignment error
52	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_READ_CTR_MASK: Mask Read centering error
53	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_WRITE_CTR_MASK: Mask Write centering error
54	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_INITIAL_COARSE_WR_MASK: Mask Initial Coarse Pattern Write centering error
55	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_COARSE_RD_MASK: Mask Coarse read centering error
56	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_CUSTOM_RD_MASK: Mask Custom pattern read centering error
57	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_CUSTOM_WR_MASK: Mask Custom pattern write centering error
58	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_DIGITAL_EYE_MASK: Mask Digital Eye error
59:63	RO	constant=0b00000

Register Name	*PC IO PVT N/P FET Driver Status*
Mnemonic	DPHY01.DDRPHY_PC_IO_PVT_FET_STATUS_P1
Address	8001C01B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P1_PVTP: PFET Driver PVTP value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.
53:57	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P1_PVTN: NFET Driver PVTN value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.
58:63	RO	constant=0b000000

Register Name	*PC Mode 0 Primary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP0_P1
Address	8001C01C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP0_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP0_P1
Address	8001C01D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP0_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP0_P1
Address	8001C01E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_PC_MR2_PRI_RP0_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	***PC Mode 3 Primary RP0***
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP0_P1
Address	8001C01F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP0_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	***PC Mode 0 Secondary RP0***
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP0_P1
Address	8001C0200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP0_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP0***
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP0_P1
Address	8001C0210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP0_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP0_P1
Address	8001C0220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP0_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP0*
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP0_P1
Address	8001C0230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP0_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Rank Pair 2*
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR2_P1
Address	8001C0300301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_TER: Tertiary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_TER_V: Value in the RANK_PAIR0_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_QUA: Quaternary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_QUA_V: Value in the RANK_PAIR0_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_TER: Tertiary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_TER_V: Value in the RANK_PAIR1_TER field is valid.

Bits	SCOM	Field Mnemonic: Description
60:62	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_QUA: Quaternary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_QUA_V: Value in the RANK_PAIR1_QUA field is valid.

Register Name	***PC Rank Pair 3***
Mnemonic	DPHY01.DDRPHY_PC_RANK_PAIR3_P1
Address	8001C0310301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_TER: Tertiary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_TER_V: Value in the RANK_PAIR2_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_QUA: Quaternary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_QUA_V: Value in the RANK_PAIR2_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_TER: Tertiary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_TER_V: Value in the RANK_PAIR3_TER field is valid.
60:62	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_QUA: Quaternary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_QUA_V: Value in the RANK_PAIR3_QUA field is valid.

Register Name	***PC Chip Select ID Configuration***
Mnemonic	DPHY01.DDRPHY_PC_CSID_CFG_P1
Address	8001C0330301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_CSID_CFG_P1_CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair registers, then CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
49	RW	DDRPHY_PC_CSID_CFG_P1_CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair registers, then CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
50	RW	DDRPHY_PC_CSID_CFG_P1_CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair registers, then CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
51	RW	DDRPHY_PC_CSID_CFG_P1_CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair registers, then CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_PC_CSID_CFG_P1_CS4_INIT_CAL_VALUE: If CS4 is not selected by any of the Rank Pair registers, then CS4 is driven to this value during initial calibration. If CS4 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
53	RW	DDRPHY_PC_CSID_CFG_P1_CS5_INIT_CAL_VALUE: If CS5 is not selected by any of the Rank Pair registers, then CS5 is driven to this value during initial calibration. If CS5 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
54	RW	DDRPHY_PC_CSID_CFG_P1_CS6_INIT_CAL_VALUE: If CS6 is not selected by any of the Rank Pair registers, then CS6 is driven to this value during initial calibration. If CS6 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
55	RW	DDRPHY_PC_CSID_CFG_P1_CS7_INIT_CAL_VALUE: If CS7 is not selected by any of the Rank Pair registers, then CS7 is driven to this value during initial calibration. If CS7 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
56:63	RO	constant=0b00000000

Register Name	***PC Rank Group Extension***
Mnemonic	DPHY01.DDRPHY_PC_RANK_GROUP_EXT_P1
Address	8001C0350301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP0_TER: '1'b - Enable Address Mirroring Rank Pair 0 Tertiary
49	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP0_QUA: '1'b - Enable Address Mirroring Rank Pair 0 Quaternary
50	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP1_TER: '1'b - Enable Address Mirroring Rank Pair 1 Tertiary
51	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP1_QUA: '1'b - Enable Address Mirroring Rank Pair 1 Quaternary
52	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP2_TER: '1'b - Enable Address Mirroring Rank Pair 2 Tertiary
53	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP2_QUA: '1'b - Enable Address Mirroring Rank Pair 2 Quaternary
54	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP3_TER: '1'b - Enable Address Mirroring Rank Pair 3 Tertiary
55	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP3_QUA: '1'b - Enable Address Mirroring Rank Pair 3 Quaternary
56:63	RO	constant=0b00000000

Register Name	***PC Mode 0 Primary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP1_P1
Address	8001C11C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP1_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP1_P1
Address	8001C11D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP1_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP1_P1
Address	8001C11E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP1_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP1_P1
Address	8001C11F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP1_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP1*
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP1_P1
Address	8001C1200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP1_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP1_P1
Address	8001C1210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP1_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP1_P1
Address	8001C1220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP1_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP1***
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP1_P1
Address	8001C1230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP1_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	***PC Mode 0 Primary RP2***
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP2_P1
Address	8001C21C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP2_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	***PC Mode 1 Primary RP2***
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP2_P1
Address	8001C21D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP2_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	***PC Mode 2 Primary RP2***
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP2_P1
Address	8001C21E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP2_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP2_P1
Address	8001C21F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP2_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP2_P1
Address	8001C2200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP2_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP2_P1
Address	8001C2210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP2_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP2_P1
Address	8001C2220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP2_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP2*
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP2_P1
Address	8001C2230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP2_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR0_PRI_RP3_P1
Address	8001C31C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP3_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR1_PRI_RP3_P1
Address	8001C31D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP3_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR2_PRI_RP3_P1
Address	8001C31E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP3_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR3_PRI_RP3_P1
Address	8001C31F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP3_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR0_SEC_RP3_P1
Address	8001C3200301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP3_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR1_SEC_RP3_P1
Address	8001C3210301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP3_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR2_SEC_RP3_P1
Address	8001C3220301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP3_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP3*
Mnemonic	DPHY01.DDRPHY_PC_MR3_SEC_RP3_P1
Address	8001C3230301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP3_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*SEQ Read/Write Data 0*
Mnemonic	DPHY01.DDRPHY_SEQ_RD_WR_DATA0_P1
Address	8001C4000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA0_P1_RD_WR_DATA_REG0: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0 are written to MPR0. - bits 8:15 of register 0 are written to MPR1. - bits 0:7 of register 1 are written to MPR2. - bits 8:15 of register 1 are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	*SEQ Read/Write Data 1*
Mnemonic	DPHY01.DDRPHY_SEQ_RD_WR_DATA1_P1
Address	8001C4010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA1_P1_RD_WR_DATA_REG1: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0 are written to MPR0. - bits 8:15 of register 0 are written to MPR1. - bits 0:7 of register 1 are written to MPR2. - bits 8:15 of register 1 are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	***SEQ Configuration 0***
Mnemonic	DPHY01.DDRPHY_SEQ_CONFIG0_P1
Address	8001C4020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_CONFIG0_P1_MPR_PATTERN_BIT: Read and write calibration algorithms are based on eight-beat bursts. This register controls the readwrite burst data pattern. For Write data: The MPR_PATTERN_BIT value is available on all bit lanes of beat 1, 3, 5 and 7 and the inverse of the MPR_PATTERN_BIT on all bit lanes of beat 2, 3, 6 and 8, ensuring all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For Read data: Bit 0 is brought out as output of Sequencer and DP18 composes the expected pattern from this output.
49	RW	DDRPHY_SEQ_CONFIG0_P1_TWO_CYCLE_ADDR_EN: DDR3 and DDR4: '1'b - During calibrations, the address and command are driven onto the addresscmd bus for two memory clock cycles while the appropriate chip selects are active only during the second memory clock cycle of the command. '0'b - During calibration, the address and command and chip selects are driven and active for one memory clock cycle. All other protocols: This bit must be set to '0'b. The address and command and chip selects are driven active for one memory clock cycle.
50:53	RW	DDRPHY_SEQ_CONFIG0_P1_MR_MASK_EN: Mode Register mask enable. This register masks, or disables, the mode register access by the calibration algorithms. Bits 0- 3 map to mode register 0 - 3.
54	RW	DDRPHY_SEQ_CONFIG0_P1_DELAYED_PAR: '0'b - DDR4 PAR signal is generated coincident with addresscommand signals during init cal '1'b - DDR4 PAR signal is generated one clock cycle later than addresscommand signals during init cal Bit applies to DDR4 only and is don't care for DDR3
55	RW	DDRPHY_SEQ_CONFIG0_P1_LRDIMM_CONTEXT: Value of context bit to be used during F[0]RC12 LRDIMM Control Word commands.
56	RW	DDRPHY_SEQ_CONFIG0_P1_FORCE_RESERVED: '0'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will use the DDR4 MPR registers. '1'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory. If the PROTOCOL field does not equal DDR4, this bit is not used and is a 'don't care'.
57	RW	DDRPHY_SEQ_CONFIG0_P1_HALT_ROTATION: '0'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will rotate through the use of all 4 MPR registers by changing BA[0:1] during the calibration. '1'b - When the PROTOCOL field equals DDR4, Custom Read Centering and Initial Pattern Write will set BA[0:1] = '00'b. The same 8 beats will be read repeatedly on a particular DQ lane and the expect data will not be rotated through the 4 bytes of the register every 8 beats. If the PROTOCOL field does not equal DDR4, this bit is not used and is a 'don't care'.
58	RW	DDRPHY_SEQ_CONFIG0_P1_FORCE_MPR: '0'b - When the PROTOCOL field equals DDR3, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory, allowing a custom 8 bit repeating pattern to be compared during read centering. '1'b - When the PROTOCOL field equals DDR3, Custom Read Centering and Initial Pattern Write will use 4 DRAM MPR registers, allowing Custom Read Centering to read the 4 MPR registers. This is not a mode described by the DDR3 JEDEC standard. If the PROTOCOL field does not equal DDR3, this bit is not used and is a 'don't care'.
59:63	RW	

Register Name	***SEQ Reserved Address 0***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR0_P1
Address	8001C4030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR0_P1_RESERVED_ADDR0: Reserved Address Field 0. Exact definition is protocol dependent DDR3DDR4: Bits 0-15 map to A0-A15. The lower 2 bytes of row address are used. RLDRAM2RLDRAM3: Bits 0-15 map to A0-A15. Lower 2 bytes of the row and column address are used.

Register Name	***SEQ Reserved Address 1***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR1_P1
Address	8001C4040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR1_P1_RESERVED_ADDR1: Reserved Address Field 1. The exact definition is protocol dependent For DDR3: bits 0 - 15 are reserved. For DDR4: Bits 0 - 4 map to A16 - A20; bits 5 - 15 are reserved. This protocol uses the upper bit of the row address. For RLDRAM2 and RLDRAM3: Bits 0 - 6 map to A16 - A22; bits 7 - 15 are reserved. This protocol uses the upper bits of the row and column address.

Register Name	***SEQ Reserved Address 2***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR2_P1
Address	8001C4050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR2_P1_RESERVED_ADDR2: Reserved Address Field 2. This register controls the lower 2 bytes of the column address. Exact definition is protocol and command dependent Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION . DDR3 writes with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR3 reads with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 writes with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '1'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR4 reads with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '0'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 Refresh: A11:A15 = bits 11:15 A10 (AP) = '1'b A0:A9 = bits 0:9 DDR3 Refresh: A0:A15 = bits 0:15

Register Name	***SEQ Reserved Address 3***
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR3_P1
Address	8001C4060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR3_P1_RESERVED_ADDR3: Reserved Address Field 3. The exact definition is protocol dependent For DDR3DDR4RLDRAM2RLDRAM3: bits 0-15 are reserved

Register Name	*SEQ Reserved Address 4*
Mnemonic	DPHY01.DDRPHY_SEQ_RESERVED_ADDR4_P1
Address	8001C4070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR4_P1_RESERVED_ADDR4: Reserved Address Field 4. Bank Address. The exact definition is protocol dependent For DDR3RLDRAM2: Bits 0 - 2 map to BA0-BA2. Bits 3 - 15 are reserved. For DDR4: Bits 0 - 1 map to BA0-BA1 and bits 2 - 3 map to BG0 - BG1. Bits 4 - 15 are reserved. MPR Reads performed by the internal calibration routines: BA0-BA1 are forced to '00'b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0-BA1 addressed used/reserved). For RLDRAM2: Bits 0 - 2 map to BA0 - BA2. Bits 3 - 15 are reserved. For RLDRAM3: Bits 0 - 3 map to BA0 - BA3. Bits 4 - 15 are reserved.

Register Name	*SEQ Error Status 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ERROR_STATUS0_P1
Address	8001C4080301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_MULTIPLE_REQ_ERROR: '1'b - Error: Multiple requests received at same time.
49	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_INVALID_REQTYPE_ERROR: '1'b - Error: In the current state, this request is not expected.
50	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_EARLY_REQ_ERROR: '1'b - Error: A new request arrived before acknowledge of previous request.
51:53	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 3:5 = {PC_REQ, RC_REQ, WC_REQ}
54:57	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register. See functional description section of Sequence generator for request types from each source.
58:60	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 10:12 = {PC_REQ, RC_REQ, WC_REQ}
61:63	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 13:15 = {PC_REQ, RC_REQ, WC_REQ}

Register Name	*SEQ Error Mask 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ERROR_MASK0_P1
Address	8001C4090301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ERROR_MASK0_P1_MULT_REQ_ERR_MASK: '1'b - Prevent the MULTIPLE_REQ_ERROR bit from being set in the register. '0'b - Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	DDRPHY_SEQ_ERROR_MASK0_P1_INVALID_REQTYPE_ERR_MASK: '1'b - Prevent the INVALID_REQTYPE_ERROR bit from being set in the register. '0'b - Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	DDRPHY_SEQ_ERROR_MASK0_P1_EARLY_REQ_ERR_MASK: '1'b - Prevent the EARLY_REQ_ERROR bit from being set in the register. '0'b - Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	

Register Name	*SEQ ODT Write Configuration 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG0_P1
Address	8001C40A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P1_ODT_WR_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P1_ODT_WR_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Write Configuration 1*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG1_P1
Address	8001C40B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P1_ODT_WR_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P1_ODT_WR_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Write Configuration 2*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG2_P1
Address	8001C40C0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P1_ODT_WR_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P1_ODT_WR_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Write Configuration 3*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_WR_CONFIG3_P1
Address	8001C40D0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P1_ODT_WR_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P1_ODT_WR_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG0_P1
Address	8001C40E0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P1_ODT_RD_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P1_ODT_RD_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 1*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG1_P1
Address	8001C40F0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P1_ODT_RD_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P1_ODT_RD_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 2*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG2_P1
Address	8001C4100301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P1_ODT_RD_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P1_ODT_RD_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 3*
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_RD_CONFIG3_P1
Address	8001C4110301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P1_ODT_RD_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P1_ODT_RD_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ Memory Timing Parameter 0*
Mnemonic	DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM0_P1
Address	8001C4120301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TMOD_CYCLES: For DDR3 and DDR4: max(tMRD, tMOD) For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TRCD_CYCLES: For DDR3 and DDR4: tRCD For RLD2 and RLD3: reserved
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TRP_CYCLES: For DDR3 and DDR4 tRP For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TRFC_CYCLES: For DDR3 and DDR4: tRFC For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 1*
Mnemonic	DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM1_P1
Address	8001C4130301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TZQINIT_CYCLES: For DDR3, DDR4, RLD2, and RLD3: max(tZQINIT,tZQOPER)
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TZQCS_CYCLES: For DDR3, DDR4, RLD2, and RLD3: tZQCS
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TWLDQSEN_CYCLES: For DDR3 and DDR4: tWLDQSEN For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TWRMRD_CYCLES: For DDR3 and DDR4: tWLMRD For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 2*
Mnemonic	DPHY01.DDRPHY_SEQ_MEM_TIMING_PARAM2_P1
Address	8001C4140301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P1_TODTLON_OFF_CYCLES: For DDR3 and DDR4: max(ODTLon, ODTLoff) When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES ^ 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change or a change from read ODT values to write ODT values, or because an MRS command is issued. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window and waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued and the DDR PHY waits for tMOD cycles and then restores the ODT pins to their prior state. For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P1_TRC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tRC
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P1_TMRSC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tMRSC
60:63	RW	

Register Name	***SEQ Low Power Termination Address 2***
Mnemonic	DPHY01.DDRPHY_SEQ_LPT_ADDR2_P1
Address	8001C4170301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR2_P1_LPT_ADDR2: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ Low Power Termination Address 3***
Mnemonic	DPHY01.DDRPHY_SEQ_LPT_ADDR3_P1
Address	8001C4180301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_SEQ_LPT_ADDR3_P1_LPT_ADDR3: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	*SEQ Low Power Termination Address 4*
Mnemonic	DPHY01.DDRPHY_SEQ_LPT_ADDR4_P1
Address	8001C4190301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR4_P1_LPT_ADDR4: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	*SEQ ZQCal Encoded Rank Control 0*
Mnemonic	DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1
Address	8001C41A0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ZQCal Encoded Rank Control 1***
Mnemonic	DPHY01.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1
Address	8001C41B0301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ODT Default Configuration***
Mnemonic	DPHY01.DDRPHY_SEQ_ODT_DEFAULT_CFG_P1
Address	8001C4240301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_DEFAULT_CFG_P1_ODT_DEF_VALUES: The eight ODT values in this register are driven to the ODT pins during MRS commands. Typically the PDT value should be set to 0 during MRS commands. However if the ODT is an ODTCID function pin, then the corresponding bit in this register should be set to the desired CID value, and the corresponding bits in the ODT Write and Read Configuration registers should be set to similar values. Where: bit 0 - ODT value for ODT pin 0 during MRS command bit 1 - ODT value for ODT pin 1 during MRS command bit 2 - ODT value for ODT pin 2 during MRS command ... bit 7 - ODT value for ODT pin 7 during MRS command
56:63	RW	

Register Name	*RC Configuration 0*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG0_P1
Address	8001C8000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_RC_CONFIG0_P1_GLOBAL_PHY_OFFSET: Global PHY Offset, GPO. This field is the number of memory clock cycles added to the total read latency in the PHY. Minimum Value: When ADVANCE_RD_VALID = '0'b, the minimum value for this field is 5 + max{RoundUp(System_Delay)} - RLO. When ADVANCE_RD_VALID = '1'b, the minimum value for this field is 6 + max{RoundUp(System_Delay)} - RLO. When SPAM_EN = '1'b , the minimum value calculated for this field is increased by 1. Where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1128th of a MEMINTCLKO clock cycle}) 128) + {number of pipeline stages in the addrcmd path} + {number of pipeline stages in the read data path} max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. RLO is the READ_LATENCY_OFFSET field . Maximum Value: In 2:1 mode, the maximum value for this field is 'B'h. In 4:1 mode, the maximum value for this field is 'D'h.
52	RW	DDRPHY_RC_CONFIG0_P1_ADVANCE_RD_VALID: Number of MEMCTLCLKI clock cycles MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted before the associated read data. '0'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted during the same MEMCTLCLKI clock cycle the associated read data is valid. '1'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted one MEMCTLCLKI clock cycle before the associated read data is valid. In 4:1 Data Multiplexer mode, this field must be '0'b.
53	RW	DDRPHY_RC_CONFIG0_P1_PER_DUTY_CYCLE_SW: Set to '0' for normal function. Read commands are generated during periodic cal with a 50% duty cycle. When set to '1', periodic cal issues read commands continuously.
54:56	RW	DDRPHY_RC_CONFIG0_P1_PER_REPEAT_COUNT: If this field is 000 then the number of additional periodic cals performed per request is zero. A nonzero value in this field will preform additional periodic calibrations for each request per below: 000 is No additional periodic cal iterations are performed per request. 001 is One additional periodic cal iteration is performed per request. 010 is Two additional periodic cal iterations are performed per request. .... 111 is Seven additional periodic cal iterations are performed per request.
57	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP0: '1'b - Single bit MPR pattern memory devices in Rank Pair 0. '0'b - All bit MPR pattern memory devices in Rank Pair 0.
58	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP1: '1'b - Single bit MPR pattern memory devices in Rank Pair 1. '0'b - All bit MPR pattern memory devices in Rank Pair 1.
59	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP2: '1'b - Single bit MPR pattern memory devices in Rank Pair 2. '0'b - All bit MPR pattern memory devices in Rank Pair 2.
60	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP3: '1'b - Single bit MPR pattern memory devices in Rank Pair 3. '0'b - All bit MPR pattern memory devices in Rank Pair 3.
61	RW	DDRPHY_RC_CONFIG0_P1_ALIGN_ON_EVEN_CYCLES: This bit is only valid in 4:1 Data Multiplexer Mode. In 2:1 Data Multiplexer Mode it must be '0'b. When set, latency is added, if required, to have the read data returned on the MEMCTL Interface with the first four beats of read data returned in the same dphy_nclk cycle on the R, F, RX, and FX pins. '1'b = The first beat of a read data burst is always returned on the R pin, second beat on the F pin, third beat on the RX pin, and fourth beat on the FX pin. '0'b = The first beat of a read data burst may be returned on the R or RX pin, second beat on the F or FX pin, third beat on the RX or R pin, and fourth beat on the FX or F pin. This bit must be '0'b when a burst length that is not a multiple of four is used.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_RC_CONFIG0_P1_PERFORM_RDCLK_ALIGN: This bit must be set to '1'b in hardware. This bit is a method for behavioral simulations to skip the calibration step . '1'b - The calibration must be performed for correct operation. '0'b - In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClkRdClk Alignment. Values have no effect. The calibration fails if it is run.
63	RW	DDRPHY_RC_CONFIG0_P1_STAGGERED_PATTERN: '0'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Serial mode by the DDR PHY during Custom Read Centering. '1'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Staggered mode by the DDR PHY during Custom Read Centering.

Register Name	*RC Configuration 1*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG1_P1
Address	8001C8010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:61	RW	DDRPHY_RC_CONFIG1_P1_OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. Outer loop iteration count for digital eye. This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	constant=0b00

Register Name	*RC Configuration 2*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG2_P1
Address	8001C8020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_RC_CONFIG2_P1_CONSEQ_PASS: The number of consecutive passes required when determining the left edge of the data eye when stepping the read strobeclock through the phase rotator. When DIGITAL_EYE_EN is '1'b , this field, DIGEYE_MIN_SPACING, specifies the minimum number of cycles between outer loop iterations of digital eye (0-31 tCK cycles). This field must be set to minimum value of 6 when sampling 8 beats of data, and a minimum value of 12 when sampling 4 beats of data.
53:56	RW	
57:58	RW	DDRPHY_RC_CONFIG2_P1_BURST_WINDOW: Beats of data used for INIT and Periodic Read Eye Centering
59	RW	DDRPHY_RC_CONFIG2_P1_ALLOW_RD_FIFO_AUTO_RESET: Automatic Reset Control for RD FIFO
60:63	RO	constant=0b0000

Register Name	*RC Error Status 0*
Mnemonic	DPHY01.DDRPHY_RC_ERROR_STATUS0_P1
Address	8001C8050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_RC_ERROR_STATUS0_P1_RD_CNTL_ERROR: '1'b - Read Control Error.
49:63	RO	constant=0b000000000000000

Register Name	*RC Error Mask 0*
Mnemonic	DPHY01.DDRPHY_RC_ERROR_MASK0_P1
Address	8001C8060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_RC_ERROR_MASK0_P1_RD_CNTL_ERROR_MASK: '1'b - Mask RD_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*RC Configuration 3*
Mnemonic	DPHY01.DDRPHY_RC_CONFIG3_P1
Address	8001C8070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_RC_CONFIG3_P1_FINE_CAL_STEP_SIZE: Fine Calibration step size:000 = 1128, 001 = 164, 010 = 3128, 011 = 132100 = 5128, 101 = 364, 110 = 7128, 111 = 116
51:54	RW	DDRPHY_RC_CONFIG3_P1_COARSE_CAL_STEP_SIZE: Coarse Calibration step size:0000 = 1128, 0001 =164, 0010 = 3128, 0011 = 1320100 = 5128, 0101 = 364, 0110 = 7128, 0111 = 1161000 through 1111 = Reserved. When DIGITAL_EYE_EN is '1'b : bit 3:4 Reserved. bit 5: DIGEYE_16_NOT_1: '1'b - Block of 16 BL8 is issued during each outer loop iteration of digital eye. '0'b - One BL8 read is issued during each outer loop iteration of digital eye. bit 6: DIGEYE_REFRESH: '1' b - Issues a precharge and refresh during every outer loop iteration of digital eye. '0'b - Issues a precharge and refresh at least once every 16 outer loop iteration of digital eye.
55:56	RWX	DDRPHY_RC_CONFIG3_P1_DQ_SEL_QUAD: The quadrant within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that will automatically increment during some types of calibrations.
57:59	RWX	DDRPHY_RC_CONFIG3_P1_DQ_SEL_LANE: The data bit within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	constant=0b0000

Register Name	*WC Configuration 0*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG0_P1
Address	8001CC000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_WC_CONFIG0_P1_TWLO_TWLOE: Number of memory clock cycles which equals: 12 + {The greater of (Twldqsen - Tmod) converted to and rounded up to the nearest integer number of memory clock cycles or (Twlo + Twloe) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {Plus: The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} Used during Write Leveling.
56	RW	DDRPHY_WC_CONFIG0_P1_WL_ONE_DQS_PULSE: '0'b - continuous DQS pulses during Write Leveling. In 2:1 mode, 32 continuous pulses are sent. In 4:1 mode, 64 continuous pulses are sent. '1'b - one DQS pulse during each Write Leveling adjustment.
57:62	RW	DDRPHY_WC_CONFIG0_P1_FW_WR_RD: Number of memory clock cycles to wait between the write and read command pairs during Write Centering.
63	RW	DDRPHY_WC_CONFIG0_P1_CUSTOM_INIT_WRITE: '1'b - Write the data pattern in the registers during the Initial Pattern Write algorithm. '0'b - Write the MPR like pattern defined by the field MPR_PATTERN_BIT in the register defined in during the Initial Pattern Write algorithm.

Register Name	*WC Configuration 1*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG1_P1
Address	8001CC010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG1_P1_BIG_STEP: The amount the phase rotator value is adjusted during a big step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (BIG_STEP + 1) 128th of a memory clock.
52:54	RW	DDRPHY_WC_CONFIG1_P1_SMALL_STEP: The amount the phase rotator value is adjusted during a small step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (SMALL_STEP + 1)128th of a memory clock. Note: The Write Leveling and Write Centering algorithms will achieve the most accurate results when this field is set to zero.
55:60	RW	DDRPHY_WC_CONFIG1_P1_WR_PRE_DLY: The number of dphy_nclk cycles between a write command and a precharge command in the Coarse Initial Pattern Write, Initial Write, and Write Centering calibration algorithms.
61:63	RO	constant=0b000

Register Name	*WC Configuration 2*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG2_P1
Address	8001CC020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG2_P1_NUM_VALID_SAMPLES: The Write Leveling and Write Centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The Write Leveling algorithm performs the second to last sample at the current sample point plus 12 UI to ensure that the current sample point is at the '0'b to '1'b transition.
52:57	RW	DDRPHY_WC_CONFIG2_P1_FW_RD_WR: This delay value is used in two places in the write centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as AL + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3)
58:62	RW	
63	RW	DDRPHY_WC_CONFIG2_P1_EN_RESET_WR_DELAY_WL: '1'b - The registers are reset at the start of the Write Leveling Calibration algorithm for rank pair 0. '0'b - The registers are not reset at the start of the Write Leveling Calibration algorithm.

Register Name	*WC Error Status 0*
Mnemonic	DPHY01.DDRPHY_WC_ERROR_STATUS0_P1
Address	8001CC030301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_WC_ERROR_STATUS0_P1_WR_CNTL_ERROR: '1'b - Write Control Error.
49:63	RO	constant=0b000000000000000

Register Name	*WC Error Mask 0*
Mnemonic	DPHY01.DDRPHY_WC_ERROR_MASK0_P1
Address	8001CC040301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_ERROR_MASK0_P1_WR_CNTL_ERROR_MASK: '1'b - Mask WR_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*WC Configuration 3*
Mnemonic	DPHY01.DDRPHY_WC_CONFIG3_P1
Address	8001CC050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_CONFIG3_P1_DDR4_MRS_CMD_DQ_EN: In DDR4: '1'b - When a DDR4 MRS command is detected passing through the DDR PHY, the values in the MRS_CMD_DATA_N{0,1,2,3} fields will be driven out on the DQ pins. '0'b - DQ pins are not driven when an MRS command passes through the DDR PHY. (DDR4 ballot 1716.52) For all other protocols, this bit must be '0'b.
49:54	RW	DDRPHY_WC_CONFIG3_P1_MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. WL_per_DRAM_addr = 10 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode WL_per_DRAM_addr = 18 + 2 * MRS_CMD_DQ_ON memory clock cycles in 4:1 mode
55:60	RW	DDRPHY_WC_CONFIG3_P1_MRS_CMD_DQ_OFF: MRS_CMD_DQ_OFF = the number of dphy_nclks after the DQ pin are driven the DQ pins are not set to high impedance.
61:63	RO	constant=0b000

Register Name	*APB Configuration 0*
Mnemonic	DPHY01.DDRPHY_APB_CONFIG0_P1
Address	8001D0000301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_CONFIG0_P1_DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = False), this bit is reserved. If the core was configured for parity (APB_PARITY = True), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers and the PSLVERRO is not asserted due to bad write data parity.
49	RW	DDRPHY_APB_CONFIG0_P1_RESET_ERR_RPT: Write this bit to '1'b then write this bit to '0'b (toggle) to reset the registers defined in and.
50	RW	DDRPHY_APB_CONFIG0_P1_FORCE_ON_CLK_GATE: When set to '1'b, the clock gate in the APB Control Logic Block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB Control Logic Block to go to other logic blocks when the PHY is active.
51	RW	DDRPHY_APB_CONFIG0_P1_DEBUG_BUS_SEL_LO: Reserved.
52:55	RW	DDRPHY_APB_CONFIG0_P1_DEBUG__BUS_SEL_HI: Selects DP18 driving the high order half (bits 0:43) of the debugbus_o outputs.
56:63	RO	constant=0b00000000

Register Name	*APB Error Status 0*
Mnemonic	DPHY01.DDRPHY_APB_ERROR_STATUS0_P1
Address	8001D0010301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_ERROR_STATUS0_P1_INVALID_ADDRESS: '1'b - Register read or write to an invalid, undefined, or unused address.
49	ROX	DDRPHY_APB_ERROR_STATUS0_P1_WR_PAR_ERR: '1'b - Write data during a write operation on the APB Interface did not have odd parity (parity error).
50:63	RO	constant=0b00000000000000

Register Name	*APB Error Mask 0*
Mnemonic	DPHY01.DDRPHY_APB_ERROR_MASK0_P1
Address	8001D0020301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_ERROR_MASK0_P1_INVALID_ADDRESS_MASK: '1'b - Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	DDRPHY_APB_ERROR_MASK0_P1_WR_PAR_ERR_MASK: '1'b - Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	constant=0b00000000000000

Register Name	*APB ATEST Multiplexer Select*
Mnemonic	DPHY01.DDRPHY_APB_ATEST_MUX_SEL_P1
Address	8001D0050301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_ATEST_CNTL: bit 0: Enable ATEST1 bits 1:2: Select ATEST1 source: '00'b - DP18 #0 '01'b - DP18 #1 '10'b - DP18 #2 '11'b - Reserved bit 3: Enable ATEST2 bits 4:5: Select ATEST2 source '00'b - DP18 #3 '01'b - DP18 #4 '10'b - ADR52S '11'b - Reserved
54	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR0: Inject error on FIR bit 0 (ports 02) or 32 (ports 13).
55	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR1: Inject error on FIR bit 1 (ports 02) or 33 (ports 13).
56	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR2: Inject error on FIR bit 2 (ports 02) or 34 (ports 13).

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR3: Inject error on FIR bit 3 (ports 02) or 35 (ports 13).
58	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR4: Inject error on FIR bit 4 (ports 02) or 36 (ports 13).
59:63	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_VPROTH_CTL: VPROTH ATEST Register Control used during manufacturing test. Set to 0 for normal function.

Register Name	*APB FIR Error 0*
Mnemonic	DPHY01.DDRPHY_APB_FIR_ERR0_P1
Address	8001D0060301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET0: Indicates a non-recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 48 on ports 0 or 2; FIR bit 56 on ports 1 or 3. Reset by RESET_ERR_RPT in.
49	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET1: Indicates a non-recoverable register parity error in PHYTOP logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
50	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET2: Indicates a recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 51 on ports 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
51	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET3: Indicates a recoverable register parity error in PHYTOP logic. Sets FIR bit 52 on ports 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.
52	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET4: Indicates a non-recoverable register parity error in ADR52 master side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
53	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET5: Indicates a non-recoverable register parity error in ADR52 slave side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
54:58	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_FSM_DP18: Indicates a recoverable FSM state checker error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 51 on port 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
59:63	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_REG_DP18: Indicates a recoverable register parity error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 52 on port 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	*APB FIR Error 1*
Mnemonic	DPHY01.DDRPHY_APB_FIR_ERR1_P1
Address	8001D0070301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_APB_FIR_ERR1_P1_PC_ERR_STATUS0: Indicates a calibration error was latched in bits 0:2, 4:5 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Bits	SCOM	Field Mnemonic: Description
53:63	ROX	DDRPHY_APB_FIR_ERR1_P1_PC_INIT_CAL_ERR: Indicates a calibration error was latched in bits 0:10 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***PHY01 Pervasive FIR Register***
Mnemonic	DPHY01.PHY01_DDRPHY_FIR_REG
Address	800200900301143F (SCOM) 800200910301143F (SCOM1) 800200920301143F (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:47	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR0_FSM_CKSTP: DDR 0 FSM Error Checkstop (non-recoverable)
49	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR0_PARITY_CKSTP: DDR 0 Parity Error Checkstop (non-recoverable)
50	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR0_CALIBRATION_ERROR: DDR 0 Calibration Error (recoverable)
51	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR0_FSM_ERR: DDR 0 FSM Recoverable Error (recoverable)
52	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR0_PARITY_ERR: DDR 0 Parity Recoverable Error (recoverable)
53	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR01_FIR_PARITY_ERR: DDR 01 FIR Parity Recoverable Error (recoverable)
54:55	RO	N/A	N/A	constant=0b00
56	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR1_FSM_CKSTP: DDR 1 FSM Error Checkstop (non-recoverable)
57	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR1_PARITY_CKSTP: DDR 1 Parity Error Checkstop (non-recoverable)
58	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR1_CALIBRATION_ERROR: DDR 1 Calibration Error (recoverable)
59	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR1_FSM_ERR: DDR 1 FSM Recoverable Error (recoverable)
60	RWX	WOX_AND	WOX_OR	PHY01_DDRPHY_FIR_REG_DDR1_PARITY_ERR: DDR 1 Parity Recoverable Error (recoverable)
61:63	RO	N/A	N/A	constant=0b000

Register Name	***PHY01 Pervasive FIR Mask Register***
Mnemonic	DPHY01.PHY01_DDRPHY_FIR_MASK_REG
Address	800200930301143F (SCOM) 800200940301143F (SCOM1) 800200950301143F (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:47	RO	N/A	N/A	constant=0b000000000000000000000000000000000000000000000000
48	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR0_FSM_CKSTP_MASK: Mask DDR 0 FSM Error Checkstop
49	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR0_PARITY_CKSTP_MASK: Mask DDR 0 Parity Error Checkstop
50	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR0_CALIBRATION_ERROR_MASK: Mask DDR 0 Calibration Error
51	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR0_FSM_ERR_MASK: Mask DDR 0 FSM Recoverable Error
52	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR0_PARITY_ERR_MASK: Mask DDR 0 Parity Recoverable Error
53	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR01_FIR_PARITY_ERR_MASK: Mask DDR 01 FIR Parity Recoverable Error
54:55	RO	N/A	N/A	constant=0b00
56	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR1_FSM_CKSTP_MASK: Mask DDR 1 FSM Error Checkstop
57	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR1_PARITY_CKSTP_MASK: Mask DDR 1 Parity Error Checkstop
58	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR1_CALIBRATION_ERROR_MASK: Mask DDR 1 Calibration Error
59	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR1_FSM_ERR_MASK: Mask DDR 1 FSM Recoverable Error
60	RW	WO_AND	WO_OR	PHY01_DDRPHY_FIR_MASK_REG_DDR1_PARITY_ERR_MASK: Mask DDR 1 Parity Recover Error
61:63	RO	N/A	N/A	constant=0b000

Register Name	***PHY01 Pervasive FIR Action 0 Register***
Mnemonic	DPHY01.PHY01_DDRPHY_FIR_ACTION0_REG
Address	800200960301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RO	PHY01_DDRPHY_FIR_ACTION0_REG_DDR0_FIR_ACTION0: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
54:55	RO	constant=0b00
56:60	RO	PHY01_DDRPHY_FIR_ACTION0_REG_DDR1_FIR_ACTION0: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
61:63	RO	constant=0b000

Register Name	***PHY01 Pervasive FIR Action 1 Register***
Mnemonic	DPHY01.PHY01_DDRPHY_FIR_ACTION1_REG
Address	800200970301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RO	PHY01_DDRPHY_FIR_ACTION1_REG_DDR0_FIR_ACTION1: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
54:55	RO	constant=0b00
56:60	RO	PHY01_DDRPHY_FIR_ACTION1_REG_DDR1_FIR_ACTION1: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
61:63	RO	constant=0b000

Register Name	***PHY01 Pervasive FIR WOF Register***
Mnemonic	DPHY01.PHY01_DDRPHY_FIR_WOF_REG
Address	800200980301143F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RWX_WCLRREG	PHY01_DDRPHY_FIR_WOF_REG_DDR0_FIR_WOF: WOF Register locks on first error
54:55	RO	constant=0b00
56:60	RWX_WCLRREG	PHY01_DDRPHY_FIR_WOF_REG_DDR1_FIR_WOF: WOF Register locks on first error
61:63	RO	constant=0b000

7. PCB Slave 3: DPHY23 Indirect Registers

The memory buffer registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR0	0x800040000301183F	3980
DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR1	0x800044000301183F	3990
DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR2	0x800048000301183F	4000
DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR3	0x80004C000301183F	4010
DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR0	0x800140000301183F	4682
DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR1	0x800144000301183F	4692
DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR2	0x800148000301183F	4702
DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR3	0x80014C000301183F	4712
DPHY23.DDRPHY_ADR_DELAY0_P0_ADR0	0x800040040301183F	3981
DPHY23.DDRPHY_ADR_DELAY0_P0_ADR1	0x800044040301183F	3991
DPHY23.DDRPHY_ADR_DELAY0_P0_ADR2	0x800048040301183F	4001
DPHY23.DDRPHY_ADR_DELAY0_P0_ADR3	0x80004C040301183F	4011
DPHY23.DDRPHY_ADR_DELAY0_P1_ADR0	0x800140040301183F	4683
DPHY23.DDRPHY_ADR_DELAY0_P1_ADR1	0x800144040301183F	4693
DPHY23.DDRPHY_ADR_DELAY0_P1_ADR2	0x800148040301183F	4703
DPHY23.DDRPHY_ADR_DELAY0_P1_ADR3	0x80014C040301183F	4713
DPHY23.DDRPHY_ADR_DELAY1_P0_ADR0	0x800040050301183F	3981
DPHY23.DDRPHY_ADR_DELAY1_P0_ADR1	0x800044050301183F	3991
DPHY23.DDRPHY_ADR_DELAY1_P0_ADR2	0x800048050301183F	4001
DPHY23.DDRPHY_ADR_DELAY1_P0_ADR3	0x80004C050301183F	4011
DPHY23.DDRPHY_ADR_DELAY1_P1_ADR0	0x800140050301183F	4683
DPHY23.DDRPHY_ADR_DELAY1_P1_ADR1	0x800144050301183F	4693
DPHY23.DDRPHY_ADR_DELAY1_P1_ADR2	0x800148050301183F	4703
DPHY23.DDRPHY_ADR_DELAY1_P1_ADR3	0x80014C050301183F	4713
DPHY23.DDRPHY_ADR_DELAY2_P0_ADR0	0x800040060301183F	3982
DPHY23.DDRPHY_ADR_DELAY2_P0_ADR1	0x800044060301183F	3992
DPHY23.DDRPHY_ADR_DELAY2_P0_ADR2	0x800048060301183F	4002
DPHY23.DDRPHY_ADR_DELAY2_P0_ADR3	0x80004C060301183F	4012
DPHY23.DDRPHY_ADR_DELAY2_P1_ADR0	0x800140060301183F	4684
DPHY23.DDRPHY_ADR_DELAY2_P1_ADR1	0x800144060301183F	4694
DPHY23.DDRPHY_ADR_DELAY2_P1_ADR2	0x800148060301183F	4704
DPHY23.DDRPHY_ADR_DELAY2_P1_ADR3	0x80014C060301183F	4714
DPHY23.DDRPHY_ADR_DELAY3_P0_ADR0	0x800040070301183F	3982
DPHY23.DDRPHY_ADR_DELAY3_P0_ADR1	0x800044070301183F	3992
DPHY23.DDRPHY_ADR_DELAY3_P0_ADR2	0x800048070301183F	4002
DPHY23.DDRPHY_ADR_DELAY3_P0_ADR3	0x80004C070301183F	4012
DPHY23.DDRPHY_ADR_DELAY3_P1_ADR0	0x800140070301183F	4684
DPHY23.DDRPHY_ADR_DELAY3_P1_ADR1	0x800144070301183F	4694
DPHY23.DDRPHY_ADR_DELAY3_P1_ADR2	0x800148070301183F	4704
DPHY23.DDRPHY_ADR_DELAY3_P1_ADR3	0x80014C070301183F	4714
DPHY23.DDRPHY_ADR_DELAY4_P0_ADR0	0x800040080301183F	3983
DPHY23.DDRPHY_ADR_DELAY4_P0_ADR1	0x800044080301183F	3993
DPHY23.DDRPHY_ADR_DELAY4_P0_ADR2	0x800048080301183F	4003
DPHY23.DDRPHY_ADR_DELAY4_P0_ADR3	0x80004C080301183F	4013
DPHY23.DDRPHY_ADR_DELAY4_P1_ADR0	0x800140080301183F	4685

Mnemonic	Address	Page
DPHY23.DDRPHY_ADR_DELAY4_P1_ADR1	0x800144080301183F	4695
DPHY23.DDRPHY_ADR_DELAY4_P1_ADR2	0x800148080301183F	4705
DPHY23.DDRPHY_ADR_DELAY4_P1_ADR3	0x80014C080301183F	4715
DPHY23.DDRPHY_ADR_DELAY5_P0_ADR0	0x800040090301183F	3983
DPHY23.DDRPHY_ADR_DELAY5_P0_ADR1	0x800044090301183F	3993
DPHY23.DDRPHY_ADR_DELAY5_P0_ADR2	0x800048090301183F	4003
DPHY23.DDRPHY_ADR_DELAY5_P0_ADR3	0x80004C090301183F	4013
DPHY23.DDRPHY_ADR_DELAY5_P1_ADR0	0x800140090301183F	4685
DPHY23.DDRPHY_ADR_DELAY5_P1_ADR1	0x800144090301183F	4695
DPHY23.DDRPHY_ADR_DELAY5_P1_ADR2	0x800148090301183F	4705
DPHY23.DDRPHY_ADR_DELAY5_P1_ADR3	0x80014C090301183F	4715
DPHY23.DDRPHY_ADR_DELAY6_P0_ADR0	0x8000400A0301183F	3983
DPHY23.DDRPHY_ADR_DELAY6_P0_ADR1	0x8000440A0301183F	3993
DPHY23.DDRPHY_ADR_DELAY6_P0_ADR2	0x8000480A0301183F	4003
DPHY23.DDRPHY_ADR_DELAY6_P0_ADR3	0x80004C0A0301183F	4013
DPHY23.DDRPHY_ADR_DELAY6_P1_ADR0	0x8001400A0301183F	4685
DPHY23.DDRPHY_ADR_DELAY6_P1_ADR1	0x8001440A0301183F	4695
DPHY23.DDRPHY_ADR_DELAY6_P1_ADR2	0x8001480A0301183F	4705
DPHY23.DDRPHY_ADR_DELAY6_P1_ADR3	0x80014C0A0301183F	4715
DPHY23.DDRPHY_ADR_DELAY7_P0_ADR0	0x8000400B0301183F	3984
DPHY23.DDRPHY_ADR_DELAY7_P0_ADR1	0x8000440B0301183F	3994
DPHY23.DDRPHY_ADR_DELAY7_P0_ADR2	0x8000480B0301183F	4004
DPHY23.DDRPHY_ADR_DELAY7_P0_ADR3	0x80004C0B0301183F	4014
DPHY23.DDRPHY_ADR_DELAY7_P1_ADR0	0x8001400B0301183F	4686
DPHY23.DDRPHY_ADR_DELAY7_P1_ADR1	0x8001440B0301183F	4696
DPHY23.DDRPHY_ADR_DELAY7_P1_ADR2	0x8001480B0301183F	4706
DPHY23.DDRPHY_ADR_DELAY7_P1_ADR3	0x80014C0B0301183F	4716
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR0	0x8000400C0301183F	3984
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR1	0x8000440C0301183F	3994
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR2	0x8000480C0301183F	4004
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR3	0x80004C0C0301183F	4014
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR0	0x8001400C0301183F	4686
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR1	0x8001440C0301183F	4696
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR2	0x8001480C0301183F	4706
DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR3	0x80014C0C0301183F	4716
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR0	0x800040010301183F	3980
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR1	0x800044010301183F	3990
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR2	0x800048010301183F	4000
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR3	0x80004C010301183F	4010
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR0	0x800140010301183F	4682
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR1	0x800144010301183F	4692
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR2	0x800148010301183F	4702
DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR3	0x80014C010301183F	4712
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR0	0x800040200301183F	3986
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR1	0x800044200301183F	3996
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR2	0x800048200301183F	4006
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR3	0x80004C200301183F	4016
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR0	0x800140200301183F	4688
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR1	0x800144200301183F	4698
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR2	0x800148200301183F	4708
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR3	0x80014C200301183F	4718

Mnemonic	Address	Page
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR0	0x800040210301183F	3986
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR1	0x800044210301183F	3996
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR2	0x800048210301183F	4006
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR3	0x80004C210301183F	4016
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR0	0x800140210301183F	4688
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR1	0x800144210301183F	4698
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR2	0x800148210301183F	4708
DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR3	0x80014C210301183F	4718
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0	0x8000402A0301183F	3987
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1	0x8000442A0301183F	3997
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2	0x8000482A0301183F	4007
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3	0x80004C2A0301183F	4017
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0	0x8001402A0301183F	4689
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1	0x8001442A0301183F	4699
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2	0x8001482A0301183F	4709
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3	0x80014C2A0301183F	4719
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0	0x8000402B0301183F	3988
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1	0x8000442B0301183F	3998
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2	0x8000482B0301183F	4008
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3	0x80004C2B0301183F	4018
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0	0x8001402B0301183F	4690
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1	0x8001442B0301183F	4700
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2	0x8001482B0301183F	4710
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3	0x80014C2B0301183F	4720
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR0	0x8000401A0301183F	3985
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR1	0x8000441A0301183F	3995
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR2	0x8000481A0301183F	4005
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR3	0x80004C1A0301183F	4015
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR0	0x8001401A0301183F	4687
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR1	0x8001441A0301183F	4697
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR2	0x8001481A0301183F	4707
DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR3	0x80014C1A0301183F	4717
DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S0	0x800080330301183F	4022
DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S1	0x800084330301183F	4028
DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S0	0x800180330301183F	4724
DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S1	0x800184330301183F	4730
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S0	0x800080360301183F	4024
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S1	0x800084360301183F	4030
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S0	0x800180360301183F	4726
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S1	0x800184360301183F	4732
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S0	0x800080370301183F	4024
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S1	0x800084370301183F	4030
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S0	0x800180370301183F	4726
DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S1	0x800184370301183F	4732
DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S0	0x800080350301183F	4024
DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S1	0x800084350301183F	4029
DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S0	0x800180350301183F	4726
DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S1	0x800184350301183F	4731
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S0	0x800080300301183F	4020
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S1	0x800084300301183F	4025
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S0	0x800180300301183F	4722

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DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S1	0x800184300301183F	4727
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S0	0x800080310301183F	4020
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S1	0x800084310301183F	4026
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S0	0x800180310301183F	4722
DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S1	0x800184310301183F	4728
DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR0	0x8000402C0301183F	3989
DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR1	0x8000442C0301183F	3999
DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR2	0x8000482C0301183F	4009
DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR3	0x80004C2C0301183F	4019
DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR0	0x8001402C0301183F	4691
DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR1	0x8001442C0301183F	4701
DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR2	0x8001482C0301183F	4711
DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR3	0x80014C2C0301183F	4721
DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S0	0x800080390301183F	4025
DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S1	0x800084390301183F	4031
DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S0	0x800180390301183F	4727
DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S1	0x800184390301183F	4733
DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S0	0x800080320301183F	4021
DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S1	0x800084320301183F	4027
DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S0	0x800180320301183F	4723
DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S1	0x800184320301183F	4729
DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S0	0x800080340301183F	4023
DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S1	0x800084340301183F	4029
DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S0	0x800180340301183F	4725
DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S1	0x800184340301183F	4731
DPHY23.DDRPHY_APB_ATEST_MUX_SEL_P0	0x8000D0050301183F	4075
DPHY23.DDRPHY_APB_ATEST_MUX_SEL_P1	0x8001D0050301183F	4777
DPHY23.DDRPHY_APB_CONFIG0_P0	0x8000D0000301183F	4074
DPHY23.DDRPHY_APB_CONFIG0_P1	0x8001D0000301183F	4776
DPHY23.DDRPHY_APB_ERROR_MASK0_P0	0x8000D0020301183F	4075
DPHY23.DDRPHY_APB_ERROR_MASK0_P1	0x8001D0020301183F	4777
DPHY23.DDRPHY_APB_ERROR_STATUS0_P0	0x8000D0010301183F	4075
DPHY23.DDRPHY_APB_ERROR_STATUS0_P1	0x8001D0010301183F	4777
DPHY23.DDRPHY_APB_FIR_ERR0_P0	0x8000D0060301183F	4076
DPHY23.DDRPHY_APB_FIR_ERR0_P1	0x8001D0060301183F	4778
DPHY23.DDRPHY_APB_FIR_ERR1_P0	0x8000D0070301183F	4076
DPHY23.DDRPHY_APB_FIR_ERR1_P1	0x8001D0070301183F	4778
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_0	0x800000020301183F	3377
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_1	0x800004020301183F	3497
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_2	0x800008020301183F	3618
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_3	0x80000C020301183F	3739
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_4	0x800010020301183F	3860
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_0	0x800100020301183F	4078
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_1	0x800104020301183F	4199
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_2	0x800108020301183F	4320
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_3	0x80010C020301183F	4441
DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_4	0x800110020301183F	4562
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_0	0x800000030301183F	3377
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_1	0x800004030301183F	3497
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_2	0x800008030301183F	3618
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_3	0x80000C030301183F	3739

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DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_4	0x800010030301183F	3860
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_0	0x800100030301183F	4078
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_1	0x800104030301183F	4199
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_2	0x800108030301183F	4320
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_3	0x80010C030301183F	4441
DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_4	0x800110030301183F	4562
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_0	0x8000007C0301183F	3421
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_1	0x8000047C0301183F	3542
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_2	0x8000087C0301183F	3663
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_3	0x80000C7C0301183F	3784
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_4	0x8000107C0301183F	3905
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_0	0x8001007C0301183F	4123
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_1	0x8001047C0301183F	4244
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_2	0x8001087C0301183F	4365
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_3	0x80010C7C0301183F	4486
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_4	0x8001107C0301183F	4607
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_0	0x8000017C0301183F	3445
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_1	0x8000057C0301183F	3566
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_2	0x8000097C0301183F	3687
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_3	0x80000D7C0301183F	3808
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_4	0x8000117C0301183F	3929
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_0	0x8001017C0301183F	4147
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_1	0x8001057C0301183F	4268
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_2	0x8001097C0301183F	4389
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_3	0x80010D7C0301183F	4510
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_4	0x8001117C0301183F	4631
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_0	0x8000027C0301183F	3470
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_1	0x8000067C0301183F	3591
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_2	0x80000A7C0301183F	3712
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_3	0x80000E7C0301183F	3833
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_4	0x8000127C0301183F	3954
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_0	0x8001027C0301183F	4172
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_1	0x8001067C0301183F	4293
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_2	0x80010A7C0301183F	4414
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_3	0x80010E7C0301183F	4535
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_4	0x8001127C0301183F	4656
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_0	0x8000037C0301183F	3494
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_1	0x8000077C0301183F	3615
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_2	0x80000B7C0301183F	3736
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_3	0x80000F7C0301183F	3857
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_4	0x8000137C0301183F	3978
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_0	0x8001037C0301183F	4196
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_1	0x8001077C0301183F	4317
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_2	0x80010B7C0301183F	4438
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_3	0x80010F7C0301183F	4559
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_4	0x8001137C0301183F	4680
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_0	0x8000007D0301183F	3421
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_1	0x8000047D0301183F	3542
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_2	0x8000087D0301183F	3663
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_3	0x80000C7D0301183F	3784
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_4	0x8000107D0301183F	3905

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DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_0	0x8001007D0301183F	4123
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_1	0x8001047D0301183F	4244
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_2	0x8001087D0301183F	4365
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_3	0x80010C7D0301183F	4486
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_4	0x8001107D0301183F	4607
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_0	0x8000017D0301183F	3446
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_1	0x8000057D0301183F	3566
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_2	0x8000097D0301183F	3687
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_3	0x80000D7D0301183F	3808
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_4	0x8000117D0301183F	3929
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_0	0x8001017D0301183F	4147
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_1	0x8001057D0301183F	4268
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_2	0x8001097D0301183F	4389
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_3	0x80010D7D0301183F	4510
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_4	0x8001117D0301183F	4631
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_0	0x8000027D0301183F	3470
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_1	0x8000067D0301183F	3591
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_2	0x80000A7D0301183F	3712
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_3	0x80000E7D0301183F	3833
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_4	0x8000127D0301183F	3954
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_0	0x8001027D0301183F	4172
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_1	0x8001067D0301183F	4293
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_2	0x80010A7D0301183F	4414
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_3	0x80010E7D0301183F	4535
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_4	0x8001127D0301183F	4656
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_0	0x8000037D0301183F	3495
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_1	0x8000077D0301183F	3616
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_2	0x80000B7D0301183F	3737
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_3	0x80000F7D0301183F	3858
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_4	0x8000137D0301183F	3979
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_0	0x8001037D0301183F	4197
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_1	0x8001077D0301183F	4318
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_2	0x80010B7D0301183F	4439
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_3	0x80010F7D0301183F	4560
DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_4	0x8001137D0301183F	4681
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_0	0x800000000301183F	3375
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_1	0x800004000301183F	3496
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_2	0x800008000301183F	3617
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_3	0x80000C000301183F	3738
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_4	0x800010000301183F	3859
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_0	0x800100000301183F	4077
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_1	0x800104000301183F	4198
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_2	0x800108000301183F	4319
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_3	0x80010C000301183F	4440
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_4	0x800110000301183F	4561
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_0	0x800000010301183F	3376
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_1	0x800004010301183F	3496
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_2	0x800008010301183F	3617
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_3	0x80000C010301183F	3738
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_4	0x800010010301183F	3859
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_0	0x800100010301183F	4077

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DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_1	0x800104010301183F	4198
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_2	0x800108010301183F	4319
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_3	0x80010C010301183F	4440
DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_4	0x800110010301183F	4561
DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_0	0x8000000B0301183F	3384
DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_1	0x8000040B0301183F	3505
DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_2	0x8000080B0301183F	3626
DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_3	0x80000C0B0301183F	3747
DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_4	0x8000100B0301183F	3868
DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_0	0x8001000B0301183F	4086
DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_1	0x8001040B0301183F	4207
DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_2	0x8001080B0301183F	4328
DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_3	0x80010C0B0301183F	4449
DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_4	0x8001100B0301183F	4570
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0	0x8000006F0301183F	3415
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1	0x8000046F0301183F	3535
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2	0x8000086F0301183F	3656
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3	0x80000C6F0301183F	3777
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4	0x8000106F0301183F	3898
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0	0x8001006F0301183F	4116
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1	0x8001046F0301183F	4237
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2	0x8001086F0301183F	4358
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3	0x80010C6F0301183F	4479
DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4	0x8001106F0301183F	4600
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_0	0x8000000080301183F	3383
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_1	0x8000040080301183F	3503
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_2	0x8000080080301183F	3624
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_3	0x80000C080301183F	3745
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_4	0x8000100080301183F	3866
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_0	0x8001000080301183F	4084
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_1	0x800104080301183F	4205
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_2	0x800108080301183F	4326
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_3	0x80010C080301183F	4447
DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_4	0x800110080301183F	4568
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_0	0x8000001D0301183F	3393
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_1	0x8000041D0301183F	3514
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_2	0x8000081D0301183F	3635
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_3	0x80000C1D0301183F	3756
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_4	0x8000101D0301183F	3877
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_0	0x8001001D0301183F	4095
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_1	0x8001041D0301183F	4216
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_2	0x8001081D0301183F	4337
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_3	0x80010C1D0301183F	4458
DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_4	0x8001101D0301183F	4579
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_0	0x8000003703011 83F	3396
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_1	0x8000043703011 83F	3517
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_2	0x8000083703011 83F	3638
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_3	0x80000C3703011 83F	3759
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_4	0x8000103703011 83F	3880
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_0	0x8001003703011 83F	4098
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_1	0x8001043703011 83F	4219

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DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_2	0x800108370301183F	4340
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_3	0x80010C370301183F	4461
DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_4	0x800110370301183F	4582
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_0	0x800000300301183F	3394
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_1	0x800004300301183F	3515
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_2	0x800008300301183F	3636
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_3	0x80000C300301183F	3757
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_4	0x800010300301183F	3878
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_0	0x800100300301183F	4096
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_1	0x800104300301183F	4217
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_2	0x800108300301183F	4338
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_3	0x80010C300301183F	4459
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_4	0x800110300301183F	4580
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_0	0x800001300301183F	3427
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_1	0x800005300301183F	3548
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_2	0x800009300301183F	3669
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_3	0x80000D300301183F	3790
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_4	0x800011300301183F	3911
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_0	0x800101300301183F	4129
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_1	0x800105300301183F	4250
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_2	0x800109300301183F	4371
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_3	0x80010D300301183F	4492
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_4	0x800111300301183F	4613
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_0	0x800002300301183F	3452
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_1	0x800006300301183F	3572
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_2	0x80000A300301183F	3693
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_3	0x80000E300301183F	3814
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_4	0x800012300301183F	3935
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_0	0x800102300301183F	4153
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_1	0x800106300301183F	4274
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_2	0x80010A300301183F	4395
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_3	0x80010E300301183F	4516
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_4	0x800112300301183F	4637
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_0	0x800003300301183F	3476
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_1	0x800007300301183F	3597
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_2	0x80000B300301183F	3718
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_3	0x80000F300301183F	3839
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_4	0x800013300301183F	3960
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_0	0x800103300301183F	4178
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_1	0x800107300301183F	4299
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_2	0x80010B300301183F	4420
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_3	0x80010F300301183F	4541
DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_4	0x800113300301183F	4662
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_0	0x800000310301183F	3394
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_1	0x800004310301183F	3515
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_2	0x800008310301183F	3636
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_3	0x80000C310301183F	3757
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_4	0x800010310301183F	3878
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_0	0x800100310301183F	4096
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_1	0x800104310301183F	4217
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_2	0x800108310301183F	4338

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DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_3	0x80010C310301183F	4459
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_4	0x800110310301183F	4580
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_0	0x800001310301183F	3428
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_1	0x800005310301183F	3548
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_2	0x800009310301183F	3669
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_3	0x80000D310301183F	3790
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_4	0x800011310301183F	3911
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_0	0x800101310301183F	4129
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_1	0x800105310301183F	4250
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_2	0x800109310301183F	4371
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_3	0x80010D310301183F	4492
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_4	0x800111310301183F	4613
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_0	0x800002310301183F	3452
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_1	0x800006310301183F	3573
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_2	0x80000A310301183F	3694
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_3	0x80000E310301183F	3815
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_4	0x800012310301183F	3936
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_0	0x800102310301183F	4154
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_1	0x800106310301183F	4275
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_2	0x80010A310301183F	4396
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_3	0x80010E310301183F	4517
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_4	0x800112310301183F	4638
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_0	0x800003310301183F	3477
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_1	0x800007310301183F	3598
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_2	0x80000B310301183F	3719
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_3	0x80000F310301183F	3840
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_4	0x800013310301183F	3961
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_0	0x800103310301183F	4179
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_1	0x800107310301183F	4300
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_2	0x80010B310301183F	4421
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_3	0x80010F310301183F	4542
DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_4	0x800113310301183F	4663
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_0	0x800000130301183F	3387
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_1	0x800004130301183F	3508
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_2	0x800008130301183F	3629
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_3	0x80000C130301183F	3750
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_4	0x800010130301183F	3871
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_0	0x800100130301183F	4089
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_1	0x800104130301183F	4210
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_2	0x800108130301183F	4331
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_3	0x80010C130301183F	4452
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_4	0x800110130301183F	4573
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_0	0x800001130301183F	3427
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_1	0x800005130301183F	3547
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_2	0x800009130301183F	3668
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_3	0x80000D130301183F	3789
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_4	0x800011130301183F	3910
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_0	0x800101130301183F	4128
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_1	0x800105130301183F	4249
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_2	0x800109130301183F	4370
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_3	0x80010D130301183F	4491

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DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_4	0x800111130301183F	4612
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_0	0x800002130301183F	3451
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_1	0x800006130301183F	3572
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_2	0x80000A130301183F	3693
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_3	0x80000E130301183F	3814
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_4	0x800012130301183F	3935
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_0	0x800102130301183F	4153
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_1	0x800106130301183F	4274
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_2	0x80010A130301183F	4395
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_3	0x80010E130301183F	4516
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_4	0x800112130301183F	4637
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_0	0x800003130301183F	3476
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_1	0x800007130301183F	3597
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_2	0x80000B130301183F	3718
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_3	0x80000F130301183F	3839
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_4	0x800013130301183F	3960
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_0	0x800103130301183F	4178
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_1	0x800107130301183F	4299
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_2	0x80010B130301183F	4420
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_3	0x80010F130301183F	4541
DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_4	0x800113130301183F	4662
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_0	0x800000090301183F	3383
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_1	0x800004090301183F	3504
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_2	0x800008090301183F	3625
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_3	0x80000C090301183F	3746
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_4	0x800010090301183F	3867
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_0	0x800100090301183F	4085
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_1	0x800104090301183F	4206
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_2	0x800108090301183F	4327
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_3	0x80010C090301183F	4448
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_4	0x800110090301183F	4569
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_0	0x800001090301183F	3425
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_1	0x800005090301183F	3546
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_2	0x800009090301183F	3667
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_3	0x80000D090301183F	3788
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_4	0x800011090301183F	3909
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_0	0x800101090301183F	4127
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_1	0x800105090301183F	4248
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_2	0x800109090301183F	4369
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_3	0x80010D090301183F	4490
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_4	0x800111090301183F	4611
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_0	0x800002090301183F	3450
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_1	0x800006090301183F	3570
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_2	0x80000A090301183F	3691
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_3	0x80000E090301183F	3812
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_4	0x800012090301183F	3933
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_0	0x800102090301183F	4151
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_1	0x800106090301183F	4272
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_2	0x80010A090301183F	4393
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_3	0x80010E090301183F	4514
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_4	0x800112090301183F	4635

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DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_0	0x8000030903011 83F	3474
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_1	0x8000070903011 83F	3595
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_2	0x80000B0903011 83F	3716
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_3	0x80000F0903011 83F	3837
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_4	0x8000130903011 83F	3958
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_0	0x8001030903011 83F	4176
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_1	0x8001070903011 83F	4297
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_2	0x80010B0903011 83F	4418
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_3	0x80010F0903011 83F	4539
DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_4	0x8001130903011 83F	4660
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_0	0x8000007E0301183F	3421
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_1	0x8000047E0301183F	3542
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_2	0x8000087E0301183F	3663
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_3	0x80000C7E0301183F	3784
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_4	0x8000107E0301183F	3905
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_0	0x8001007E0301183F	4123
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_1	0x8001047E0301183F	4244
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_2	0x8001087E0301183F	4365
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_3	0x80010C7E0301183F	4486
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_4	0x8001107E0301183F	4607
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_0	0x8000017E0301183F	3446
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_1	0x8000057E0301183F	3567
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_2	0x8000097E0301183F	3688
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_3	0x80000D7E0301183F	3809
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_4	0x8000117E0301183F	3930
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_0	0x8001017E0301183F	4148
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_1	0x8001057E0301183F	4269
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_2	0x8001097E0301183F	4390
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_3	0x80010D7E0301183F	4511
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_4	0x8001117E0301183F	4632
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_0	0x8000027E0301183F	3470
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_1	0x8000067E0301183F	3591
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_2	0x80000A7E0301183F	3712
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_3	0x80000E7E0301183F	3833
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_4	0x8000127E0301183F	3954
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_0	0x8001027E0301183F	4172
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_1	0x8001067E0301183F	4293
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_2	0x80010A7E0301183F	4414
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_3	0x80010E7E0301183F	4535
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_4	0x8001127E0301183F	4656
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_0	0x8000037E0301183F	3495
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_1	0x8000077E0301183F	3616
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_2	0x80000B7E0301183F	3737
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_3	0x80000F7E0301183F	3858
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_4	0x8000137E0301183F	3979
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_0	0x8001037E0301183F	4197
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_1	0x8001077E0301183F	4318
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_2	0x80010B7E0301183F	4439
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_3	0x80010F7E0301183F	4560
DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_4	0x8001137E0301183F	4681
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_0	0x8000000A0301183F	3384

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DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_1	0x8000040A0301183F	3504
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_2	0x8000080A0301183F	3625
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_3	0x80000C0A0301183F	3746
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_4	0x8000100A0301183F	3867
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_0	0x8001000A0301183F	4085
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_1	0x8001040A0301183F	4206
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_2	0x8001080A0301183F	4327
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_3	0x80010C0A0301183F	4448
DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_4	0x8001100A0301183F	4569
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_0	0x8000005C0301183F	3407
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_1	0x8000045C0301183F	3528
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_2	0x8000085C0301183F	3649
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_3	0x80000C5C0301183F	3770
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_4	0x8000105C0301183F	3891
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_0	0x8001005C0301183F	4109
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_1	0x8001045C0301183F	4230
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_2	0x8001085C0301183F	4351
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_3	0x80010C5C0301183F	4472
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_4	0x8001105C0301183F	4593
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_0	0x8000015C0301183F	3439
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_1	0x8000055C0301183F	3559
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_2	0x8000095C0301183F	3680
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_3	0x80000D5C0301183F	3801
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_4	0x8000115C0301183F	3922
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_0	0x8001015C0301183F	4140
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_1	0x8001055C0301183F	4261
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_2	0x8001095C0301183F	4382
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_3	0x80010D5C0301183F	4503
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_4	0x8001115C0301183F	4624
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_0	0x8000025C0301183F	3463
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_1	0x8000065C0301183F	3584
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_2	0x80000A5C0301183F	3705
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_3	0x80000E5C0301183F	3826
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_4	0x8000125C0301183F	3947
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_0	0x8001025C0301183F	4165
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_1	0x8001065C0301183F	4286
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_2	0x80010A5C0301183F	4407
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_3	0x80010E5C0301183F	4528
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_4	0x8001125C0301183F	4649
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_0	0x8000035C0301183F	3488
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_1	0x8000075C0301183F	3609
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_2	0x80000B5C0301183F	3730
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_3	0x80000F5C0301183F	3851
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_4	0x8000135C0301183F	3972
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_0	0x8001035C0301183F	4190
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_1	0x8001075C0301183F	4311
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_2	0x80010B5C0301183F	4432
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_3	0x80010F5C0301183F	4553
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_4	0x8001135C0301183F	4674
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_0	0x8000005D0301183F	3408
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_1	0x8000045D0301183F	3528

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DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_2	0x8000085D0301183F	3649
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_3	0x80000C5D0301183F	3770
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_4	0x8000105D0301183F	3891
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_0	0x8001005D0301183F	4109
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_1	0x8001045D0301183F	4230
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_2	0x8001085D0301183F	4351
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_3	0x80010C5D0301183F	4472
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_4	0x8001105D0301183F	4593
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_0	0x8000015D0301183F	3439
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_1	0x8000055D0301183F	3560
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_2	0x8000095D0301183F	3681
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_3	0x80000D5D0301183F	3802
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_4	0x8000115D0301183F	3923
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_0	0x8001015D0301183F	4141
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_1	0x8001055D0301183F	4262
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_2	0x8001095D0301183F	4383
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_3	0x80010D5D0301183F	4504
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_4	0x8001115D0301183F	4625
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_0	0x8000025D0301183F	3463
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_1	0x8000065D0301183F	3584
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_2	0x80000A5D0301183F	3705
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_3	0x80000E5D0301183F	3826
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_4	0x8000125D0301183F	3947
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_0	0x8001025D0301183F	4165
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_1	0x8001065D0301183F	4286
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_2	0x80010A5D0301183F	4407
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_3	0x80010E5D0301183F	4528
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_4	0x8001125D0301183F	4649
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_0	0x8000035D0301183F	3488
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_1	0x8000075D0301183F	3609
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_2	0x80000B5D0301183F	3730
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_3	0x80000F5D0301183F	3851
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_4	0x8000135D0301183F	3972
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_0	0x8001035D0301183F	4190
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_1	0x8001075D0301183F	4311
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_2	0x80010B5D0301183F	4432
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_3	0x80010F5D0301183F	4553
DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_4	0x8001135D0301183F	4674
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_0	0x800000750301183F	3417
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_1	0x800004750301183F	3537
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_2	0x800008750301183F	3658
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_3	0x80000C750301183F	3779
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_4	0x800010750301183F	3900
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_0	0x800100750301183F	4118
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_1	0x800104750301183F	4239
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_2	0x800108750301183F	4360
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_3	0x80010C750301183F	4481
DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_4	0x800110750301183F	4602
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_0	0x800000780301183F	3419
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_1	0x800004780301183F	3540
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_2	0x800008780301183F	3661

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DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_3	0x80000C780301183F	3782
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_4	0x800010780301183F	3903
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_0	0x800100780301183F	4121
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_1	0x800104780301183F	4242
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_2	0x800108780301183F	4363
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_3	0x80010C780301183F	4484
DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_4	0x800110780301183F	4605
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_0	0x8000007A0301183F	3420
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_1	0x8000047A0301183F	3541
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_2	0x8000087A0301183F	3662
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_3	0x80000C7A0301183F	3783
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_4	0x8000107A0301183F	3904
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_0	0x8001007A0301183F	4122
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_1	0x8001047A0301183F	4243
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_2	0x8001087A0301183F	4364
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_3	0x80010C7A0301183F	4485
DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_4	0x8001107A0301183F	4606
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_0	0x800000790301183F	3420
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_1	0x800004790301183F	3540
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_2	0x800008790301183F	3661
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_3	0x80000C790301183F	3782
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_4	0x800010790301183F	3903
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_0	0x800100790301183F	4121
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_1	0x800104790301183F	4242
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_2	0x800108790301183F	4363
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_3	0x80010C790301183F	4484
DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_4	0x800110790301183F	4605
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_0	0x8000007B0301183F	3420
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_1	0x8000047B0301183F	3541
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_2	0x8000087B0301183F	3662
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_3	0x80000C7B0301183F	3783
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_4	0x8000107B0301183F	3904
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_0	0x8001007B0301183F	4122
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_1	0x8001047B0301183F	4243
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_2	0x8001087B0301183F	4364
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_3	0x80010C7B0301183F	4485
DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_4	0x8001107B0301183F	4606
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_0	0x800000320301183F	3394
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_1	0x800004320301183F	3515
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_2	0x800008320301183F	3636
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_3	0x80000C320301183F	3757
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_4	0x800010320301183F	3878
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_0	0x800100320301183F	4096
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_1	0x800104320301183F	4217
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_2	0x800108320301183F	4338
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_3	0x80010C320301183F	4459
DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_4	0x800110320301183F	4580
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_0	0x800000330301183F	3395
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_1	0x800004330301183F	3516
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_2	0x800008330301183F	3637
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_3	0x80000C330301183F	3758

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DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_4	0x800010330301183F	3879
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_0	0x800100330301183F	4097
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_1	0x800104330301183F	4218
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_2	0x800108330301183F	4339
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_3	0x80010C330301183F	4460
DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_4	0x800110330301183F	4581
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_0	0x800000340301183F	3396
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_1	0x800004340301183F	3516
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_2	0x800008340301183F	3637
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_3	0x80000C340301183F	3758
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_4	0x800010340301183F	3879
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_0	0x800100340301183F	4097
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_1	0x800104340301183F	4218
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_2	0x800108340301183F	4339
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_3	0x80010C340301183F	4460
DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_4	0x800110340301183F	4581
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_0	0x800000760301183F	3418
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_1	0x800004760301183F	3538
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_2	0x800008760301183F	3659
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_3	0x80000C760301183F	3780
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_4	0x800010760301183F	3901
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_0	0x800100760301183F	4119
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_1	0x800104760301183F	4240
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_2	0x800108760301183F	4361
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_3	0x80010C760301183F	4482
DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_4	0x800110760301183F	4603
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_0	0x800000770301183F	3418
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_1	0x800004770301183F	3539
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_2	0x800008770301183F	3660
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_3	0x80000C770301183F	3781
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_4	0x800010770301183F	3902
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_0	0x800100770301183F	4120
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_1	0x800104770301183F	4241
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_2	0x800108770301183F	4362
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_3	0x80010C770301183F	4483
DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_4	0x800110770301183F	4604
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_0	0x8000006D0301183F	3414
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_1	0x8000046D0301183F	3535
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_2	0x8000086D0301183F	3656
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_3	0x80000C6D0301183F	3777
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_4	0x8000106D0301183F	3898
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_0	0x8001006D0301183F	4116
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_1	0x8001046D0301183F	4237
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_2	0x8001086D0301183F	4358
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_3	0x80010C6D0301183F	4479
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_4	0x8001106D0301183F	4600
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_0	0x800000120301183F	3386
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_1	0x800004120301183F	3507
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_2	0x800008120301183F	3628
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_3	0x80000C120301183F	3749
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_4	0x800010120301183F	3870

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DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_0	0x800100120301183F	4088
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_1	0x800104120301183F	4209
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_2	0x800108120301183F	4330
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_3	0x80010C120301183F	4451
DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_4	0x800110120301183F	4572
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_0	0x800000150301183F	3389
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_1	0x800004150301183F	3510
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_2	0x800008150301183F	3631
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_3	0x80000C150301183F	3752
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_4	0x800010150301183F	3873
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_0	0x800100150301183F	4091
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_1	0x800104150301183F	4212
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_2	0x800108150301183F	4333
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_3	0x80010C150301183F	4454
DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_4	0x800110150301183F	4575
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_0	0x8000000E0301183F	3385
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_1	0x8000040E0301183F	3506
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_2	0x8000080E0301183F	3627
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_3	0x80000C0E0301183F	3748
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_4	0x8000100E0301183F	3869
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_0	0x8001000E0301183F	4087
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_1	0x8001040E0301183F	4208
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_2	0x8001080E0301183F	4329
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_3	0x80010C0E0301183F	4450
DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_4	0x8001100E0301183F	4571
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_0	0x8000000F0301183F	3385
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_1	0x8000040F0301183F	3506
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_2	0x8000080F0301183F	3627
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_3	0x80000C0F0301183F	3748
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_4	0x8000100F0301183F	3869
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_0	0x8001000F0301183F	4087
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_1	0x8001040F0301183F	4208
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_2	0x8001080F0301183F	4329
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_3	0x80010C0F0301183F	4450
DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_4	0x8001100F0301183F	4571
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_0	0x800000100301183F	3386
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_1	0x800004100301183F	3506
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_2	0x800008100301183F	3627
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_3	0x80000C100301183F	3748
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_4	0x800010100301183F	3869
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_0	0x800100100301183F	4087
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_1	0x800104100301183F	4208
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_2	0x800108100301183F	4329
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_3	0x80010C100301183F	4450
DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_4	0x800110100301183F	4571
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_0	0x800000110301183F	3386
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_1	0x800004110301183F	3507
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_2	0x800008110301183F	3628
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_3	0x80000C110301183F	3749
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_4	0x800010110301183F	3870
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_0	0x800100110301183F	4088

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DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_1	0x800104110301183F	4209
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_2	0x800108110301183F	4330
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_3	0x80010C110301183F	4451
DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_4	0x800110110301183F	4572
DPHY23.DDRPHY_DP18_RD_STATUS0_P0_0	0x800000140301183F	3387
DPHY23.DDRPHY_DP18_RD_STATUS0_P0_1	0x800004140301183F	3508
DPHY23.DDRPHY_DP18_RD_STATUS0_P0_2	0x800008140301183F	3629
DPHY23.DDRPHY_DP18_RD_STATUS0_P0_3	0x80000C140301183F	3750
DPHY23.DDRPHY_DP18_RD_STATUS0_P0_4	0x800010140301183F	3871
DPHY23.DDRPHY_DP18_RD_STATUS0_P1_0	0x800100140301183F	4089
DPHY23.DDRPHY_DP18_RD_STATUS0_P1_1	0x800104140301183F	4210
DPHY23.DDRPHY_DP18_RD_STATUS0_P1_2	0x800108140301183F	4331
DPHY23.DDRPHY_DP18_RD_STATUS0_P1_3	0x80010C140301183F	4452
DPHY23.DDRPHY_DP18_RD_STATUS0_P1_4	0x800110140301183F	4573
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_0	0x800000040301183F	3378
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_1	0x800004040301183F	3498
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_2	0x800008040301183F	3619
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_3	0x80000C040301183F	3740
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_4	0x800010040301183F	3861
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_0	0x800100040301183F	4079
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_1	0x800104040301183F	4200
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_2	0x800108040301183F	4321
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_3	0x80010C040301183F	4442
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_4	0x800110040301183F	4563
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_0	0x800001040301183F	3422
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_1	0x800005040301183F	3543
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_2	0x800009040301183F	3664
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_3	0x80000D040301183F	3785
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_4	0x800011040301183F	3906
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_0	0x800101040301183F	4124
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_1	0x800105040301183F	4245
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_2	0x800109040301183F	4366
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_3	0x80010D040301183F	4487
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_4	0x800111040301183F	4608
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_0	0x800002040301183F	3447
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_1	0x800006040301183F	3567
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_2	0x80000A040301183F	3688
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_3	0x80000E040301183F	3809
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_4	0x800012040301183F	3930
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_0	0x800102040301183F	4148
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_1	0x800106040301183F	4269
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_2	0x80010A040301183F	4390
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_3	0x80010E040301183F	4511
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_4	0x800112040301183F	4632
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_0	0x800003040301183F	3471
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_1	0x800007040301183F	3592
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_2	0x80000B040301183F	3713
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_3	0x80000F040301183F	3834
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_4	0x800013040301183F	3955
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_0	0x800103040301183F	4173
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_1	0x800107040301183F	4294

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DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_2	0x80010B040301183F	4415
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_3	0x80010F040301183F	4536
DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_4	0x800113040301183F	4657
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_0	0x800000500301183F	3403
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_1	0x800004500301183F	3524
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_2	0x800008500301183F	3645
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_3	0x80000C500301183F	3766
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_4	0x800010500301183F	3887
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_0	0x800100500301183F	4105
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_1	0x800104500301183F	4226
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_2	0x800108500301183F	4347
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_3	0x80010C500301183F	4468
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_4	0x800110500301183F	4589
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_0	0x800001500301183F	3435
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_1	0x800005500301183F	3555
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_2	0x800009500301183F	3676
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_3	0x80000D500301183F	3797
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_4	0x800011500301183F	3918
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_0	0x800101500301183F	4136
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_1	0x800105500301183F	4257
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_2	0x800109500301183F	4378
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_3	0x80010D500301183F	4499
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_4	0x800111500301183F	4620
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_0	0x800002500301183F	3459
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_1	0x800006500301183F	3580
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_2	0x80000A500301183F	3701
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_3	0x80000E500301183F	3822
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_4	0x800012500301183F	3943
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_0	0x800102500301183F	4161
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_1	0x800106500301183F	4282
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_2	0x80010A500301183F	4403
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_3	0x80010E500301183F	4524
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_4	0x800112500301183F	4645
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_0	0x800003500301183F	3484
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_1	0x800007500301183F	3605
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_2	0x80000B500301183F	3726
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_3	0x80000F500301183F	3847
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_4	0x800013500301183F	3968
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_0	0x800103500301183F	4186
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_1	0x800107500301183F	4307
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_2	0x80010B500301183F	4428
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_3	0x80010F500301183F	4549
DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_4	0x800113500301183F	4670
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_0	0x800000510301183F	3404
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_1	0x800004510301183F	3525
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_2	0x800008510301183F	3646
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_3	0x80000C510301183F	3767
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_4	0x800010510301183F	3888
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_0	0x800100510301183F	4106
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_1	0x800104510301183F	4227
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_2	0x800108510301183F	4348

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DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_3	0x80010C510301183F	4469
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_4	0x800110510301183F	4590
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_0	0x800001510301183F	3435
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_1	0x800005510301183F	3556
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_2	0x800009510301183F	3677
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_3	0x80000D510301183F	3798
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_4	0x800011510301183F	3919
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_0	0x800101510301183F	4137
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_1	0x800105510301183F	4258
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_2	0x800109510301183F	4379
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_3	0x80010D510301183F	4500
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_4	0x800111510301183F	4621
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_0	0x800002510301183F	3460
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_1	0x800006510301183F	3580
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_2	0x80000A510301183F	3701
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_3	0x80000E510301183F	3822
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_4	0x800012510301183F	3943
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_0	0x800102510301183F	4161
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_1	0x800106510301183F	4282
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_2	0x80010A510301183F	4403
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_3	0x80010E510301183F	4524
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_4	0x800112510301183F	4645
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_0	0x800003510301183F	3484
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_1	0x800007510301183F	3605
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_2	0x80000B510301183F	3726
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_3	0x80000F510301183F	3847
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_4	0x800013510301183F	3968
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_0	0x800103510301183F	4186
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_1	0x800107510301183F	4307
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_2	0x80010B510301183F	4428
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_3	0x80010F510301183F	4549
DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_4	0x800113510301183F	4670
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_0	0x800000520301183F	3404
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_1	0x800004520301183F	3525
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_2	0x800008520301183F	3646
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_3	0x80000C520301183F	3767
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_4	0x800010520301183F	3888
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_0	0x800100520301183F	4106
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_1	0x800104520301183F	4227
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_2	0x800108520301183F	4348
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_3	0x80010C520301183F	4469
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_4	0x800110520301183F	4590
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_0	0x800001520301183F	3436
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_1	0x800005520301183F	3556
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_2	0x800009520301183F	3677
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_3	0x80000D520301183F	3798
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_4	0x800011520301183F	3919
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_0	0x800101520301183F	4137
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_1	0x800105520301183F	4258
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_2	0x800109520301183F	4379
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_3	0x80010D520301183F	4500

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DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_4	0x800111520301183F	4621
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_0	0x800002520301183F	3460
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_1	0x800006520301183F	3581
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_2	0x80000A520301183F	3702
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_3	0x80000E520301183F	3823
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_4	0x800012520301183F	3944
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_0	0x800102520301183F	4162
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_1	0x800106520301183F	4283
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_2	0x80010A520301183F	4404
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_3	0x80010E520301183F	4525
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_4	0x800112520301183F	4646
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_0	0x800003520301183F	3485
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_1	0x800007520301183F	3606
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_2	0x80000B520301183F	3727
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_3	0x80000F520301183F	3848
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_4	0x800013520301183F	3969
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_0	0x800103520301183F	4187
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_1	0x800107520301183F	4308
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_2	0x80010B520301183F	4429
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_3	0x80010F520301183F	4550
DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_4	0x800113520301183F	4671
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_0	0x800000530301183F	3405
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_1	0x800004530301183F	3526
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_2	0x800008530301183F	3647
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_3	0x80000C530301183F	3768
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_4	0x800010530301183F	3889
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_0	0x800100530301183F	4107
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_1	0x800104530301183F	4228
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_2	0x800108530301183F	4349
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_3	0x80010C530301183F	4470
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_4	0x800110530301183F	4591
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_0	0x800001530301183F	3436
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_1	0x800005530301183F	3557
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_2	0x800009530301183F	3678
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_3	0x80000D530301183F	3799
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_4	0x800011530301183F	3920
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_0	0x800101530301183F	4138
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_1	0x800105530301183F	4259
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_2	0x800109530301183F	4380
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_3	0x80010D530301183F	4501
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_4	0x800111530301183F	4622
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_0	0x800002530301183F	3461
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_1	0x800006530301183F	3581
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_2	0x80000A530301183F	3702
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_3	0x80000E530301183F	3823
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_4	0x800012530301183F	3944
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_0	0x800102530301183F	4162
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_1	0x800106530301183F	4283
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_2	0x80010A530301183F	4404
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_3	0x80010E530301183F	4525
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_4	0x800112530301183F	4646

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DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_0	0x8000035303011 83F	3485
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_1	0x8000075303011 83F	3606
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_2	0x80000B5303011 83F	3727
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_3	0x80000F5303011 83F	3848
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_4	0x8000135303011 83F	3969
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_0	0x8001035303011 83F	4187
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_1	0x8001075303011 83F	4308
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_2	0x80010B5303011 83F	4429
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_3	0x80010F5303011 83F	4550
DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_4	0x8001135303011 83F	4671
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_0	0x8000054030118 3F	3405
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_1	0x8000454030118 3F	3526
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_2	0x8000854030118 3F	3647
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_3	0x80000C5403011 83F	3768
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_4	0x8000105403011 83F	3889
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_0	0x8001005403011 83F	4107
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_1	0x8001045403011 83F	4228
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_2	0x8001085403011 83F	4349
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_3	0x80010C5403011 83F	4470
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_4	0x8001105403011 83F	4591
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_0	0x8000015403011 83F	3437
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_1	0x8000055403011 83F	3557
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_2	0x8000095403011 83F	3678
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_3	0x80000D5403011 83F	3799
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_4	0x8000115403011 83F	3920
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_0	0x8001015403011 83F	4138
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_1	0x8001055403011 83F	4259
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_2	0x8001095403011 83F	4380
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_3	0x80010D5403011 83F	4501
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_4	0x8001115403011 83F	4622
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_0	0x8000025403011 83F	3461
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_1	0x8000065403011 83F	3582
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_2	0x80000A5403011 83F	3703
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_3	0x80000E5403011 83F	3824
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_4	0x8000125403011 83F	3945
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_0	0x8001025403011 83F	4163
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_1	0x8001065403011 83F	4284
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_2	0x80010A5403011 83F	4405
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_3	0x80010E5403011 83F	4526
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_4	0x8001125403011 83F	4647
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_0	0x8000035403011 83F	3486
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_1	0x8000075403011 83F	3607
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_2	0x80000B5403011 83F	3728
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_3	0x80000F5403011 83F	3849
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_4	0x8000135403011 83F	3970
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_0	0x8001035403011 83F	4188
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_1	0x8001075403011 83F	4309
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_2	0x80010B5403011 83F	4430
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_3	0x80010F5403011 83F	4551
DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_4	0x8001135403011 83F	4672
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_0	0x8000005503011 83F	3406

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DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_1	0x800004550301183F	3527
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_2	0x800008550301183F	3648
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_3	0x80000C550301183F	3769
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_4	0x800010550301183F	3890
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_0	0x800100550301183F	4108
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_1	0x800104550301183F	4229
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_2	0x800108550301183F	4350
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_3	0x80010C550301183F	4471
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_4	0x800110550301183F	4592
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_0	0x800001550301183F	3437
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_1	0x800005550301183F	3558
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_2	0x800009550301183F	3679
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_3	0x80000D550301183F	3800
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_4	0x800011550301183F	3921
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_0	0x800101550301183F	4139
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_1	0x800105550301183F	4260
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_2	0x800109550301183F	4381
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_3	0x80010D550301183F	4502
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_4	0x800111550301183F	4623
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_0	0x800002550301183F	3462
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_1	0x800006550301183F	3582
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_2	0x80000A550301183F	3703
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_3	0x80000E550301183F	3824
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_4	0x800012550301183F	3945
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_0	0x800102550301183F	4163
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_1	0x800106550301183F	4284
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_2	0x80010A550301183F	4405
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_3	0x80010E550301183F	4526
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_4	0x800112550301183F	4647
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_0	0x800003550301183F	3486
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_1	0x800007550301183F	3607
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_2	0x80000B550301183F	3728
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_3	0x80000F550301183F	3849
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_4	0x800013550301183F	3970
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_0	0x800103550301183F	4188
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_1	0x800107550301183F	4309
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_2	0x80010B550301183F	4430
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_3	0x80010F550301183F	4551
DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_4	0x800113550301183F	4672
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_0	0x800000560301183F	3406
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_1	0x800004560301183F	3527
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_2	0x800008560301183F	3648
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_3	0x80000C560301183F	3769
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_4	0x800010560301183F	3890
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_0	0x800100560301183F	4108
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_1	0x800104560301183F	4229
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_2	0x800108560301183F	4350
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_3	0x80010C560301183F	4471
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_4	0x800110560301183F	4592
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_0	0x800001560301183F	3438
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_1	0x800005560301183F	3558

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DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_2	0x800009560301183F	3679
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_3	0x80000D560301183F	3800
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_4	0x800011560301183F	3921
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_0	0x800101560301183F	4139
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_1	0x800105560301183F	4260
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_2	0x800109560301183F	4381
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_3	0x80010D560301183F	4502
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_4	0x800111560301183F	4623
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_0	0x800002560301183F	3462
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_1	0x800006560301183F	3583
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_2	0x80000A560301183F	3704
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_3	0x80000E560301183F	3825
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_4	0x800012560301183F	3946
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_0	0x800102560301183F	4164
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_1	0x800106560301183F	4285
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_2	0x80010A560301183F	4406
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_3	0x80010E560301183F	4527
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_4	0x800112560301183F	4648
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_0	0x800003560301183F	3487
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_1	0x800007560301183F	3608
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_2	0x80000B560301183F	3729
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_3	0x80000F560301183F	3850
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_4	0x800013560301183F	3971
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_0	0x800103560301183F	4189
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_1	0x800107560301183F	4310
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_2	0x80010B560301183F	4431
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_3	0x80010F560301183F	4552
DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_4	0x800113560301183F	4673
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_0	0x800000570301183F	3407
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_1	0x800004570301183F	3528
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_2	0x800008570301183F	3649
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_3	0x80000C570301183F	3770
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_4	0x800010570301183F	3891
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_0	0x800100570301183F	4109
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_1	0x800104570301183F	4230
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_2	0x800108570301183F	4351
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_3	0x80010C570301183F	4472
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_4	0x800110570301183F	4593
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_0	0x800001570301183F	3438
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_1	0x800005570301183F	3559
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_2	0x800009570301183F	3680
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_3	0x80000D570301183F	3801
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_4	0x800011570301183F	3922
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_0	0x800101570301183F	4140
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_1	0x800105570301183F	4261
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_2	0x800109570301183F	4382
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_3	0x80010D570301183F	4503
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_4	0x800111570301183F	4624
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_0	0x800002570301183F	3463
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_1	0x800006570301183F	3583
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_2	0x80000A570301183F	3704

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DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_3	0x80000E570301183F	3825
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_4	0x800012570301183F	3946
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_0	0x800102570301183F	4164
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_1	0x800106570301183F	4285
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_2	0x80010A570301183F	4406
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_3	0x80010E570301183F	4527
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_4	0x800112570301183F	4648
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_0	0x800003570301183F	3487
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_1	0x800007570301183F	3608
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_2	0x80000B570301183F	3729
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_3	0x80000F570301183F	3850
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_4	0x800013570301183F	3971
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_0	0x800103570301183F	4189
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_1	0x800107570301183F	4310
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_2	0x80010B570301183F	4431
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_3	0x80010F570301183F	4552
DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_4	0x800113570301183F	4673
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_0	0x8000000C0301183F	3384
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_1	0x8000040C0301183F	3505
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_2	0x8000080C0301183F	3626
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_3	0x80000C0C0301183F	3747
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_4	0x8000100C0301183F	3868
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_0	0x8001000C0301183F	4086
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_1	0x8001040C0301183F	4207
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_2	0x8001080C0301183F	4328
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_3	0x80010C0C0301183F	4449
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_4	0x8001100C0301183F	4570
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_0	0x8000010C0301183F	3426
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_1	0x8000050C0301183F	3546
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_2	0x8000090C0301183F	3667
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_3	0x80000D0C0301183F	3788
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_4	0x8000110C0301183F	3909
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_0	0x8001010C0301183F	4127
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_1	0x8001050C0301183F	4248
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_2	0x8001090C0301183F	4369
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_3	0x80010D0C0301183F	4490
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_4	0x8001110C0301183F	4611
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_0	0x8000020C0301183F	3450
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_1	0x8000060C0301183F	3571
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_2	0x80000A0C0301183F	3692
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_3	0x80000E0C0301183F	3813
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_4	0x8000120C0301183F	3934
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_0	0x8001020C0301183F	4152
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_1	0x8001060C0301183F	4273
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_2	0x80010A0C0301183F	4394
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_3	0x80010E0C0301183F	4515
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_4	0x8001120C0301183F	4636
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_0	0x8000030C0301183F	3475
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_1	0x8000070C0301183F	3596
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_2	0x80000B0C0301183F	3717
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_3	0x80000F0C0301183F	3838

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DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_4	0x8000130C0301183F	3959
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_0	0x8001030C0301183F	4177
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_1	0x8001070C0301183F	4298
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_2	0x80010B0C0301183F	4419
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_3	0x80010F0C0301183F	4540
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_4	0x8001130C0301183F	4661
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_0	0x8000000D0301183F	3385
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_1	0x8000040D0301183F	3505
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_2	0x8000080D0301183F	3626
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_3	0x80000C0D0301183F	3747
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_4	0x8000100D0301183F	3868
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_0	0x8001000D0301183F	4086
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_1	0x8001040D0301183F	4207
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_2	0x8001080D0301183F	4328
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_3	0x80010C0D0301183F	4449
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_4	0x8001100D0301183F	4570
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_0	0x8000010D0301183F	3426
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_1	0x8000050D0301183F	3547
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_2	0x8000090D0301183F	3668
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_3	0x80000D0D0301183F	3789
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_4	0x8000110D0301183F	3910
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_0	0x8001010D0301183F	4128
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_1	0x8001050D0301183F	4249
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_2	0x8001090D0301183F	4370
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_3	0x80010D0D0301183F	4491
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_4	0x8001110D0301183F	4612
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_0	0x8000020D0301183F	3451
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_1	0x8000060D0301183F	3571
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_2	0x80000A0D0301183F	3692
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_3	0x80000E0D0301183F	3813
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_4	0x8000120D0301183F	3934
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_0	0x8001020D0301183F	4152
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_1	0x8001060D0301183F	4273
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_2	0x80010A0D0301183F	4394
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_3	0x80010E0D0301183F	4515
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_4	0x8001120D0301183F	4636
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_0	0x8000030D0301183F	3475
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_1	0x8000070D0301183F	3596
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_2	0x80000B0D0301183F	3717
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_3	0x80000F0D0301183F	3838
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_4	0x8000130D0301183F	3959
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_0	0x8001030D0301183F	4177
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_1	0x8001070D0301183F	4298
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_2	0x80010B0D0301183F	4419
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_3	0x80010F0D0301183F	4540
DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_4	0x8001130D0301183F	4661
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_0	0x800000720301183F	3416
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_1	0x800004720301183F	3536
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_2	0x800008720301183F	3657
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_3	0x80000C720301183F	3778
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_4	0x800010720301183F	3899

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DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_0	0x800100720301183F	4117
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_1	0x800104720301183F	4238
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_2	0x800108720301183F	4359
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_3	0x80010C720301183F	4480
DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_4	0x800110720301183F	4601
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_0	0x800000600301183F	3408
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_1	0x800004600301183F	3529
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_2	0x800008600301183F	3650
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_3	0x80000C600301183F	3771
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_4	0x800010600301183F	3892
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_0	0x800100600301183F	4110
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_1	0x800104600301183F	4231
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_2	0x800108600301183F	4352
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_3	0x80010C600301183F	4473
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_4	0x800110600301183F	4594
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_0	0x800001600301183F	3439
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_1	0x800005600301183F	3560
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_2	0x800009600301183F	3681
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_3	0x80000D600301183F	3802
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_4	0x800011600301183F	3923
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_0	0x800101600301183F	4141
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_1	0x800105600301183F	4262
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_2	0x800109600301183F	4383
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_3	0x80010D600301183F	4504
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_4	0x800111600301183F	4625
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_0	0x800002600301183F	3464
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_1	0x800006600301183F	3585
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_2	0x80000A600301183F	3706
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_3	0x80000E600301183F	3827
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_4	0x800012600301183F	3948
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_0	0x800102600301183F	4166
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_1	0x800106600301183F	4287
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_2	0x80010A600301183F	4408
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_3	0x80010E600301183F	4529
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_4	0x800112600301183F	4650
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_0	0x800003600301183F	3488
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_1	0x800007600301183F	3609
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_2	0x80000B600301183F	3730
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_3	0x80000F600301183F	3851
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_4	0x800013600301183F	3972
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_0	0x800103600301183F	4190
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_1	0x800107600301183F	4311
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_2	0x80010B600301183F	4432
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_3	0x80010F600301183F	4553
DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_4	0x800113600301183F	4674
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_0	0x8000006A0301183F	3413
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_1	0x8000046A0301183F	3534
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_2	0x8000086A0301183F	3655
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_3	0x80000C6A0301183F	3776
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_4	0x8000106A0301183F	3897
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_0	0x8001006A0301183F	4115

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_1	0x8001046A0301183F	4236
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_2	0x8001086A0301183F	4357
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_3	0x80010C6A0301183F	4478
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_4	0x8001106A0301183F	4599
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_0	0x8000016A0301183F	3444
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_1	0x8000056A0301183F	3565
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_2	0x8000096A0301183F	3686
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_3	0x80000D6A0301183F	3807
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_4	0x8000116A0301183F	3928
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_0	0x8001016A0301183F	4146
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_1	0x8001056A0301183F	4267
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_2	0x8001096A0301183F	4388
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_3	0x80010D6A0301183F	4509
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_4	0x8001116A0301183F	4630
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_0	0x8000026A0301183F	3469
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_1	0x8000066A0301183F	3590
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_2	0x80000A6A0301183F	3711
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_3	0x80000E6A0301183F	3832
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_4	0x8000126A0301183F	3953
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_0	0x8001026A0301183F	4171
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_1	0x8001066A0301183F	4292
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_2	0x80010A6A0301183F	4413
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_3	0x80010E6A0301183F	4534
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_4	0x8001126A0301183F	4655
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_0	0x8000036A0301183F	3493
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_1	0x8000076A0301183F	3614
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_2	0x80000B6A0301183F	3735
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_3	0x80000F6A0301183F	3856
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_4	0x8000136A0301183F	3977
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_0	0x8001036A0301183F	4195
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_1	0x8001076A0301183F	4316
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_2	0x80010B6A0301183F	4437
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_3	0x80010F6A0301183F	4558
DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_4	0x8001136A0301183F	4679
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_0	0x8000006B0301183F	3414
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_1	0x8000046B0301183F	3534
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_2	0x8000086B0301183F	3655
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_3	0x80000C6B0301183F	3776
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_4	0x8000106B0301183F	3897
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_0	0x8001006B0301183F	4115
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_1	0x8001046B0301183F	4236
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_2	0x8001086B0301183F	4357
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_3	0x80010C6B0301183F	4478
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_4	0x8001106B0301183F	4599
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_0	0x8000016B0301183F	3445
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_1	0x8000056B0301183F	3566
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_2	0x8000096B0301183F	3687
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_3	0x80000D6B0301183F	3808
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_4	0x8000116B0301183F	3929
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_0	0x8001016B0301183F	4147
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_1	0x8001056B0301183F	4268

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_2	0x8001096B0301183F	4389
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_3	0x80010D6B0301183F	4510
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_4	0x8001116B0301183F	4631
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_0	0x8000026B0301183F	3469
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_1	0x8000066B0301183F	3590
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_2	0x80000A6B0301183F	3711
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_3	0x80000E6B0301183F	3832
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_4	0x8000126B0301183F	3953
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_0	0x8001026B0301183F	4171
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_1	0x8001066B0301183F	4292
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_2	0x80010A6B0301183F	4413
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_3	0x80010E6B0301183F	4534
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_4	0x8001126B0301183F	4655
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_0	0x8000036B0301183F	3494
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_1	0x8000076B0301183F	3615
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_2	0x80000B6B0301183F	3736
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_3	0x80000F6B0301183F	3857
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_4	0x8000136B0301183F	3978
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_0	0x8001036B0301183F	4196
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_1	0x8001076B0301183F	4317
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_2	0x80010B6B0301183F	4438
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_3	0x80010F6B0301183F	4559
DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_4	0x8001136B0301183F	4680
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_0	0x8000006103011 83F	3409
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_1	0x8000046103011 83F	3529
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_2	0x8000086103011 83F	3650
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_3	0x80000C6103011 83F	3771
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_4	0x8000106103011 83F	3892
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_0	0x8001006103011 83F	4110
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_1	0x8001046103011 83F	4231
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_2	0x8001086103011 83F	4352
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_3	0x80010C6103011 83F	4473
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_4	0x8001106103011 83F	4594
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_0	0x8000016103011 83F	3440
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_1	0x8000056103011 83F	3561
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_2	0x8000096103011 83F	3682
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_3	0x80000D6103011 83F	3803
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_4	0x8000116103011 83F	3924
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_0	0x8001016103011 83F	4142
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_1	0x8001056103011 83F	4263
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_2	0x8001096103011 83F	4384
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_3	0x80010D6103011 83F	4505
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_4	0x8001116103011 83F	4626
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_0	0x8000026103011 83F	3464
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_1	0x8000066103011 83F	3585
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_2	0x80000A6103011 83F	3706
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_3	0x80000E6103011 83F	3827
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_4	0x8000126103011 83F	3948
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_0	0x8001026103011 83F	4166
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_1	0x8001066103011 83F	4287
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_2	0x80010A6103011 83F	4408

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_3	0x80010E610301183F	4529
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_4	0x800112610301183F	4650
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_0	0x800003610301183F	3489
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_1	0x800007610301183F	3610
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_2	0x80000B610301183F	3731
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_3	0x80000F610301183F	3852
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_4	0x800013610301183F	3973
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_0	0x800103610301183F	4191
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_1	0x800107610301183F	4312
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_2	0x80010B610301183F	4433
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_3	0x80010F610301183F	4554
DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_4	0x800113610301183F	4675
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_0	0x800000620301183F	3409
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_1	0x800004620301183F	3530
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_2	0x800008620301183F	3651
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_3	0x80000C620301183F	3772
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_4	0x800010620301183F	3893
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_0	0x800100620301183F	4111
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_1	0x800104620301183F	4232
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_2	0x800108620301183F	4353
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_3	0x80010C620301183F	4474
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_4	0x800110620301183F	4595
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_0	0x800001620301183F	3440
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_1	0x800005620301183F	3561
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_2	0x800009620301183F	3682
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_3	0x80000D620301183F	3803
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_4	0x800011620301183F	3924
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_0	0x800101620301183F	4142
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_1	0x800105620301183F	4263
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_2	0x800109620301183F	4384
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_3	0x80010D620301183F	4505
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_4	0x800111620301183F	4626
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_0	0x800002620301183F	3465
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_1	0x800006620301183F	3586
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_2	0x80000A620301183F	3707
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_3	0x80000E620301183F	3828
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_4	0x800012620301183F	3949
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_0	0x800102620301183F	4167
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_1	0x800106620301183F	4288
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_2	0x80010A620301183F	4409
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_3	0x80010E620301183F	4530
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_4	0x800112620301183F	4651
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_0	0x800003620301183F	3489
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_1	0x800007620301183F	3610
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_2	0x80000B620301183F	3731
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_3	0x80000F620301183F	3852
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_4	0x800013620301183F	3973
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_0	0x800103620301183F	4191
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_1	0x800107620301183F	4312
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_2	0x80010B620301183F	4433
DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_3	0x80010F620301183F	4554

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_4	0x800113620301183F	4675
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_0	0x800000630301183F	3410
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_1	0x800004630301183F	3530
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_2	0x800008630301183F	3651
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_3	0x80000C630301183F	3772
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_4	0x800010630301183F	3893
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_0	0x800100630301183F	4111
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_1	0x800104630301183F	4232
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_2	0x800108630301183F	4353
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_3	0x80010C630301183F	4474
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_4	0x800110630301183F	4595
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_0	0x800001630301183F	3441
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_1	0x800005630301183F	3562
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_2	0x800009630301183F	3683
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_3	0x80000D630301183F	3804
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_4	0x800011630301183F	3925
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_0	0x800101630301183F	4143
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_1	0x800105630301183F	4264
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_2	0x800109630301183F	4385
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_3	0x80010D630301183F	4506
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_4	0x800111630301183F	4627
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_0	0x800002630301183F	3465
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_1	0x800006630301183F	3586
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_2	0x80000A630301183F	3707
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_3	0x80000E630301183F	3828
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_4	0x800012630301183F	3949
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_0	0x800102630301183F	4167
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_1	0x800106630301183F	4288
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_2	0x80010A630301183F	4409
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_3	0x80010E630301183F	4530
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_4	0x800112630301183F	4651
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_0	0x800003630301183F	3490
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_1	0x800007630301183F	3611
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_2	0x80000B630301183F	3732
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_3	0x80000F630301183F	3853
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_4	0x800013630301183F	3974
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_0	0x800103630301183F	4192
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_1	0x800107630301183F	4313
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_2	0x80010B630301183F	4434
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_3	0x80010F630301183F	4555
DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_4	0x800113630301183F	4676
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_0	0x800000640301183F	3410
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_1	0x800004640301183F	3531
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_2	0x800008640301183F	3652
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_3	0x80000C640301183F	3773
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_4	0x800010640301183F	3894
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_0	0x800100640301183F	4112
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_1	0x800104640301183F	4233
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_2	0x800108640301183F	4354
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_3	0x80010C640301183F	4475
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_4	0x800110640301183F	4596

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_0	0x800001640301183F	3441
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_1	0x800005640301183F	3562
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_2	0x800009640301183F	3683
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_3	0x80000D640301183F	3804
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_4	0x800011640301183F	3925
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_0	0x800101640301183F	4143
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_1	0x800105640301183F	4264
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_2	0x800109640301183F	4385
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_3	0x80010D640301183F	4506
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_4	0x800111640301183F	4627
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_0	0x800002640301183F	3466
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_1	0x800006640301183F	3587
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_2	0x80000A640301183F	3708
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_3	0x80000E640301183F	3829
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_4	0x800012640301183F	3950
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_0	0x800102640301183F	4168
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_1	0x800106640301183F	4289
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_2	0x80010A640301183F	4410
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_3	0x80010E640301183F	4531
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_4	0x800112640301183F	4652
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_0	0x800003640301183F	3490
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_1	0x800007640301183F	3611
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_2	0x80000B640301183F	3732
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_3	0x80000F640301183F	3853
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_4	0x800013640301183F	3974
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_0	0x800103640301183F	4192
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_1	0x800107640301183F	4313
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_2	0x80010B640301183F	4434
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_3	0x80010F640301183F	4555
DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_4	0x800113640301183F	4676
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_0	0x800000650301183F	3411
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_1	0x800004650301183F	3531
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_2	0x800008650301183F	3652
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_3	0x80000C650301183F	3773
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_4	0x800010650301183F	3894
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_0	0x800100650301183F	4112
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_1	0x800104650301183F	4233
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_2	0x800108650301183F	4354
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_3	0x80010C650301183F	4475
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_4	0x800110650301183F	4596
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_0	0x800001650301183F	3442
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_1	0x800005650301183F	3563
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_2	0x800009650301183F	3684
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_3	0x80000D650301183F	3805
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_4	0x800011650301183F	3926
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_0	0x800101650301183F	4144
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_1	0x800105650301183F	4265
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_2	0x800109650301183F	4386
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_3	0x80010D650301183F	4507
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_4	0x800111650301183F	4628
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_0	0x800002650301183F	3466

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_1	0x8000066503011 83F	3587
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_2	0x80000A650301183F	3708
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_3	0x80000E650301183F	3829
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_4	0x8000126503011 83F	3950
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_0	0x8001026503011 83F	4168
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_1	0x8001066503011 83F	4289
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_2	0x80010A650301183F	4410
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_3	0x80010E650301183F	4531
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_4	0x8001126503011 83F	4652
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_0	0x8000036503011 83F	3491
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_1	0x8000076503011 83F	3612
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_2	0x80000B650301183F	3733
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_3	0x80000F650301183F	3854
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_4	0x8000136503011 83F	3975
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_0	0x8001036503011 83F	4193
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_1	0x8001076503011 83F	4314
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_2	0x80010B650301183F	4435
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_3	0x80010F650301183F	4556
DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_4	0x8001136503011 83F	4677
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_0	0x8000006603011 83F	3411
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_1	0x8000046603011 83F	3532
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_2	0x8000086603011 83F	3653
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_3	0x80000C660301183F	3774
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_4	0x8000106603011 83F	3895
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_0	0x8001006603011 83F	4113
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_1	0x8001046603011 83F	4234
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_2	0x8001086603011 83F	4355
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_3	0x80010C660301183F	4476
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_4	0x8001106603011 83F	4597
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_0	0x8000016603011 83F	3442
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_1	0x8000056603011 83F	3563
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_2	0x8000096603011 83F	3684
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_3	0x80000D660301183F	3805
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_4	0x8000116603011 83F	3926
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_0	0x8001016603011 83F	4144
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_1	0x8001056603011 83F	4265
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_2	0x8001096603011 83F	4386
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_3	0x80010D660301183F	4507
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_4	0x8001116603011 83F	4628
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_0	0x8000026603011 83F	3467
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_1	0x8000066603011 83F	3588
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_2	0x80000A660301183F	3709
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_3	0x80000E660301183F	3830
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_4	0x8000126603011 83F	3951
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_0	0x8001026603011 83F	4169
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_1	0x8001066603011 83F	4290
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_2	0x80010A660301183F	4411
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_3	0x80010E660301183F	4532
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_4	0x8001126603011 83F	4653
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_0	0x8000036603011 83F	3491
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_1	0x8000076603011 83F	3612

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_2	0x80000B660301183F	3733
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_3	0x80000F660301183F	3854
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_4	0x800013660301183F	3975
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_0	0x800103660301183F	4193
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_1	0x800107660301183F	4314
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_2	0x80010B660301183F	4435
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_3	0x80010F660301183F	4556
DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_4	0x800113660301183F	4677
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_0	0x800000670301183F	3412
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_1	0x800004670301183F	3532
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_2	0x800008670301183F	3653
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_3	0x80000C670301183F	3774
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_4	0x800010670301183F	3895
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_0	0x800100670301183F	4113
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_1	0x800104670301183F	4234
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_2	0x800108670301183F	4355
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_3	0x80010C670301183F	4476
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_4	0x800110670301183F	4597
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_0	0x800001670301183F	3443
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_1	0x800005670301183F	3564
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_2	0x800009670301183F	3685
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_3	0x80000D670301183F	3806
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_4	0x800011670301183F	3927
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_0	0x800101670301183F	4145
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_1	0x800105670301183F	4266
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_2	0x800109670301183F	4387
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_3	0x80010D670301183F	4508
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_4	0x800111670301183F	4629
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_0	0x800002670301183F	3467
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_1	0x800006670301183F	3588
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_2	0x80000A670301183F	3709
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_3	0x80000E670301183F	3830
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_4	0x800012670301183F	3951
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_0	0x800102670301183F	4169
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_1	0x800106670301183F	4290
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_2	0x80010A670301183F	4411
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_3	0x80010E670301183F	4532
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_4	0x800112670301183F	4653
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_0	0x800003670301183F	3492
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_1	0x800007670301183F	3613
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_2	0x80000B670301183F	3734
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_3	0x80000F670301183F	3855
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_4	0x800013670301183F	3976
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_0	0x800103670301183F	4194
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_1	0x800107670301183F	4315
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_2	0x80010B670301183F	4436
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_3	0x80010F670301183F	4557
DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_4	0x800113670301183F	4678
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_0	0x800000680301183F	3412
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_1	0x800004680301183F	3533
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_2	0x800008680301183F	3654

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_3	0x80000C680301183F	3775
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_4	0x800010680301183F	3896
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_0	0x800100680301183F	4114
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_1	0x800104680301183F	4235
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_2	0x800108680301183F	4356
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_3	0x80010C680301183F	4477
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_4	0x800110680301183F	4598
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_0	0x800001680301183F	3443
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_1	0x800005680301183F	3564
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_2	0x800009680301183F	3685
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_3	0x80000D680301183F	3806
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_4	0x800011680301183F	3927
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_0	0x800101680301183F	4145
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_1	0x800105680301183F	4266
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_2	0x800109680301183F	4387
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_3	0x80010D680301183F	4508
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_4	0x800111680301183F	4629
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_0	0x800002680301183F	3468
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_1	0x800006680301183F	3589
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_2	0x80000A680301183F	3710
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_3	0x80000E680301183F	3831
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_4	0x800012680301183F	3952
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_0	0x800102680301183F	4170
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_1	0x800106680301183F	4291
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_2	0x80010A680301183F	4412
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_3	0x80010E680301183F	4533
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_4	0x800112680301183F	4654
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_0	0x800003680301183F	3492
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_1	0x800007680301183F	3613
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_2	0x80000B680301183F	3734
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_3	0x80000F680301183F	3855
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_4	0x800013680301183F	3976
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_0	0x800103680301183F	4194
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_1	0x800107680301183F	4315
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_2	0x80010B680301183F	4436
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_3	0x80010F680301183F	4557
DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_4	0x800113680301183F	4678
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_0	0x800000690301183F	3413
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_1	0x800004690301183F	3533
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_2	0x800008690301183F	3654
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_3	0x80000C690301183F	3775
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_4	0x800010690301183F	3896
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_0	0x800100690301183F	4114
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_1	0x800104690301183F	4235
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_2	0x800108690301183F	4356
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_3	0x80010C690301183F	4477
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_4	0x800110690301183F	4598
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_0	0x800001690301183F	3444
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_1	0x800005690301183F	3565
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_2	0x800009690301183F	3686
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_3	0x80000D690301183F	3807

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DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_4	0x800011690301183F	3928
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_0	0x800101690301183F	4146
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_1	0x800105690301183F	4267
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_2	0x800109690301183F	4388
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_3	0x80010D690301183F	4509
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_4	0x800111690301183F	4630
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_0	0x800002690301183F	3468
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_1	0x800006690301183F	3589
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_2	0x80000A690301183F	3710
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_3	0x80000E690301183F	3831
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_4	0x800012690301183F	3952
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_0	0x800102690301183F	4170
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_1	0x800106690301183F	4291
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_2	0x80010A690301183F	4412
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_3	0x80010E690301183F	4533
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_4	0x800112690301183F	4654
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_0	0x800003690301183F	3493
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_1	0x800007690301183F	3614
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_2	0x80000B690301183F	3735
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_3	0x80000F690301183F	3856
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_4	0x800013690301183F	3977
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_0	0x800103690301183F	4195
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_1	0x800107690301183F	4316
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_2	0x80010B690301183F	4437
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_3	0x80010F690301183F	4558
DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_4	0x800113690301183F	4679
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_0	0x800000700301183F	3415
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_1	0x800004700301183F	3536
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_2	0x800008700301183F	3657
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_3	0x80000C700301183F	3778
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_4	0x800010700301183F	3899
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_0	0x800100700301183F	4117
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_1	0x800104700301183F	4238
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_2	0x800108700301183F	4359
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_3	0x80010C700301183F	4480
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_4	0x800110700301183F	4601
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_0	0x800000710301183F	3415
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_1	0x800004710301183F	3536
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_2	0x800008710301183F	3657
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_3	0x80000C710301183F	3778
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_4	0x800010710301183F	3899
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_0	0x800100710301183F	4117
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_1	0x800104710301183F	4238
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_2	0x800108710301183F	4359
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_3	0x80010C710301183F	4480
DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_4	0x800110710301183F	4601
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_0	0x800000060301183F	3381
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_1	0x800004060301183F	3501
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_2	0x800008060301183F	3622
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_3	0x80000C060301183F	3743
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_4	0x800010060301183F	3864

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DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_0	0x800100060301183F	4082
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_1	0x800104060301183F	4203
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_2	0x800108060301183F	4324
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_3	0x80010C060301183F	4445
DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_4	0x800110060301183F	4566
DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_0	0x800000070301183F	3382
DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_1	0x800004070301183F	3502
DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_2	0x800008070301183F	3623
DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_3	0x80000C070301183F	3744
DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_4	0x800010070301183F	3865
DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_0	0x800100070301183F	4083
DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_1	0x800104070301183F	4204
DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_2	0x800108070301183F	4325
DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_3	0x80010C070301183F	4446
DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_4	0x800110070301183F	4567
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_0	0x800000730301183F	3416
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_1	0x800004730301183F	3537
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_2	0x800008730301183F	3658
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_3	0x80000C730301183F	3779
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_4	0x800010730301183F	3900
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_0	0x800100730301183F	4118
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_1	0x800104730301183F	4239
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_2	0x800108730301183F	4360
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_3	0x80010C730301183F	4481
DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_4	0x800110730301183F	4602
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_0	0x800000050301183F	3379
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_1	0x800004050301183F	3500
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_2	0x800008050301183F	3621
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_3	0x80000C050301183F	3742
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_4	0x800010050301183F	3863
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_0	0x800100050301183F	4081
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_1	0x800104050301183F	4202
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_2	0x800108050301183F	4323
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_3	0x80010C050301183F	4444
DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_4	0x800110050301183F	4565
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_0	0x800001050301183F	3424
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_1	0x800005050301183F	3544
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_2	0x800009050301183F	3665
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_3	0x80000D050301183F	3786
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_4	0x800011050301183F	3907
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_0	0x800101050301183F	4125
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_1	0x800105050301183F	4246
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_2	0x800109050301183F	4367
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_3	0x80010D050301183F	4488
DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_4	0x800111050301183F	4609
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_0	0x800002050301183F	3448
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_1	0x800006050301183F	3569
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_2	0x80000A050301183F	3690
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_3	0x80000E050301183F	3811
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_4	0x800012050301183F	3932
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_0	0x800102050301183F	4150

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DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_1	0x8001060503011 83F	4271
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_2	0x80010A050301183F	4392
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_3	0x80010E050301183F	4513
DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_4	0x8001120503011 83F	4634
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_0	0x8000030503011 83F	3473
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_1	0x8000070503011 83F	3594
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_2	0x80000B050301183F	3715
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_3	0x80000F050301183F	3836
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_4	0x8000130503011 83F	3957
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_0	0x8001030503011 83F	4175
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_1	0x8001070503011 83F	4296
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_2	0x80010B050301183F	4417
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_3	0x80010F050301183F	4538
DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_4	0x8001130503011 83F	4659
DPHY23.DDRPHY_DP18_WRCLK_PR_P0_0	0x8000007403011 83F	3416
DPHY23.DDRPHY_DP18_WRCLK_PR_P0_1	0x8000047403011 83F	3537
DPHY23.DDRPHY_DP18_WRCLK_PR_P0_2	0x8000087403011 83F	3658
DPHY23.DDRPHY_DP18_WRCLK_PR_P0_3	0x80000C740301183F	3779
DPHY23.DDRPHY_DP18_WRCLK_PR_P0_4	0x8000107403011 83F	3900
DPHY23.DDRPHY_DP18_WRCLK_PR_P1_0	0x8001007403011 83F	4118
DPHY23.DDRPHY_DP18_WRCLK_PR_P1_1	0x8001047403011 83F	4239
DPHY23.DDRPHY_DP18_WRCLK_PR_P1_2	0x8001087403011 83F	4360
DPHY23.DDRPHY_DP18_WRCLK_PR_P1_3	0x80010C740301183F	4481
DPHY23.DDRPHY_DP18_WRCLK_PR_P1_4	0x8001107403011 83F	4602
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_0	0x8000001803011 83F	3390
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_1	0x8000041803011 83F	3511
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_2	0x8000081803011 83F	3632
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_3	0x80000C180301183F	3753
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_4	0x8000101803011 83F	3874
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_0	0x8001001803011 83F	4092
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_1	0x8001041803011 83F	4213
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_2	0x8001081803011 83F	4334
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_3	0x80010C180301183F	4455
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_4	0x8001101803011 83F	4576
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_0	0x8000001903011 83F	3391
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_1	0x8000041903011 83F	3512
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_2	0x8000081903011 83F	3633
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_3	0x80000C190301183F	3754
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_4	0x8000101903011 83F	3875
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_0	0x8001001903011 83F	4093
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_1	0x8001041903011 83F	4214
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_2	0x8001081903011 83F	4335
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_3	0x80010C190301183F	4456
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_4	0x8001101903011 83F	4577
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_0	0x8000001A03011 83F	3391
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_1	0x8000041A03011 83F	3512
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_2	0x8000081A03011 83F	3633
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_3	0x80000C1A03011 83F	3754
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_4	0x8000101A03011 83F	3875
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_0	0x8001001A03011 83F	4093
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_1	0x8001041A03011 83F	4214

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DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_2	0x8001081A0301183F	4335
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_3	0x80010C1A0301183F	4456
DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_4	0x8001101A0301183F	4577
DPHY23.DDRPHY_DP18_WR_ERROR0_P0_0	0x8000001B0301183F	3392
DPHY23.DDRPHY_DP18_WR_ERROR0_P0_1	0x8000041B0301183F	3512
DPHY23.DDRPHY_DP18_WR_ERROR0_P0_2	0x8000081B0301183F	3633
DPHY23.DDRPHY_DP18_WR_ERROR0_P0_3	0x80000C1B0301183F	3754
DPHY23.DDRPHY_DP18_WR_ERROR0_P0_4	0x8000101B0301183F	3875
DPHY23.DDRPHY_DP18_WR_ERROR0_P1_0	0x8001001B0301183F	4093
DPHY23.DDRPHY_DP18_WR_ERROR0_P1_1	0x8001041B0301183F	4214
DPHY23.DDRPHY_DP18_WR_ERROR0_P1_2	0x8001081B0301183F	4335
DPHY23.DDRPHY_DP18_WR_ERROR0_P1_3	0x80010C1B0301183F	4456
DPHY23.DDRPHY_DP18_WR_ERROR0_P1_4	0x8001101B0301183F	4577
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_0	0x8000001C0301183F	3392
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_1	0x8000041C0301183F	3513
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_2	0x8000081C0301183F	3634
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_3	0x80000C1C0301183F	3755
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_4	0x8000101C0301183F	3876
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_0	0x8001001C0301183F	4094
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_1	0x8001041C0301183F	4215
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_2	0x8001081C0301183F	4336
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_3	0x80010C1C0301183F	4457
DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_4	0x8001101C0301183F	4578
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_0	0x8000001703011 83F	3390
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_1	0x8000041703011 83F	3510
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_2	0x8000081703011 83F	3631
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_3	0x80000C1703011 83F	3752
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_4	0x8000101703011 83F	3873
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_0	0x8001001703011 83F	4091
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_1	0x8001041703011 83F	4212
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_2	0x8001081703011 83F	4333
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_3	0x80010C1703011 83F	4454
DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_4	0x8001101703011 83F	4575
DPHY23.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P0	0x8000C0010301183F	4031
DPHY23.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P1	0x8001C0010301183F	4733
DPHY23.DDRPHY_PC_BASE_CNTR0_P0	0x8000C0040301183F	4033
DPHY23.DDRPHY_PC_BASE_CNTR0_P1	0x8001C0040301183F	4735
DPHY23.DDRPHY_PC_BASE_CNTR1_P0	0x8000C0060301183F	4033
DPHY23.DDRPHY_PC_BASE_CNTR1_P1	0x8001C0060301183F	4735
DPHY23.DDRPHY_PC_CAL_TIMER_P0	0x8000C0070301183F	4034
DPHY23.DDRPHY_PC_CAL_TIMER_P1	0x8001C0070301183F	4736
DPHY23.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0	0x8000C0080301183F	4034
DPHY23.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1	0x8001C0080301183F	4736
DPHY23.DDRPHY_PC_CONFIG0_P0	0x8000C00C0301183F	4036
DPHY23.DDRPHY_PC_CONFIG0_P1	0x8001C00C0301183F	4738
DPHY23.DDRPHY_PC_CONFIG1_P0	0x8000C00D0301183F	4037
DPHY23.DDRPHY_PC_CONFIG1_P1	0x8001C00D0301183F	4739
DPHY23.DDRPHY_PC_CSID_CFG_P0	0x8000C0330301183F	4049
DPHY23.DDRPHY_PC_CSID_CFG_P1	0x8001C0330301183F	4751
DPHY23.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P0	0x8000C0000301183F	4031
DPHY23.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P1	0x8001C0000301183F	4733

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DPHY23.DDRPHY_PC_ERROR_MASK0_P0	0x8000C0130301183F	4041
DPHY23.DDRPHY_PC_ERROR_MASK0_P1	0x8001C0130301183F	4743
DPHY23.DDRPHY_PC_ERROR_STATUS0_P0	0x8000C0120301183F	4040
DPHY23.DDRPHY_PC_ERROR_STATUS0_P1	0x8001C0120301183F	4742
DPHY23.DDRPHY_PC_INIT_CAL_CONFIG0_P0	0x8000C0160301183F	4042
DPHY23.DDRPHY_PC_INIT_CAL_CONFIG0_P1	0x8001C0160301183F	4744
DPHY23.DDRPHY_PC_INIT_CAL_CONFIG1_P0	0x8000C0170301183F	4043
DPHY23.DDRPHY_PC_INIT_CAL_CONFIG1_P1	0x8001C0170301183F	4745
DPHY23.DDRPHY_PC_INIT_CAL_ERROR_P0	0x8000C0180301183F	4044
DPHY23.DDRPHY_PC_INIT_CAL_ERROR_P1	0x8001C0180301183F	4746
DPHY23.DDRPHY_PC_INIT_CAL_MASK_P0	0x8000C01A0301183F	4045
DPHY23.DDRPHY_PC_INIT_CAL_MASK_P1	0x8001C01A0301183F	4747
DPHY23.DDRPHY_PC_INIT_CAL_STATUS_P0	0x8000C0190301183F	4044
DPHY23.DDRPHY_PC_INIT_CAL_STATUS_P1	0x8001C0190301183F	4746
DPHY23.DDRPHY_PC_IO_PVT_FET_CONTROL_P0	0x8000C0140301183F	4041
DPHY23.DDRPHY_PC_IO_PVT_FET_CONTROL_P1	0x8001C0140301183F	4743
DPHY23.DDRPHY_PC_IO_PVT_FET_STATUS_P0	0x8000C01B0301183F	4045
DPHY23.DDRPHY_PC_IO_PVT_FET_STATUS_P1	0x8001C01B0301183F	4747
DPHY23.DDRPHY_PC_MR0_PRI_RP0_P0	0x8000C01C0301183F	4046
DPHY23.DDRPHY_PC_MR0_PRI_RP0_P1	0x8001C01C0301183F	4748
DPHY23.DDRPHY_PC_MR0_PRI_RP1_P0	0x8000C11C0301183F	4050
DPHY23.DDRPHY_PC_MR0_PRI_RP1_P1	0x8001C11C0301183F	4752
DPHY23.DDRPHY_PC_MR0_PRI_RP2_P0	0x8000C21C0301183F	4053
DPHY23.DDRPHY_PC_MR0_PRI_RP2_P1	0x8001C21C0301183F	4755
DPHY23.DDRPHY_PC_MR0_PRI_RP3_P0	0x8000C31C0301183F	4055
DPHY23.DDRPHY_PC_MR0_PRI_RP3_P1	0x8001C31C0301183F	4757
DPHY23.DDRPHY_PC_MR0_SEC_RP0_P0	0x8000C0200301183F	4047
DPHY23.DDRPHY_PC_MR0_SEC_RP0_P1	0x8001C0200301183F	4749
DPHY23.DDRPHY_PC_MR0_SEC_RP1_P0	0x8000C1200301183F	4051
DPHY23.DDRPHY_PC_MR0_SEC_RP1_P1	0x8001C1200301183F	4753
DPHY23.DDRPHY_PC_MR0_SEC_RP2_P0	0x8000C2200301183F	4054
DPHY23.DDRPHY_PC_MR0_SEC_RP2_P1	0x8001C2200301183F	4756
DPHY23.DDRPHY_PC_MR0_SEC_RP3_P0	0x8000C3200301183F	4056
DPHY23.DDRPHY_PC_MR0_SEC_RP3_P1	0x8001C3200301183F	4758
DPHY23.DDRPHY_PC_MR1_PRI_RP0_P0	0x8000C01D0301183F	4046
DPHY23.DDRPHY_PC_MR1_PRI_RP0_P1	0x8001C01D0301183F	4748
DPHY23.DDRPHY_PC_MR1_PRI_RP1_P0	0x8000C11D0301183F	4051
DPHY23.DDRPHY_PC_MR1_PRI_RP1_P1	0x8001C11D0301183F	4753
DPHY23.DDRPHY_PC_MR1_PRI_RP2_P0	0x8000C21D0301183F	4053
DPHY23.DDRPHY_PC_MR1_PRI_RP2_P1	0x8001C21D0301183F	4755
DPHY23.DDRPHY_PC_MR1_PRI_RP3_P0	0x8000C31D0301183F	4055
DPHY23.DDRPHY_PC_MR1_PRI_RP3_P1	0x8001C31D0301183F	4757
DPHY23.DDRPHY_PC_MR1_SEC_RP0_P0	0x8000C0210301183F	4047
DPHY23.DDRPHY_PC_MR1_SEC_RP0_P1	0x8001C0210301183F	4749
DPHY23.DDRPHY_PC_MR1_SEC_RP1_P0	0x8000C1210301183F	4052
DPHY23.DDRPHY_PC_MR1_SEC_RP1_P1	0x8001C1210301183F	4754
DPHY23.DDRPHY_PC_MR1_SEC_RP2_P0	0x8000C2210301183F	4054
DPHY23.DDRPHY_PC_MR1_SEC_RP2_P1	0x8001C2210301183F	4756
DPHY23.DDRPHY_PC_MR1_SEC_RP3_P0	0x8000C3210301183F	4057
DPHY23.DDRPHY_PC_MR1_SEC_RP3_P1	0x8001C3210301183F	4759
DPHY23.DDRPHY_PC_MR2_PRI_RP0_P0	0x8000C01E0301183F	4046

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DPHY23.DDRPHY_PC_MR2_PRI_RP0_P1	0x8001C01E0301183F	4748
DPHY23.DDRPHY_PC_MR2_PRI_RP1_P0	0x8000C11E0301183F	4051
DPHY23.DDRPHY_PC_MR2_PRI_RP1_P1	0x8001C11E0301183F	4753
DPHY23.DDRPHY_PC_MR2_PRI_RP2_P0	0x8000C21E0301183F	4053
DPHY23.DDRPHY_PC_MR2_PRI_RP2_P1	0x8001C21E0301183F	4755
DPHY23.DDRPHY_PC_MR2_PRI_RP3_P0	0x8000C31E0301183F	4056
DPHY23.DDRPHY_PC_MR2_PRI_RP3_P1	0x8001C31E0301183F	4758
DPHY23.DDRPHY_PC_MR2_SEC_RP0_P0	0x8000C0220301183F	4047
DPHY23.DDRPHY_PC_MR2_SEC_RP0_P1	0x8001C0220301183F	4749
DPHY23.DDRPHY_PC_MR2_SEC_RP1_P0	0x8000C1220301183F	4052
DPHY23.DDRPHY_PC_MR2_SEC_RP1_P1	0x8001C1220301183F	4754
DPHY23.DDRPHY_PC_MR2_SEC_RP2_P0	0x8000C2220301183F	4055
DPHY23.DDRPHY_PC_MR2_SEC_RP2_P1	0x8001C2220301183F	4757
DPHY23.DDRPHY_PC_MR2_SEC_RP3_P0	0x8000C3220301183F	4057
DPHY23.DDRPHY_PC_MR2_SEC_RP3_P1	0x8001C3220301183F	4759
DPHY23.DDRPHY_PC_MR3_PRI_RP0_P0	0x8000C01F0301183F	4046
DPHY23.DDRPHY_PC_MR3_PRI_RP0_P1	0x8001C01F0301183F	4748
DPHY23.DDRPHY_PC_MR3_PRI_RP1_P0	0x8000C11F0301183F	4051
DPHY23.DDRPHY_PC_MR3_PRI_RP1_P1	0x8001C11F0301183F	4753
DPHY23.DDRPHY_PC_MR3_PRI_RP2_P0	0x8000C21F0301183F	4054
DPHY23.DDRPHY_PC_MR3_PRI_RP2_P1	0x8001C21F0301183F	4756
DPHY23.DDRPHY_PC_MR3_PRI_RP3_P0	0x8000C31F0301183F	4056
DPHY23.DDRPHY_PC_MR3_PRI_RP3_P1	0x8001C31F0301183F	4758
DPHY23.DDRPHY_PC_MR3_SEC_RP0_P0	0x8000C0230301183F	4048
DPHY23.DDRPHY_PC_MR3_SEC_RP0_P1	0x8001C0230301183F	4750
DPHY23.DDRPHY_PC_MR3_SEC_RP1_P0	0x8000C1230301183F	4052
DPHY23.DDRPHY_PC_MR3_SEC_RP1_P1	0x8001C1230301183F	4754
DPHY23.DDRPHY_PC_MR3_SEC_RP2_P0	0x8000C2230301183F	4055
DPHY23.DDRPHY_PC_MR3_SEC_RP2_P1	0x8001C2230301183F	4757
DPHY23.DDRPHY_PC_MR3_SEC_RP3_P0	0x8000C3230301183F	4057
DPHY23.DDRPHY_PC_MR3_SEC_RP3_P1	0x8001C3230301183F	4759
DPHY23.DDRPHY_PC_PER_CAL_CONFIG_P0	0x8000C00B0301183F	4035
DPHY23.DDRPHY_PC_PER_CAL_CONFIG_P1	0x8001C00B0301183F	4737
DPHY23.DDRPHY_PC_PER_ZCAL_CONFIG_P0	0x8000C00F0301183F	4038
DPHY23.DDRPHY_PC_PER_ZCAL_CONFIG_P1	0x8001C00F0301183F	4740
DPHY23.DDRPHY_PC_POWERDOWN_1_P0	0x8000C0100301183F	4038
DPHY23.DDRPHY_PC_POWERDOWN_1_P1	0x8001C0100301183F	4740
DPHY23.DDRPHY_PC_RANK_GROUP_EXT_P0	0x8000C0350301183F	4050
DPHY23.DDRPHY_PC_RANK_GROUP_EXT_P1	0x8001C0350301183F	4752
DPHY23.DDRPHY_PC_RANK_GROUP_P0	0x8000C0110301183F	4039
DPHY23.DDRPHY_PC_RANK_GROUP_P1	0x8001C0110301183F	4741
DPHY23.DDRPHY_PC_RANK_PAIR0_P0	0x8000C0020301183F	4032
DPHY23.DDRPHY_PC_RANK_PAIR0_P1	0x8001C0020301183F	4734
DPHY23.DDRPHY_PC_RANK_PAIR1_P0	0x8000C0030301183F	4032
DPHY23.DDRPHY_PC_RANK_PAIR1_P1	0x8001C0030301183F	4734
DPHY23.DDRPHY_PC_RANK_PAIR2_P0	0x8000C0300301183F	4048
DPHY23.DDRPHY_PC_RANK_PAIR2_P1	0x8001C0300301183F	4750
DPHY23.DDRPHY_PC_RANK_PAIR3_P0	0x8000C0310301183F	4049
DPHY23.DDRPHY_PC_RANK_PAIR3_P1	0x8001C0310301183F	4751
DPHY23.DDRPHY_PC_RELOAD_VALUE0_P0	0x8000C0050301183F	4033
DPHY23.DDRPHY_PC_RELOAD_VALUE0_P1	0x8001C0050301183F	4735

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DPHY23.DDRPHY_PC_RESETS_P0	0x8000C00E0301183F	4038
DPHY23.DDRPHY_PC_RESETS_P1	0x8001C00E0301183F	4740
DPHY23.DDRPHY_PC_VREF_DRV_CONTROL_P0	0x8000C0150301183F	4041
DPHY23.DDRPHY_PC_VREF_DRV_CONTROL_P1	0x8001C0150301183F	4743
DPHY23.DDRPHY_PC_ZCAL_TIMER_P0	0x8000C0090301183F	4034
DPHY23.DDRPHY_PC_ZCAL_TIMER_P1	0x8001C0090301183F	4736
DPHY23.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0	0x8000C00A0301183F	4035
DPHY23.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1	0x8001C00A0301183F	4737
DPHY23.DDRPHY_RC_CONFIG0_P0	0x8000C8000301183F	4069
DPHY23.DDRPHY_RC_CONFIG0_P1	0x8001C8000301183F	4771
DPHY23.DDRPHY_RC_CONFIG1_P0	0x8000C8010301183F	4070
DPHY23.DDRPHY_RC_CONFIG1_P1	0x8001C8010301183F	4772
DPHY23.DDRPHY_RC_CONFIG2_P0	0x8000C8020301183F	4070
DPHY23.DDRPHY_RC_CONFIG2_P1	0x8001C8020301183F	4772
DPHY23.DDRPHY_RC_CONFIG3_P0	0x8000C8070301183F	4071
DPHY23.DDRPHY_RC_CONFIG3_P1	0x8001C8070301183F	4773
DPHY23.DDRPHY_RC_ERROR_MASK0_P0	0x8000C8060301183F	4071
DPHY23.DDRPHY_RC_ERROR_MASK0_P1	0x8001C8060301183F	4773
DPHY23.DDRPHY_RC_ERROR_STATUS0_P0	0x8000C8050301183F	4071
DPHY23.DDRPHY_RC_ERROR_STATUS0_P1	0x8001C8050301183F	4773
DPHY23.DDRPHY_SEQ_CONFIG0_P0	0x8000C4020301183F	4059
DPHY23.DDRPHY_SEQ_CONFIG0_P1	0x8001C4020301183F	4761
DPHY23.DDRPHY_SEQ_ERROR_MASK0_P0	0x8000C4090301183F	4062
DPHY23.DDRPHY_SEQ_ERROR_MASK0_P1	0x8001C4090301183F	4764
DPHY23.DDRPHY_SEQ_ERROR_STATUS0_P0	0x8000C4080301183F	4061
DPHY23.DDRPHY_SEQ_ERROR_STATUS0_P1	0x8001C4080301183F	4763
DPHY23.DDRPHY_SEQ_LPT_ADDR2_P0	0x8000C4170301183F	4066
DPHY23.DDRPHY_SEQ_LPT_ADDR2_P1	0x8001C4170301183F	4768
DPHY23.DDRPHY_SEQ_LPT_ADDR3_P0	0x8000C4180301183F	4066
DPHY23.DDRPHY_SEQ_LPT_ADDR3_P1	0x8001C4180301183F	4768
DPHY23.DDRPHY_SEQ_LPT_ADDR4_P0	0x8000C4190301183F	4067
DPHY23.DDRPHY_SEQ_LPT_ADDR4_P1	0x8001C4190301183F	4769
DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM0_P0	0x8000C4120301183F	4065
DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM0_P1	0x8001C4120301183F	4767
DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM1_P0	0x8000C4130301183F	4065
DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM1_P1	0x8001C4130301183F	4767
DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM2_P0	0x8000C4140301183F	4065
DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM2_P1	0x8001C4140301183F	4767
DPHY23.DDRPHY_SEQ_ODT_DEFAULT_CFG_P0	0x8000C4240301183F	4068
DPHY23.DDRPHY_SEQ_ODT_DEFAULT_CFG_P1	0x8001C4240301183F	4770
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG0_P0	0x8000C40E0301183F	4063
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG0_P1	0x8001C40E0301183F	4765
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG1_P0	0x8000C40F0301183F	4064
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG1_P1	0x8001C40F0301183F	4766
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG2_P0	0x8000C4100301183F	4064
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG2_P1	0x8001C4100301183F	4766
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG3_P0	0x8000C4110301183F	4064
DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG3_P1	0x8001C4110301183F	4766
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG0_P0	0x8000C40A0301183F	4062
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG0_P1	0x8001C40A0301183F	4764
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG1_P0	0x8000C40B0301183F	4062

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DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG1_P1	0x8001C40B0301183F	4764
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG2_P0	0x8000C40C0301183F	4063
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG2_P1	0x8001C40C0301183F	4765
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG3_P0	0x8000C40D0301183F	4063
DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG3_P1	0x8001C40D0301183F	4765
DPHY23.DDRPHY_SEQ_RD_WR_DATA0_P0	0x8000C4000301183F	4058
DPHY23.DDRPHY_SEQ_RD_WR_DATA0_P1	0x8001C4000301183F	4760
DPHY23.DDRPHY_SEQ_RD_WR_DATA1_P0	0x8000C4010301183F	4058
DPHY23.DDRPHY_SEQ_RD_WR_DATA1_P1	0x8001C4010301183F	4760
DPHY23.DDRPHY_SEQ_RESERVED_ADDR0_P0	0x8000C4030301183F	4060
DPHY23.DDRPHY_SEQ_RESERVED_ADDR0_P1	0x8001C4030301183F	4762
DPHY23.DDRPHY_SEQ_RESERVED_ADDR1_P0	0x8000C4040301183F	4060
DPHY23.DDRPHY_SEQ_RESERVED_ADDR1_P1	0x8001C4040301183F	4762
DPHY23.DDRPHY_SEQ_RESERVED_ADDR2_P0	0x8000C4050301183F	4060
DPHY23.DDRPHY_SEQ_RESERVED_ADDR2_P1	0x8001C4050301183F	4762
DPHY23.DDRPHY_SEQ_RESERVED_ADDR3_P0	0x8000C4060301183F	4061
DPHY23.DDRPHY_SEQ_RESERVED_ADDR3_P1	0x8001C4060301183F	4763
DPHY23.DDRPHY_SEQ_RESERVED_ADDR4_P0	0x8000C4070301183F	4061
DPHY23.DDRPHY_SEQ_RESERVED_ADDR4_P1	0x8001C4070301183F	4763
DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0	0x8000C41A0301183F	4067
DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1	0x8001C41A0301183F	4769
DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0	0x8000C41B0301183F	4068
DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1	0x8001C41B0301183F	4770
DPHY23.DDRPHY_WC_CONFIG0_P0	0x8000CC000301183F	4072
DPHY23.DDRPHY_WC_CONFIG0_P1	0x8001CC000301183F	4774
DPHY23.DDRPHY_WC_CONFIG1_P0	0x8000CC010301183F	4072
DPHY23.DDRPHY_WC_CONFIG1_P1	0x8001CC010301183F	4774
DPHY23.DDRPHY_WC_CONFIG2_P0	0x8000CC020301183F	4073
DPHY23.DDRPHY_WC_CONFIG2_P1	0x8001CC020301183F	4775
DPHY23.DDRPHY_WC_CONFIG3_P0	0x8000CC050301183F	4074
DPHY23.DDRPHY_WC_CONFIG3_P1	0x8001CC050301183F	4776
DPHY23.DDRPHY_WC_ERROR_MASK0_P0	0x8000CC040301183F	4073
DPHY23.DDRPHY_WC_ERROR_MASK0_P1	0x8001CC040301183F	4775
DPHY23.DDRPHY_WC_ERROR_STATUS0_P0	0x8000CC030301183F	4073
DPHY23.DDRPHY_WC_ERROR_STATUS0_P1	0x8001CC030301183F	4775
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_0	0x800000380301183F	3397
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_1	0x800004380301183F	3517
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_2	0x800008380301183F	3638
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_3	0x80000C380301183F	3759
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_4	0x800010380301183F	3880
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_0	0x800100380301183F	4098
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_1	0x800104380301183F	4219
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_2	0x800108380301183F	4340
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_3	0x80010C380301183F	4461
DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_4	0x800110380301183F	4582
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_0	0x800001380301183F	3428
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_1	0x800005380301183F	3549
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_2	0x800009380301183F	3670
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_3	0x80000D380301183F	3791
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_4	0x800011380301183F	3912
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_0	0x800101380301183F	4130

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DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_1	0x800105380301183F	4251
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_2	0x800109380301183F	4372
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_3	0x80010D380301183F	4493
DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_4	0x800111380301183F	4614
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_0	0x800002380301183F	3452
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_1	0x800006380301183F	3573
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_2	0x80000A380301183F	3694
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_3	0x80000E380301183F	3815
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_4	0x800012380301183F	3936
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_0	0x800102380301183F	4154
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_1	0x800106380301183F	4275
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_2	0x80010A380301183F	4396
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_3	0x80010E380301183F	4517
DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_4	0x800112380301183F	4638
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_0	0x800003380301183F	3477
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_1	0x800007380301183F	3598
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_2	0x80000B380301183F	3719
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_3	0x80000F380301183F	3840
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_4	0x800013380301183F	3961
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_0	0x800103380301183F	4179
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_1	0x800107380301183F	4300
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_2	0x80010B380301183F	4421
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_3	0x80010F380301183F	4542
DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_4	0x800113380301183F	4663
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_0	0x800000420301183F	3400
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_1	0x800004420301183F	3521
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_2	0x800008420301183F	3642
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_3	0x80000C420301183F	3763
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_4	0x800010420301183F	3884
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_0	0x800100420301183F	4102
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_1	0x800104420301183F	4223
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_2	0x800108420301183F	4344
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_3	0x80010C420301183F	4465
DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_4	0x800110420301183F	4586
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_0	0x800001420301183F	3431
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_1	0x800005420301183F	3552
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_2	0x800009420301183F	3673
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_3	0x80000D420301183F	3794
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_4	0x800011420301183F	3915
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_0	0x800101420301183F	4133
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_1	0x800105420301183F	4254
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_2	0x800109420301183F	4375
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_3	0x80010D420301183F	4496
DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_4	0x800111420301183F	4617
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_0	0x800002420301183F	3456
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_1	0x800006420301183F	3577
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_2	0x80000A420301183F	3698
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_3	0x80000E420301183F	3819
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_4	0x800012420301183F	3940
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_0	0x800102420301183F	4158
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_1	0x800106420301183F	4279

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DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_2	0x80010A420301183F	4400
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_3	0x80010E420301183F	4521
DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_4	0x800112420301183F	4642
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_0	0x800003420301183F	3480
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_1	0x800007420301183F	3601
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_2	0x80000B420301183F	3722
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_3	0x80000F420301183F	3843
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_4	0x800013420301183F	3964
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_0	0x800103420301183F	4182
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_1	0x800107420301183F	4303
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_2	0x80010B420301183F	4424
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_3	0x80010F420301183F	4545
DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_4	0x800113420301183F	4666
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_0	0x800000430301183F	3400
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_1	0x800004430301183F	3521
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_2	0x800008430301183F	3642
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_3	0x80000C430301183F	3763
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_4	0x800010430301183F	3884
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_0	0x800100430301183F	4102
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_1	0x800104430301183F	4223
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_2	0x800108430301183F	4344
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_3	0x80010C430301183F	4465
DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_4	0x800110430301183F	4586
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_0	0x800001430301183F	3432
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_1	0x800005430301183F	3552
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_2	0x800009430301183F	3673
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_3	0x80000D430301183F	3794
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_4	0x800011430301183F	3915
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_0	0x800101430301183F	4133
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_1	0x800105430301183F	4254
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_2	0x800109430301183F	4375
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_3	0x80010D430301183F	4496
DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_4	0x800111430301183F	4617
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_0	0x800002430301183F	3456
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_1	0x800006430301183F	3577
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_2	0x80000A430301183F	3698
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_3	0x80000E430301183F	3819
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_4	0x800012430301183F	3940
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_0	0x800102430301183F	4158
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_1	0x800106430301183F	4279
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_2	0x80010A430301183F	4400
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_3	0x80010E430301183F	4521
DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_4	0x800112430301183F	4642
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_0	0x800003430301183F	3481
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_1	0x800007430301183F	3602
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_2	0x80000B430301183F	3723
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_3	0x80000F430301183F	3844
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_4	0x800013430301183F	3965
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_0	0x800103430301183F	4183
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_1	0x800107430301183F	4304
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_2	0x80010B430301183F	4425

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DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_3	0x80010F430301183F	4546
DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_4	0x800113430301183F	4667
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_0	0x800000440301183F	3401
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_1	0x800004440301183F	3521
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_2	0x800008440301183F	3642
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_3	0x80000C440301183F	3763
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_4	0x800010440301183F	3884
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_0	0x800100440301183F	4102
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_1	0x800104440301183F	4223
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_2	0x800108440301183F	4344
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_3	0x80010C440301183F	4465
DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_4	0x800110440301183F	4586
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_0	0x800001440301183F	3432
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_1	0x800005440301183F	3553
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_2	0x800009440301183F	3674
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_3	0x80000D440301183F	3795
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_4	0x800011440301183F	3916
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_0	0x800101440301183F	4134
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_1	0x800105440301183F	4255
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_2	0x800109440301183F	4376
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_3	0x80010D440301183F	4497
DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_4	0x800111440301183F	4618
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_0	0x800002440301183F	3456
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_1	0x800006440301183F	3577
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_2	0x80000A440301183F	3698
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_3	0x80000E440301183F	3819
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_4	0x800012440301183F	3940
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_0	0x800102440301183F	4158
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_1	0x800106440301183F	4279
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_2	0x80010A440301183F	4400
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_3	0x80010E440301183F	4521
DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_4	0x800112440301183F	4642
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_0	0x800003440301183F	3481
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_1	0x800007440301183F	3602
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_2	0x80000B440301183F	3723
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_3	0x80000F440301183F	3844
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_4	0x800013440301183F	3965
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_0	0x800103440301183F	4183
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_1	0x800107440301183F	4304
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_2	0x80010B440301183F	4425
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_3	0x80010F440301183F	4546
DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_4	0x800113440301183F	4667
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_0	0x800000450301183F	3401
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_1	0x800004450301183F	3522
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_2	0x800008450301183F	3643
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_3	0x80000C450301183F	3764
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_4	0x800010450301183F	3885
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_0	0x800100450301183F	4103
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_1	0x800104450301183F	4224
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_2	0x800108450301183F	4345
DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_3	0x80010C450301183F	4466

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DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_4	0x800110450301183F	4587
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_0	0x800001450301183F	3432
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_1	0x800005450301183F	3553
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_2	0x800009450301183F	3674
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_3	0x80000D450301183F	3795
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_4	0x800011450301183F	3916
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_0	0x800101450301183F	4134
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_1	0x800105450301183F	4255
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_2	0x800109450301183F	4376
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_3	0x80010D450301183F	4497
DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_4	0x800111450301183F	4618
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_0	0x800002450301183F	3457
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_1	0x800006450301183F	3578
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_2	0x80000A450301183F	3699
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_3	0x80000E450301183F	3820
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_4	0x800012450301183F	3941
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_0	0x800102450301183F	4159
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_1	0x800106450301183F	4280
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_2	0x80010A450301183F	4401
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_3	0x80010E450301183F	4522
DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_4	0x800112450301183F	4643
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_0	0x800003450301183F	3481
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_1	0x800007450301183F	3602
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_2	0x80000B450301183F	3723
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_3	0x80000F450301183F	3844
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_4	0x800013450301183F	3965
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_0	0x800103450301183F	4183
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_1	0x800107450301183F	4304
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_2	0x80010B450301183F	4425
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_3	0x80010F450301183F	4546
DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_4	0x800113450301183F	4667
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_0	0x800000460301183F	3401
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_1	0x800004460301183F	3522
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_2	0x800008460301183F	3643
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_3	0x80000C460301183F	3764
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_4	0x800010460301183F	3885
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_0	0x800100460301183F	4103
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_1	0x800104460301183F	4224
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_2	0x800108460301183F	4345
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_3	0x80010C460301183F	4466
DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_4	0x800110460301183F	4587
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_0	0x800001460301183F	3433
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_1	0x800005460301183F	3553
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_2	0x800009460301183F	3674
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_3	0x80000D460301183F	3795
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_4	0x800011460301183F	3916
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_0	0x800101460301183F	4134
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_1	0x800105460301183F	4255
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_2	0x800109460301183F	4376
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_3	0x80010D460301183F	4497
DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_4	0x800111460301183F	4618

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DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_0	0x8000024603011 83F	3457
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_1	0x8000064603011 83F	3578
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_2	0x80000A4603011 83F	3699
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_3	0x80000E4603011 83F	3820
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_4	0x8000124603011 83F	3941
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_0	0x8001024603011 83F	4159
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_1	0x8001064603011 83F	4280
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_2	0x80010A4603011 83F	4401
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_3	0x80010E4603011 83F	4522
DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_4	0x8001124603011 83F	4643
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_0	0x8000034603011 83F	3482
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_1	0x8000074603011 83F	3603
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_2	0x80000B4603011 83F	3724
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_3	0x80000F4603011 83F	3845
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_4	0x8000134603011 83F	3966
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_0	0x8001034603011 83F	4184
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_1	0x8001074603011 83F	4305
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_2	0x80010B4603011 83F	4426
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_3	0x80010F4603011 83F	4547
DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_4	0x8001134603011 83F	4668
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_0	0x8000004703011 83F	3402
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_1	0x8000044703011 83F	3522
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_2	0x8000084703011 83F	3643
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_3	0x80000C4703011 83F	3764
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_4	0x8000104703011 83F	3885
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_0	0x8001004703011 83F	4103
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_1	0x8001044703011 83F	4224
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_2	0x8001084703011 83F	4345
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_3	0x80010C4703011 83F	4466
DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_4	0x8001104703011 83F	4587
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_0	0x8000014703011 83F	3433
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_1	0x8000054703011 83F	3554
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_2	0x8000094703011 83F	3675
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_3	0x80000D4703011 83F	3796
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_4	0x8000114703011 83F	3917
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_0	0x8001014703011 83F	4135
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_1	0x8001054703011 83F	4256
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_2	0x8001094703011 83F	4377
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_3	0x80010D4703011 83F	4498
DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_4	0x8001114703011 83F	4619
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_0	0x8000024703011 83F	3457
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_1	0x8000064703011 83F	3578
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_2	0x80000A4703011 83F	3699
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_3	0x80000E4703011 83F	3820
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_4	0x8000124703011 83F	3941
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_0	0x8001024703011 83F	4159
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_1	0x8001064703011 83F	4280
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_2	0x80010A4703011 83F	4401
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_3	0x80010E4703011 83F	4522
DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_4	0x8001124703011 83F	4643
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_0	0x8000034703011 83F	3482

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DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_1	0x8000074703011 83F	3603
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_2	0x80000B4703011 83F	3724
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_3	0x80000F4703011 83F	3845
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_4	0x8000134703011 83F	3966
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_0	0x8001034703011 83F	4184
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_1	0x8001074703011 83F	4305
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_2	0x80010B4703011 83F	4426
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_3	0x80010F4703011 83F	4547
DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_4	0x8001134703011 83F	4668
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_0	0x8000004803011 83F	3402
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_1	0x8000044803011 83F	3523
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_2	0x8000084803011 83F	3644
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_3	0x80000C4803011 83F	3765
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_4	0x8000104803011 83F	3886
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_0	0x8001004803011 83F	4104
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_1	0x8001044803011 83F	4225
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_2	0x8001084803011 83F	4346
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_3	0x80010C4803011 83F	4467
DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_4	0x8001104803011 83F	4588
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_0	0x8000014803011 83F	3433
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_1	0x8000054803011 83F	3554
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_2	0x8000094803011 83F	3675
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_3	0x80000D4803011 83F	3796
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_4	0x8000114803011 83F	3917
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_0	0x8001014803011 83F	4135
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_1	0x8001054803011 83F	4256
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_2	0x8001094803011 83F	4377
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_3	0x80010D4803011 83F	4498
DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_4	0x8001114803011 83F	4619
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_0	0x8000024803011 83F	3458
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_1	0x8000064803011 83F	3579
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_2	0x80000A4803011 83F	3700
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_3	0x80000E4803011 83F	3821
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_4	0x8000124803011 83F	3942
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_0	0x8001024803011 83F	4160
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_1	0x8001064803011 83F	4281
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_2	0x80010A4803011 83F	4402
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_3	0x80010E4803011 83F	4523
DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_4	0x8001124803011 83F	4644
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_0	0x8000034803011 83F	3482
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_1	0x8000074803011 83F	3603
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_2	0x80000B4803011 83F	3724
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_3	0x80000F4803011 83F	3845
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_4	0x8000134803011 83F	3966
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_0	0x8001034803011 83F	4184
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_1	0x8001074803011 83F	4305
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_2	0x80010B4803011 83F	4426
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_3	0x80010F4803011 83F	4547
DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_4	0x8001134803011 83F	4668
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_0	0x8000004A0301183F	3402
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_1	0x8000044A0301183F	3523

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DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_2	0x8000084A0301183F	3644
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_3	0x80000C4A0301183F	3765
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_4	0x8000104A0301183F	3886
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_0	0x8001004A0301183F	4104
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_1	0x8001044A0301183F	4225
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_2	0x8001084A0301183F	4346
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_3	0x80010C4A0301183F	4467
DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_4	0x8001104A0301183F	4588
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_0	0x8000014A0301183F	3434
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_1	0x8000054A0301183F	3554
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_2	0x8000094A0301183F	3675
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_3	0x80000D4A0301183F	3796
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_4	0x8000114A0301183F	3917
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_0	0x8001014A0301183F	4135
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_1	0x8001054A0301183F	4256
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_2	0x8001094A0301183F	4377
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_3	0x80010D4A0301183F	4498
DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_4	0x8001114A0301183F	4619
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_0	0x8000024A0301183F	3458
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_1	0x8000064A0301183F	3579
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_2	0x80000A4A0301183F	3700
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_3	0x80000E4A0301183F	3821
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_4	0x8000124A0301183F	3942
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_0	0x8001024A0301183F	4160
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_1	0x8001064A0301183F	4281
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_2	0x80010A4A0301183F	4402
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_3	0x80010E4A0301183F	4523
DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_4	0x8001124A0301183F	4644
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_0	0x8000034A0301183F	3483
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_1	0x8000074A0301183F	3604
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_2	0x80000B4A0301183F	3725
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_3	0x80000F4A0301183F	3846
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_4	0x8000134A0301183F	3967
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_0	0x8001034A0301183F	4185
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_1	0x8001074A0301183F	4306
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_2	0x80010B4A0301183F	4427
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_3	0x80010F4A0301183F	4548
DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_4	0x8001134A0301183F	4669
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_0	0x800000390301183F	3397
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_1	0x800004390301183F	3518
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_2	0x800008390301183F	3639
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_3	0x80000C390301183F	3760
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_4	0x800010390301183F	3881
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_0	0x800100390301183F	4099
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_1	0x800104390301183F	4220
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_2	0x800108390301183F	4341
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_3	0x80010C390301183F	4462
DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_4	0x800110390301183F	4583
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_0	0x800001390301183F	3428
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_1	0x800005390301183F	3549
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_2	0x800009390301183F	3670

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DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_3	0x80000D390301183F	3791
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_4	0x800011390301183F	3912
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_0	0x800101390301183F	4130
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_1	0x800105390301183F	4251
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_2	0x800109390301183F	4372
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_3	0x80010D390301183F	4493
DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_4	0x800111390301183F	4614
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_0	0x800002390301183F	3453
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_1	0x800006390301183F	3574
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_2	0x80000A390301183F	3695
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_3	0x80000E390301183F	3816
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_4	0x800012390301183F	3937
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_0	0x800102390301183F	4155
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_1	0x800106390301183F	4276
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_2	0x80010A390301183F	4397
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_3	0x80010E390301183F	4518
DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_4	0x800112390301183F	4639
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_0	0x800003390301183F	3477
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_1	0x800007390301183F	3598
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_2	0x80000B390301183F	3719
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_3	0x80000F390301183F	3840
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_4	0x800013390301183F	3961
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_0	0x800103390301183F	4179
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_1	0x800107390301183F	4300
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_2	0x80010B390301183F	4421
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_3	0x80010F390301183F	4542
DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_4	0x800113390301183F	4663
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_0	0x8000004C0301183F	3403
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_1	0x8000044C0301183F	3523
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_2	0x8000084C0301183F	3644
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_3	0x80000C4C0301183F	3765
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_4	0x8000104C0301183F	3886
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_0	0x8001004C0301183F	4104
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_1	0x8001044C0301183F	4225
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_2	0x8001084C0301183F	4346
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_3	0x80010C4C0301183F	4467
DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_4	0x8001104C0301183F	4588
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_0	0x8000014C0301183F	3434
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_1	0x8000054C0301183F	3555
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_2	0x8000094C0301183F	3676
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_3	0x80000D4C0301183F	3797
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_4	0x8000114C0301183F	3918
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_0	0x8001014C0301183F	4136
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_1	0x8001054C0301183F	4257
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_2	0x8001094C0301183F	4378
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_3	0x80010D4C0301183F	4499
DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_4	0x8001114C0301183F	4620
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_0	0x8000024C0301183F	3458
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_1	0x8000064C0301183F	3579
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_2	0x80000A4C0301183F	3700
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_3	0x80000E4C0301183F	3821

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DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_4	0x8000124C0301183F	3942
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_0	0x8001024C0301183F	4160
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_1	0x8001064C0301183F	4281
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_2	0x80010A4C0301183F	4402
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_3	0x80010E4C0301183F	4523
DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_4	0x8001124C0301183F	4644
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_0	0x8000034C0301183F	3483
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_1	0x8000074C0301183F	3604
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_2	0x80000B4C0301183F	3725
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_3	0x80000F4C0301183F	3846
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_4	0x8000134C0301183F	3967
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_0	0x8001034C0301183F	4185
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_1	0x8001074C0301183F	4306
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_2	0x80010B4C0301183F	4427
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_3	0x80010F4C0301183F	4548
DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_4	0x8001134C0301183F	4669
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_0	0x8000004E0301183F	3403
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_1	0x8000044E0301183F	3524
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_2	0x8000084E0301183F	3645
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_3	0x80000C4E0301183F	3766
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_4	0x8000104E0301183F	3887
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_0	0x8001004E0301183F	4105
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_1	0x8001044E0301183F	4226
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_2	0x8001084E0301183F	4347
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_3	0x80010C4E0301183F	4468
DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_4	0x8001104E0301183F	4589
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_0	0x8000014E0301183F	3434
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_1	0x8000054E0301183F	3555
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_2	0x8000094E0301183F	3676
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_3	0x80000D4E0301183F	3797
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_4	0x8000114E0301183F	3918
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_0	0x8001014E0301183F	4136
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_1	0x8001054E0301183F	4257
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_2	0x8001094E0301183F	4378
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_3	0x80010D4E0301183F	4499
DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_4	0x8001114E0301183F	4620
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_0	0x8000024E0301183F	3459
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_1	0x8000064E0301183F	3580
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_2	0x80000A4E0301183F	3701
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_3	0x80000E4E0301183F	3822
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_4	0x8000124E0301183F	3943
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_0	0x8001024E0301183F	4161
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_1	0x8001064E0301183F	4282
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_2	0x80010A4E0301183F	4403
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_3	0x80010E4E0301183F	4524
DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_4	0x8001124E0301183F	4645
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_0	0x8000034E0301183F	3483
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_1	0x8000074E0301183F	3604
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_2	0x80000B4E0301183F	3725
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_3	0x80000F4E0301183F	3846
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_4	0x8000134E0301183F	3967

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DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_0	0x8001034E0301183F	4185
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_1	0x8001074E0301183F	4306
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_2	0x80010B4E0301183F	4427
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_3	0x80010F4E0301183F	4548
DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_4	0x8001134E0301183F	4669
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_0	0x8000003A0301183F	3397
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_1	0x8000043A0301183F	3518
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_2	0x8000083A0301183F	3639
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_3	0x80000C3A0301183F	3760
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_4	0x8000103A0301183F	3881
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_0	0x8001003A0301183F	4099
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_1	0x8001043A0301183F	4220
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_2	0x8001083A0301183F	4341
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_3	0x80010C3A0301183F	4462
DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_4	0x8001103A0301183F	4583
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_0	0x8000013A0301183F	3429
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_1	0x8000053A0301183F	3549
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_2	0x8000093A0301183F	3670
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_3	0x80000D3A0301183F	3791
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_4	0x8000113A0301183F	3912
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_0	0x8001013A0301183F	4130
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_1	0x8001053A0301183F	4251
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_2	0x8001093A0301183F	4372
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_3	0x80010D3A0301183F	4493
DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_4	0x8001113A0301183F	4614
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_0	0x8000023A0301183F	3453
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_1	0x8000063A0301183F	3574
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_2	0x80000A3A0301183F	3695
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_3	0x80000E3A0301183F	3816
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_4	0x8000123A0301183F	3937
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_0	0x8001023A0301183F	4155
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_1	0x8001063A0301183F	4276
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_2	0x80010A3A0301183F	4397
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_3	0x80010E3A0301183F	4518
DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_4	0x8001123A0301183F	4639
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_0	0x8000033A0301183F	3478
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_1	0x8000073A0301183F	3599
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_2	0x80000B3A0301183F	3720
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_3	0x80000F3A0301183F	3841
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_4	0x8000133A0301183F	3962
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_0	0x8001033A0301183F	4180
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_1	0x8001073A0301183F	4301
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_2	0x80010B3A0301183F	4422
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_3	0x80010F3A0301183F	4543
DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_4	0x8001133A0301183F	4664
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_0	0x8000003B0301183F	3398
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_1	0x8000043B0301183F	3518
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_2	0x8000083B0301183F	3639
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_3	0x80000C3B0301183F	3760
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_4	0x8000103B0301183F	3881
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_0	0x8001003B0301183F	4099

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DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_1	0x8001043B0301183F	4220
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_2	0x8001083B0301183F	4341
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_3	0x80010C3B0301183F	4462
DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_4	0x8001103B0301183F	4583
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_0	0x8000013B0301183F	3429
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_1	0x8000053B0301183F	3550
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_2	0x8000093B0301183F	3671
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_3	0x80000D3B0301183F	3792
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_4	0x8000113B0301183F	3913
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_0	0x8001013B0301183F	4131
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_1	0x8001053B0301183F	4252
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_2	0x8001093B0301183F	4373
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_3	0x80010D3B0301183F	4494
DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_4	0x8001113B0301183F	4615
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_0	0x8000023B0301183F	3453
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_1	0x8000063B0301183F	3574
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_2	0x80000A3B0301183F	3695
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_3	0x80000E3B0301183F	3816
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_4	0x8000123B0301183F	3937
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_0	0x8001023B0301183F	4155
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_1	0x8001063B0301183F	4276
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_2	0x80010A3B0301183F	4397
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_3	0x80010E3B0301183F	4518
DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_4	0x8001123B0301183F	4639
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_0	0x8000033B0301183F	3478
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_1	0x8000073B0301183F	3599
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_2	0x80000B3B0301183F	3720
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_3	0x80000F3B0301183F	3841
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_4	0x8000133B0301183F	3962
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_0	0x8001033B0301183F	4180
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_1	0x8001073B0301183F	4301
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_2	0x80010B3B0301183F	4422
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_3	0x80010F3B0301183F	4543
DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_4	0x8001133B0301183F	4664
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_0	0x8000003C0301183F	3398
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_1	0x8000043C0301183F	3519
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_2	0x8000083C0301183F	3640
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_3	0x80000C3C0301183F	3761
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_4	0x8000103C0301183F	3882
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_0	0x8001003C0301183F	4100
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_1	0x8001043C0301183F	4221
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_2	0x8001083C0301183F	4342
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_3	0x80010C3C0301183F	4463
DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_4	0x8001103C0301183F	4584
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_0	0x8000013C0301183F	3429
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_1	0x8000053C0301183F	3550
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_2	0x8000093C0301183F	3671
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_3	0x80000D3C0301183F	3792
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_4	0x8000113C0301183F	3913
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_0	0x8001013C0301183F	4131
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_1	0x8001053C0301183F	4252

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DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_2	0x8001093C0301183F	4373
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_3	0x80010D3C0301183F	4494
DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_4	0x8001113C0301183F	4615
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_0	0x8000023C0301183F	3454
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_1	0x8000063C0301183F	3575
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_2	0x80000A3C0301183F	3696
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_3	0x80000E3C0301183F	3817
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_4	0x8000123C0301183F	3938
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_0	0x8001023C0301183F	4156
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_1	0x8001063C0301183F	4277
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_2	0x80010A3C0301183F	4398
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_3	0x80010E3C0301183F	4519
DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_4	0x8001123C0301183F	4640
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_0	0x8000033C0301183F	3478
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_1	0x8000073C0301183F	3599
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_2	0x80000B3C0301183F	3720
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_3	0x80000F3C0301183F	3841
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_4	0x8000133C0301183F	3962
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_0	0x8001033C0301183F	4180
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_1	0x8001073C0301183F	4301
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_2	0x80010B3C0301183F	4422
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_3	0x80010F3C0301183F	4543
DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_4	0x8001133C0301183F	4664
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_0	0x8000003D0301183F	3398
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_1	0x8000043D0301183F	3519
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_2	0x8000083D0301183F	3640
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_3	0x80000C3D0301183F	3761
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_4	0x8000103D0301183F	3882
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_0	0x8001003D0301183F	4100
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_1	0x8001043D0301183F	4221
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_2	0x8001083D0301183F	4342
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_3	0x80010C3D0301183F	4463
DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_4	0x8001103D0301183F	4584
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_0	0x8000013D0301183F	3430
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_1	0x8000053D0301183F	3550
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_2	0x8000093D0301183F	3671
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_3	0x80000D3D0301183F	3792
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_4	0x8000113D0301183F	3913
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_0	0x8001013D0301183F	4131
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_1	0x8001053D0301183F	4252
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_2	0x8001093D0301183F	4373
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_3	0x80010D3D0301183F	4494
DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_4	0x8001113D0301183F	4615
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_0	0x8000023D0301183F	3454
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_1	0x8000063D0301183F	3575
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_2	0x80000A3D0301183F	3696
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_3	0x80000E3D0301183F	3817
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_4	0x8000123D0301183F	3938
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_0	0x8001023D0301183F	4156
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_1	0x8001063D0301183F	4277
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_2	0x80010A3D0301183F	4398

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DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_3	0x80010E3D0301183F	4519
DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_4	0x8001123D0301183F	4640
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_0	0x8000033D0301183F	3479
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_1	0x8000073D0301183F	3600
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_2	0x80000B3D0301183F	3721
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_3	0x80000F3D0301183F	3842
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_4	0x8000133D0301183F	3963
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_0	0x8001033D0301183F	4181
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_1	0x8001073D0301183F	4302
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_2	0x80010B3D0301183F	4423
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_3	0x80010F3D0301183F	4544
DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_4	0x8001133D0301183F	4665
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_0	0x8000003E0301183F	3399
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_1	0x8000043E0301183F	3519
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_2	0x8000083E0301183F	3640
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_3	0x80000C3E0301183F	3761
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_4	0x8000103E0301183F	3882
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_0	0x8001003E0301183F	4100
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_1	0x8001043E0301183F	4221
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_2	0x8001083E0301183F	4342
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_3	0x80010C3E0301183F	4463
DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_4	0x8001103E0301183F	4584
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_0	0x8000013E0301183F	3430
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_1	0x8000053E0301183F	3551
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_2	0x8000093E0301183F	3672
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_3	0x80000D3E0301183F	3793
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_4	0x8000113E0301183F	3914
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_0	0x8001013E0301183F	4132
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_1	0x8001053E0301183F	4253
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_2	0x8001093E0301183F	4374
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_3	0x80010D3E0301183F	4495
DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_4	0x8001113E0301183F	4616
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_0	0x8000023E0301183F	3454
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_1	0x8000063E0301183F	3575
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_2	0x80000A3E0301183F	3696
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_3	0x80000E3E0301183F	3817
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_4	0x8000123E0301183F	3938
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_0	0x8001023E0301183F	4156
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_1	0x8001063E0301183F	4277
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_2	0x80010A3E0301183F	4398
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_3	0x80010E3E0301183F	4519
DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_4	0x8001123E0301183F	4640
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_0	0x8000033E0301183F	3479
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_1	0x8000073E0301183F	3600
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_2	0x80000B3E0301183F	3721
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_3	0x80000F3E0301183F	3842
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_4	0x8000133E0301183F	3963
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_0	0x8001033E0301183F	4181
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_1	0x8001073E0301183F	4302
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_2	0x80010B3E0301183F	4423
DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_3	0x80010F3E0301183F	4544

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DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_4	0x8001133E0301183F	4665
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_0	0x8000003F0301183F	3399
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_1	0x8000043F0301183F	3520
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_2	0x8000083F0301183F	3641
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_3	0x80000C3F0301183F	3762
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_4	0x8000103F0301183F	3883
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_0	0x8001003F0301183F	4101
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_1	0x8001043F0301183F	4222
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_2	0x8001083F0301183F	4343
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_3	0x80010C3F0301183F	4464
DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_4	0x8001103F0301183F	4585
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_0	0x8000013F0301183F	3430
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_1	0x8000053F0301183F	3551
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_2	0x8000093F0301183F	3672
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_3	0x80000D3F0301183F	3793
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_4	0x8000113F0301183F	3914
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_0	0x8001013F0301183F	4132
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_1	0x8001053F0301183F	4253
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_2	0x8001093F0301183F	4374
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_3	0x80010D3F0301183F	4495
DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_4	0x8001113F0301183F	4616
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_0	0x8000023F0301183F	3455
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_1	0x8000063F0301183F	3576
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_2	0x80000A3F0301183F	3697
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_3	0x80000E3F0301183F	3818
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_4	0x8000123F0301183F	3939
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_0	0x8001023F0301183F	4157
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_1	0x8001063F0301183F	4278
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_2	0x80010A3F0301183F	4399
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_3	0x80010E3F0301183F	4520
DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_4	0x8001123F0301183F	4641
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_0	0x8000033F0301183F	3479
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_1	0x8000073F0301183F	3600
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_2	0x80000B3F0301183F	3721
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_3	0x80000F3F0301183F	3842
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_4	0x8000133F0301183F	3963
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_0	0x8001033F0301183F	4181
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_1	0x8001073F0301183F	4302
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_2	0x80010B3F0301183F	4423
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_3	0x80010F3F0301183F	4544
DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_4	0x8001133F0301183F	4665
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_0	0x8000004003011830F	3399
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_1	0x8000044003011830F	3520
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_2	0x8000084003011830F	3641
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_3	0x80000C4003011830F	3762
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_4	0x8000104003011830F	3883
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_0	0x8001004003011830F	4101
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_1	0x8001044003011830F	4222
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_2	0x8001084003011830F	4343
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_3	0x80010C4003011830F	4464
DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_4	0x8001104003011830F	4585

Mnemonic	Address	Page
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_0	0x800001400301183F	3431
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_1	0x800005400301183F	3551
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_2	0x800009400301183F	3672
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_3	0x80000D400301183F	3793
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_4	0x800011400301183F	3914
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_0	0x800101400301183F	4132
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_1	0x800105400301183F	4253
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_2	0x800109400301183F	4374
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_3	0x80010D400301183F	4495
DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_4	0x800111400301183F	4616
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_0	0x800002400301183F	3455
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_1	0x800006400301183F	3576
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_2	0x80000A400301183F	3697
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_3	0x80000E400301183F	3818
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_4	0x800012400301183F	3939
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_0	0x800102400301183F	4157
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_1	0x800106400301183F	4278
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_2	0x80010A400301183F	4399
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_3	0x80010E400301183F	4520
DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_4	0x800112400301183F	4641
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_0	0x800003400301183F	3480
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_1	0x800007400301183F	3601
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_2	0x80000B400301183F	3722
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_3	0x80000F400301183F	3843
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_4	0x800013400301183F	3964
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_0	0x800103400301183F	4182
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_1	0x800107400301183F	4303
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_2	0x80010B400301183F	4424
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_3	0x80010F400301183F	4545
DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_4	0x800113400301183F	4666
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_0	0x800000410301183F	3400
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_1	0x800004410301183F	3520
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_2	0x800008410301183F	3641
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_3	0x80000C410301183F	3762
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_4	0x800010410301183F	3883
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_0	0x800100410301183F	4101
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_1	0x800104410301183F	4222
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_2	0x800108410301183F	4343
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_3	0x80010C410301183F	4464
DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_4	0x800110410301183F	4585
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_0	0x800001410301183F	3431
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_1	0x800005410301183F	3552
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_2	0x800009410301183F	3673
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_3	0x80000D410301183F	3794
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_4	0x800011410301183F	3915
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_0	0x800101410301183F	4133
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_1	0x800105410301183F	4254
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_2	0x800109410301183F	4375
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_3	0x80010D410301183F	4496
DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_4	0x800111410301183F	4617
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_0	0x800002410301183F	3455

Mnemonic	Address	Page
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_1	0x800006410301183F	3576
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_2	0x80000A410301183F	3697
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_3	0x80000E410301183F	3818
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_4	0x800012410301183F	3939
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_0	0x800102410301183F	4157
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_1	0x800106410301183F	4278
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_2	0x80010A410301183F	4399
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_3	0x80010E410301183F	4520
DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_4	0x800112410301183F	4641
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_0	0x800003410301183F	3480
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_1	0x800007410301183F	3601
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_2	0x80000B410301183F	3722
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_3	0x80000F410301183F	3843
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_4	0x800013410301183F	3964
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_0	0x800103410301183F	4182
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_1	0x800107410301183F	4303
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_2	0x80010B410301183F	4424
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_3	0x80010F410301183F	4545
DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_4	0x800113410301183F	4666
DPHY23.PHY23_DDRPHY_FIR_ACTION0_REG	0x800200960301183F	4780
DPHY23.PHY23_DDRPHY_FIR_ACTION1_REG	0x800200970301183F	4781
DPHY23.PHY23_DDRPHY_FIR_MASK_REG	0x800200930301183F	4779
DPHY23.PHY23_DDRPHY_FIR_REG	0x800200900301183F	4779
DPHY23.PHY23_DDRPHY_FIR_WOF_REG	0x800200980301183F	4781

The memory buffer registers are listed in the following tables.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_0
Address	800000000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P0_DP18_0_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_0
Address	800000010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_HW_VALUE:
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_0_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_0
Address	800000020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P0_DP18_0_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_0
Address	800000030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_0_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_0
Address	800000040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_0
Address	800000050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_0
Address	800000060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_0_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_0
Address	800000070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_0
Address	800000080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_0_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_0
Address	800000090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_0
Address	8000000A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_0_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_0_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_0
Address	8000000B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_0_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_0
Address	8000000C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_0
Address	8000000D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_0
Address	8000000E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P0_DP18_0_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_0
Address	8000000F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P0_DP18_0_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_0
Address	800000100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P0_DP18_0_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_0
Address	800000110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P0_DP18_0_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_0
Address	800000120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_0_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_0
Address	800000130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P0_0
Address	800000140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.

Bits	SCOM	Field Mnemonic: Description
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.

Bits	SCOM	Field Mnemonic: Description
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_0_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_0
Address	800000150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_0_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	*DP18 Write Leveling Status 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_0
Address	800000170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_0_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	*DP18 Write Centering Status 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_0
Address	800000180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_0_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_0
Address	800000190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P0_DP18_0_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_0
Address	8000001A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P0_DP18_0_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P0_0
Address	8000001B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_0_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	***DP18 Write Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_0
Address	8000001C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_0_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_0
Address	8000001D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_0_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_0_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B

Bits	SCOM	Field Mnemonic: Description
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_0_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_0
Address	800000300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_0
Address	800000310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_0
Address	800000320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD00_POS: MEMINTD00 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_0_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_0
Address	800000330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_0_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_0
Address	800000340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_0_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_0
Address	800000370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P0_DP18_0_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_0
Address	800000380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_0
Address	800000390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_0
Address	8000003A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP0*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_0
Address	8000003B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP0*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_0
Address	8000003C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP0*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_0
Address	8000003D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_0
Address	8000003E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_0
Address	8000003F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_0
Address	800000400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_0
Address	800000410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_0
Address	800000420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_0
Address	800000430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_0
Address	800000440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_0
Address	800000450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_0
Address	800000460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_0
Address	800000470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_0
Address	800000480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_0
Address	8000004A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_0
Address	8000004C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_0
Address	8000004E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_0
Address	800000500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_0
Address	800000510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_0
Address	800000520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_0
Address	800000530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_0
Address	800000540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_0
Address	800000550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_0
Address	800000560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_0
Address	800000570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_0
Address	8000005C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_0
Address	8000005D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_0
Address	800000600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_0
Address	800000610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_0
Address	800000620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_0
Address	800000630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_0
Address	800000640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_0
Address	800000650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_0
Address	800000660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_0
Address	800000670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_0
Address	800000680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_0
Address	800000690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_0
Address	8000006A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_0
Address	8000006B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_0
Address	8000006D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_0_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_0_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	*DP18 Delay Line Power Control*
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0
Address	8000006F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_0_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	*DP18 Read Timing Reference 0*
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_0
Address	800000700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_0_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_0_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read Timing Reference 1*
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_0
Address	800000710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_0_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_0_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_0
Address	800000720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P0_DP18_0_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.
56:63	RO	constant=0b00000000

Register Name	***DP18 SysClk Phase Rotator Value***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_0
Address	800000730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_0_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	***DP18 WrClk Phase Rotator Offset Value***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P0_0
Address	800000740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P0_DP18_0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	***DP18 IO TX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_0
Address	800000750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_0_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_0_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_0_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_0
Address	800000760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_0
Address	800000770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100

Bits	SCOM	Field Mnemonic: Description
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_0_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_0
Address	800000780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_0_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_0_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.

Bits	SCOM	Field Mnemonic: Description
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_0
Address	800000790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_0_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_0_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_0
Address	8000007A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_0_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_0_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_0
Address	8000007B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_0_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_0_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_0
Address	8000007C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_0
Address	8000007D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_0
Address	8000007E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_0
Address	800001040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_0
Address	800001050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_0
Address	800001090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_0
Address	8000010C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_0
Address	8000010D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_0
Address	800001130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_0
Address	800001300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_0
Address	800001310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_0
Address	800001380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_0
Address	800001390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_0
Address	8000013A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_0
Address	8000013B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_0
Address	8000013C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_0
Address	8000013D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_0
Address	8000013E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_0
Address	8000013F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_0
Address	800001400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_0
Address	800001410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_0
Address	800001420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_0
Address	800001430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_0
Address	800001440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_0
Address	800001450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_0
Address	800001460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_0
Address	800001470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_0
Address	800001480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_0
Address	8000014A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_0
Address	8000014C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_0
Address	8000014E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_0
Address	800001500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_0
Address	800001510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_0
Address	800001520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_0
Address	800001530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_0
Address	800001540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_0
Address	800001550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_0
Address	800001560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_0
Address	800001570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_0
Address	8000015C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_0
Address	8000015D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_0
Address	800001600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_0
Address	800001610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_0
Address	800001620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_0
Address	800001630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_0
Address	800001640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_0
Address	800001650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_0
Address	800001660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_0
Address	800001670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_0
Address	800001680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_0
Address	800001690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_0
Address	8000016A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_0
Address	8000016B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_0
Address	8000017C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_0
Address	8000017D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_0
Address	8000017E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_0
Address	800002040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_0
Address	800002050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_0
Address	800002090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_0
Address	8000020C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_0
Address	8000020D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_0
Address	800002130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_0
Address	800002300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_0
Address	800002310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_0
Address	800002380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_0
Address	800002390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_0
Address	8000023A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_0
Address	8000023B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_0
Address	8000023C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_0
Address	8000023D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_0
Address	8000023E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_0
Address	8000023F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_0
Address	800002400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_0
Address	800002410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_0
Address	800002420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_0
Address	800002430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_0
Address	800002440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_0
Address	800002450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_0
Address	800002460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_0
Address	800002470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_0
Address	800002480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_0
Address	8000024A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_0
Address	8000024C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_0
Address	8000024E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_0
Address	800002500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_0
Address	800002510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_0
Address	800002520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_0
Address	800002530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_0
Address	800002540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_0
Address	800002550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_0
Address	800002560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_0
Address	800002570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_0
Address	8000025C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_0
Address	8000025D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_0
Address	800002600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_0
Address	800002610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_0
Address	800002620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_0
Address	800002630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_0
Address	800002640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_0
Address	800002650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_0
Address	800002660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_0
Address	800002670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_0
Address	800002680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_0
Address	800002690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_0
Address	8000026A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_0
Address	8000026B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_0
Address	8000027C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_0
Address	8000027D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_0
Address	8000027E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_0
Address	800003040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_0
Address	800003050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_0
Address	800003090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_0
Address	8000030C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_0
Address	8000030D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_0
Address	800003130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_0
Address	800003300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_0
Address	800003310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_0
Address	800003380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_0
Address	800003390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_0
Address	8000033A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_0
Address	8000033B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_0
Address	8000033C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_0
Address	8000033D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_0
Address	8000033E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_0
Address	8000033F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_0
Address	800003400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_0
Address	800003410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_0
Address	800003420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_0
Address	800003430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_0
Address	800003440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_0
Address	800003450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_0
Address	800003460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_0
Address	800003470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_0
Address	800003480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_0
Address	8000034A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_0
Address	8000034C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_0
Address	8000034E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_0
Address	800003500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_0
Address	800003510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_0
Address	800003520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_0
Address	800003530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_0
Address	800003540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_0
Address	800003550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_0
Address	800003560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_0
Address	800003570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_0
Address	8000035C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_0
Address	8000035D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_0
Address	800003600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_0
Address	800003610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_0
Address	800003620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_0
Address	800003630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_0
Address	800003640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_0
Address	800003650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_0
Address	800003660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_0
Address	800003670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_0
Address	800003680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_0
Address	800003690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_0
Address	8000036A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_0
Address	8000036B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_0
Address	8000037C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P0_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Disable 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_0
Address	8000037D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P0_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	*DP18 Write DQ Offset Value RP3*
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_0
Address	8000037E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_1
Address	800004000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P0_DP18_1_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_1
Address	800004010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P0_DP18_1_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_1
Address	800004020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P0_DP18_1_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_1
Address	800004030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P0_DP18_1_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_1
Address	800004040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_1
Address	800004050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_1
Address	800004060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P0_DP18_1_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_1
Address	800004070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P0_DP18_1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_1
Address	800004080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P0_DP18_1_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_1
Address	800004090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_1
Address	8000040A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_1_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P0_DP18_1_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_1
Address	8000040B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P0_DP18_1_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_1
Address	8000040C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_1
Address	8000040D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_1
Address	8000040E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P0_DP18_1_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_1
Address	8000040F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P0_DP18_1_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_1
Address	800004100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P0_DP18_1_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_1
Address	800004110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P0_DP18_1_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_1
Address	800004120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_1_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_1
Address	800004130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P0_1
Address	800004140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P0_DP18_1_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_1
Address	800004150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P0_DP18_1_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_1
Address	800004170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P0_DP18_1_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_1
Address	800004180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P0_DP18_1_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_1
Address	800004190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P0_DP18_1_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_1
Address	8000041A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P0_DP18_1_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P0_1
Address	8000041B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P0_DP18_1_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_1
Address	8000041C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P0_DP18_1_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_1
Address	8000041D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_1_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_1_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P0_DP18_1_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_1
Address	800004300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_1
Address	800004310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_1
Address	800004320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P0_DP18_1_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_1
Address	800004330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P0_DP18_1_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_1
Address	800004340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P0_DP18_1_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_1
Address	800004370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P0_DP18_1_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_1
Address	800004380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_1
Address	800004390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_1
Address	8000043A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_1
Address	8000043B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_1
Address	8000043C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_1
Address	8000043D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_1
Address	8000043E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_1
Address	8000043F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_1
Address	800004400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_1
Address	800004410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_1
Address	800004420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_1
Address	800004430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_1
Address	800004440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_1
Address	800004450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_1
Address	800004460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_1
Address	800004470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_1
Address	800004480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_1
Address	8000044A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_1
Address	8000044C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_1
Address	8000044E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_1
Address	800004500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_1
Address	800004510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_1
Address	800004520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_1
Address	800004530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_1
Address	800004540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_1
Address	800004550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_1
Address	800004560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 7 RP0*
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_1
Address	800004570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P0_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP0*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_1
Address	8000045C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP0*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_1
Address	8000045D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_1
Address	800004600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_1
Address	800004610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_1
Address	800004620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_1
Address	800004630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_1
Address	800004640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_1
Address	800004650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_1
Address	800004660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_1
Address	800004670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_1
Address	800004680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_1
Address	800004690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_1
Address	8000046A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_1
Address	8000046B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_1
Address	8000046D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_1_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_1_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1
Address	8000046F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_1_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_1
Address	800004700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_1_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P0_DP18_1_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_1
Address	800004710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_1_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P0_DP18_1_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_1
Address	800004720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P0_DP18_1_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_1
Address	800004730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_1_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P0_DP18_1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P0_1
Address	800004740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P0_DP18_1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_1
Address	800004750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_1_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_1_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P0_DP18_1_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_1
Address	800004760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P0_DP18_1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_1
Address	800004770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P0_DP18_1_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_1
Address	800004780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_1_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P0_DP18_1_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_1
Address	800004790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_1_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P0_DP18_1_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_1
Address	8000047A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_1_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P0_DP18_1_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_1
Address	8000047B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_1_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P0_DP18_1_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_1
Address	8000047C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_1
Address	8000047D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_1
Address	8000047E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_1
Address	800005040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	*DP18 Write Clock Enable & Selection RP1*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_1
Address	800005050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_1
Address	800005090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_1
Address	8000050C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_1
Address	8000050D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_1
Address	800005130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_1
Address	800005300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_1
Address	800005310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_1
Address	800005380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_1
Address	800005390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_1
Address	8000053A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_1
Address	8000053B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_1
Address	8000053C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_1
Address	8000053D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_1
Address	8000053E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_1
Address	8000053F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_1
Address	800005400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_1
Address	800005410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_1
Address	800005420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_1
Address	800005430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_1
Address	800005440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_1
Address	800005450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_1
Address	800005460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_1
Address	800005470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_1
Address	800005480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_1
Address	8000054A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_1
Address	8000054C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_1
Address	8000054E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_1
Address	800005500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_1
Address	800005510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_1
Address	800005520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_1
Address	800005530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_1
Address	800005540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_1
Address	800005550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_1
Address	800005560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_1
Address	800005570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P0_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_1
Address	8000055C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_1
Address	8000055D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_1
Address	800005600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_1
Address	800005610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_1
Address	800005620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_1
Address	800005630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_1
Address	800005640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_1
Address	800005650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_1
Address	800005660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_1
Address	800005670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_1
Address	800005680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_1
Address	800005690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_1
Address	8000056A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_1
Address	8000056B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_1
Address	8000057C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_1
Address	8000057D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_1
Address	8000057E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_1
Address	800006040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_1
Address	800006050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_1
Address	800006090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_1
Address	8000060C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_1
Address	8000060D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_1
Address	800006130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_1
Address	800006300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_1
Address	800006310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_1
Address	800006380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_1
Address	800006390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_1
Address	8000063A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_1
Address	8000063B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_1
Address	8000063C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_1
Address	8000063D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_1
Address	8000063E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_1
Address	8000063F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_1
Address	800006400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_1
Address	800006410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_1
Address	800006420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_1
Address	800006430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_1
Address	800006440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_1
Address	800006450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_1
Address	800006460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_1
Address	800006470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_1
Address	800006480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_1
Address	8000064A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_1
Address	8000064C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_1
Address	8000064E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_1
Address	800006500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_1
Address	800006510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_1
Address	800006520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_1
Address	800006530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_1
Address	800006540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_1
Address	800006550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_1
Address	800006560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_1
Address	800006570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P0_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_1
Address	8000065C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_1
Address	8000065D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_1
Address	800006600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_1
Address	800006610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_1
Address	800006620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_1
Address	800006630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_1
Address	800006640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_1
Address	800006650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_1
Address	800006660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_1
Address	800006670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_1
Address	800006680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_1
Address	800006690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_1
Address	8000066A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_1
Address	8000066B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_1
Address	8000067C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_1
Address	8000067D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_1
Address	8000067E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_1
Address	800007040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_1
Address	800007050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P0_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_1
Address	800007090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_1
Address	8000070C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_1
Address	8000070D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_1
Address	800007130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P0_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_1
Address	800007300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_1
Address	800007310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P0_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_1
Address	800007380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_1
Address	800007390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_1
Address	8000073A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_1
Address	8000073B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_1
Address	8000073C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_1
Address	8000073D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_1
Address	8000073E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_1
Address	8000073F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_1
Address	800007400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_1
Address	800007410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_1
Address	800007420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_1
Address	800007430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_1
Address	800007440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_1
Address	800007450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_1
Address	800007460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_1
Address	800007470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_1
Address	800007480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_1
Address	8000074A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_1
Address	8000074C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_1
Address	8000074E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_1
Address	800007500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_1
Address	800007510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_1
Address	800007520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_1
Address	800007530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_1
Address	800007540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_1
Address	800007550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_1
Address	800007560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_1
Address	800007570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P0_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_1
Address	8000075C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_1
Address	8000075D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_1
Address	800007600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_1
Address	800007610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_1
Address	800007620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_1
Address	800007630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_1
Address	800007640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_1
Address	800007650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_1
Address	800007660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_1
Address	800007670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_1
Address	800007680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_1
Address	800007690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_1
Address	8000076A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_1
Address	8000076B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_1
Address	8000077C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P0_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Disable 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_1
Address	8000077D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P0_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	*DP18 Write DQ Offset Value RP3*
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_1
Address	8000077E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P0_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	*DP18 Data Bit Enable 0*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_2
Address	800008000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P0_DP18_2_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Enable 1*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_2
Address	800008010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_2_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_2
Address	800008020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P0_DP18_2_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_2
Address	800008030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_2_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_2
Address	800008040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_2
Address	800008050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_2
Address	800008060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_2_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_2
Address	800008070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_2_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_2
Address	800008080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_2_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_2
Address	800008090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_2
Address	8000080A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_2_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_2_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_2
Address	8000080B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_2_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_2
Address	8000080C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_2
Address	8000080D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_2
Address	8000080E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P0_DP18_2_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_2
Address	8000080F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P0_DP18_2_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_2
Address	800008100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P0_DP18_2_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_2
Address	800008110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P0_DP18_2_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_2
Address	800008120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_2_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_2
Address	800008130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P0_2
Address	800008140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_2_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_2
Address	800008150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_2_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_2
Address	800008170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_2_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_2
Address	800008180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_2_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_2
Address	800008190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P0_DP18_2_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_2
Address	8000081A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P0_DP18_2_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P0_2
Address	8000081B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_2_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_2
Address	8000081C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_2_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_2
Address	8000081D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_2_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_2_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_2_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_2
Address	800008300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_2
Address	800008310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_2
Address	800008320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_2_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_2
Address	800008330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_2_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_2
Address	800008340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_2_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_2
Address	800008370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P0_DP18_2_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_2
Address	800008380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_2
Address	800008390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_2
Address	8000083A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_2
Address	8000083B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_2
Address	8000083C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_2
Address	8000083D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_2
Address	8000083E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_2
Address	8000083F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_2
Address	800008400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_2
Address	800008410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_2
Address	800008420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_2
Address	800008430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_2
Address	800008440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_2
Address	800008450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_2
Address	800008460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_2
Address	800008470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_2
Address	800008480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_2
Address	8000084A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_2
Address	8000084C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_2
Address	8000084E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_2
Address	800008500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_2
Address	800008510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_2
Address	800008520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_2
Address	800008530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_2
Address	800008540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_2
Address	800008550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_2
Address	800008560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_2
Address	800008570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_2
Address	8000085C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_2
Address	8000085D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_2
Address	800008600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_2
Address	800008610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_2
Address	800008620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_2
Address	800008630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_2
Address	800008640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_2
Address	800008650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_2
Address	800008660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_2
Address	800008670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_2
Address	800008680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_2
Address	800008690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_2
Address	8000086A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_2
Address	8000086B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_2
Address	8000086D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_2_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_2_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2
Address	8000086F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_2_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_2
Address	800008700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_2_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_2_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_2
Address	800008710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_2_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_2_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_2
Address	800008720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P0_DP18_2_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_2
Address	800008730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_2_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_2_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P0_2
Address	800008740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P0_DP18_2_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_2
Address	800008750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_2_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_2_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_2_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_2
Address	800008760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_2_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_2
Address	800008770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_2_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_2
Address	800008780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_2_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_2_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_2
Address	800008790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_2_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_2_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_2
Address	8000087A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_2_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_2_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_2
Address	8000087B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_2_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_2_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_2
Address	8000087C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_2
Address	8000087D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_2
Address	8000087E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_2
Address	800009040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_2
Address	800009050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_2
Address	800090903011 83F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_2
Address	8000090C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_2
Address	8000090D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_2
Address	800009130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_2
Address	800009300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_2
Address	800009310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_2
Address	800009380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_2
Address	800009390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_2
Address	8000093A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_2
Address	8000093B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_2
Address	8000093C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_2
Address	8000093D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_2
Address	8000093E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_2
Address	8000093F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_2
Address	800009400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_2
Address	800009410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_2
Address	800009420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_2
Address	800009430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_2
Address	800009440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_2
Address	800009450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_2
Address	800009460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_2
Address	800009470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_2
Address	800009480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_2
Address	8000094A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_2
Address	8000094C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_2
Address	8000094E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_2
Address	800009500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_2
Address	800009510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_2
Address	800009520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_2
Address	800009530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_2
Address	800009540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_2
Address	800009550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_2
Address	800009560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_2
Address	800009570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_2
Address	8000095C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_2
Address	8000095D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_2
Address	800009600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_2
Address	800009610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_2
Address	800009620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_2
Address	800009630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_2
Address	800009640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_2
Address	800009650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_2
Address	800009660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_2
Address	800009670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_2
Address	800009680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_2
Address	800009690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_2
Address	8000096A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_2
Address	8000096B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_2
Address	8000097C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_2
Address	8000097D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_2
Address	8000097E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_2
Address	80000A040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_2
Address	80000A050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_2
Address	80000A090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_2
Address	80000A0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_2
Address	80000A0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_2
Address	80000A130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_2
Address	80000A300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_2
Address	80000A310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_2
Address	80000A380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_2
Address	80000A390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_2
Address	80000A3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_2
Address	80000A3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_2
Address	80000A3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_2
Address	80000A3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_2
Address	80000A3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_2
Address	80000A3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_2
Address	80000A400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_2
Address	80000A410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_2
Address	80000A420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_2
Address	80000A430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_2
Address	80000A440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_2
Address	80000A450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_2
Address	80000A460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_2
Address	80000A470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_2
Address	80000A480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_2
Address	80000A4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_2
Address	80000A4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_2
Address	80000A4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_2
Address	80000A500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_2
Address	80000A510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_2
Address	80000A520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_2
Address	80000A530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_2
Address	80000A540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_2
Address	80000A550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_2
Address	80000A560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_2
Address	80000A570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP2*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_2
Address	80000A5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP2*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_2
Address	80000A5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_2
Address	80000A600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_2
Address	80000A610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_2
Address	80000A620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_2
Address	80000A630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_2
Address	80000A640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_2
Address	80000A650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_2
Address	80000A660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_2
Address	80000A670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_2
Address	80000A680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_2
Address	80000A690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_2
Address	80000A6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_2
Address	80000A6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_2
Address	80000A7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_2
Address	80000A7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_2
Address	80000A7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_2
Address	80000B040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_2
Address	80000B050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_2
Address	80000B090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_2
Address	80000B0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_2
Address	80000B0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_2
Address	80000B130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_2
Address	80000B300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_2
Address	80000B310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_2
Address	80000B380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_2
Address	80000B390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_2
Address	80000B3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_2
Address	80000B3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_2
Address	80000B3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_2
Address	80000B3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_2
Address	80000B3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_2
Address	80000B3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_2
Address	80000B400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_2
Address	80000B410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_2
Address	80000B420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_2
Address	80000B430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_2
Address	80000B440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_2
Address	80000B450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_2
Address	80000B460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_2
Address	80000B470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_2
Address	80000B480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_2
Address	80000B4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_2
Address	80000B4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_2
Address	80000B4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_2
Address	80000B500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_2
Address	80000B510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_2
Address	80000B520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_2
Address	80000B530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_2
Address	80000B540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_2
Address	80000B550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_2
Address	80000B560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_2
Address	80000B570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_2
Address	80000B5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_2
Address	80000B5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_2
Address	80000B600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_2
Address	80000B610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_2
Address	80000B620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_2
Address	80000B630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_2
Address	80000B640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_2
Address	80000B650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_2
Address	80000B660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_2
Address	80000B670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_2
Address	80000B680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_2
Address	80000B690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_2
Address	80000B6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_2
Address	80000B6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_2
Address	80000B7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P0_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_2
Address	80000B7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P0_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_2
Address	80000B7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	*DP18 Data Bit Enable 0*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_3
Address	80000C000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P0_DP18_3_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Enable 1*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_3
Address	80000C010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P0_DP18_3_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_3
Address	80000C020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P0_DP18_3_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_3
Address	80000C030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P0_DP18_3_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_3
Address	80000C040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_3
Address	80000C050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_3
Address	80000C060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P0_DP18_3_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_3
Address	80000C070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P0_DP18_3_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_3
Address	80000C080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P0_DP18_3_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_3
Address	80000C090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_3
Address	80000C0A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_3_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P0_DP18_3_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_3
Address	80000C0B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P0_DP18_3_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_3
Address	80000C0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_3
Address	80000C0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_3
Address	80000C0E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P0_DP18_3_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_3
Address	80000C0F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P0_DP18_3_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_3
Address	80000C100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P0_DP18_3_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_3
Address	80000C110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P0_DP18_3_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_3
Address	80000C120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_3_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_3
Address	80000C130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P0_3
Address	80000C140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P0_DP18_3_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_3
Address	80000C150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P0_DP18_3_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_3
Address	80000C170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P0_DP18_3_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_3
Address	80000C180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P0_DP18_3_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_3
Address	80000C190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P0_DP18_3_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_3
Address	80000C1A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P0_DP18_3_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P0_3
Address	80000C1B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P0_DP18_3_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_3
Address	80000C1C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P0_DP18_3_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_3
Address	80000C1D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_3_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_3_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P0_DP18_3_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_3
Address	80000C300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_3
Address	80000C310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_3
Address	80000C320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P0_DP18_3_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_3
Address	80000C330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P0_DP18_3_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_3
Address	80000C340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P0_DP18_3_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_3
Address	80000C370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P0_DP18_3_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_3
Address	80000C380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_3
Address	80000C390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_3
Address	80000C3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_3
Address	80000C3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_3
Address	80000C3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_3
Address	80000C3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_3
Address	80000C3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_3
Address	80000C3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_3
Address	80000C400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_3
Address	80000C410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_3
Address	80000C420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_3
Address	80000C430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_3
Address	80000C440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_3
Address	80000C450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_3
Address	80000C460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_3
Address	80000C470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_3
Address	80000C480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_3
Address	80000C4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_3
Address	80000C4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_3
Address	80000C4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_3
Address	80000C500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_3
Address	80000C510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_3
Address	80000C520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_3
Address	80000C530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_3
Address	80000C540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_3
Address	80000C550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_3
Address	80000C560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Read Delay Value 7 RP0*
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_3
Address	80000C570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P0_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP0*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_3
Address	80000C5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP0*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_3
Address	80000C5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_3
Address	80000C600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_3
Address	80000C610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_3
Address	80000C620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_3
Address	80000C630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_3
Address	80000C640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_3
Address	80000C650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_3
Address	80000C660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_3
Address	80000C670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_3
Address	80000C680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_3
Address	80000C690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_3
Address	80000C6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_3
Address	80000C6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_3
Address	80000C6D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_3_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_3_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3
Address	80000C6F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_3_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_3
Address	80000C700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_3_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P0_DP18_3_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_3
Address	80000C710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_3_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P0_DP18_3_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_3
Address	80000C720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P0_DP18_3_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_3
Address	80000C730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_3_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P0_DP18_3_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P0_3
Address	80000C740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P0_DP18_3_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_3
Address	80000C750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_3_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_3_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P0_DP18_3_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_3
Address	80000C760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P0_DP18_3_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_3
Address	80000C770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P0_DP18_3_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_3
Address	80000C780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_3_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P0_DP18_3_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_3
Address	80000C790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_3_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P0_DP18_3_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_3
Address	80000C7A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_3_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P0_DP18_3_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_3
Address	80000C7B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_3_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P0_DP18_3_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_3
Address	80000C7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_3
Address	80000C7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_3
Address	80000C7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_3
Address	80000D040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_3
Address	80000D050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_3
Address	80000D090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_3
Address	80000D0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_3
Address	80000D0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_3
Address	80000D130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_3
Address	80000D300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_3
Address	80000D310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_3
Address	80000D380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_3
Address	80000D390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_3
Address	80000D3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_3
Address	80000D3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_3
Address	80000D3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_3
Address	80000D3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_3
Address	80000D3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_3
Address	80000D3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_3
Address	80000D400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_3
Address	80000D410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_3
Address	80000D420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_3
Address	80000D430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_3
Address	80000D440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_3
Address	80000D450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_3
Address	80000D460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_3
Address	80000D470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_3
Address	80000D480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_3
Address	80000D4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_3
Address	80000D4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_3
Address	80000D4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_3
Address	80000D500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_3
Address	80000D510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_3
Address	80000D520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_3
Address	80000D530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_3
Address	80000D540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_3
Address	80000D550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_3
Address	80000D560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_3
Address	80000D570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P0_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_3
Address	80000D5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_3
Address	80000D5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_3
Address	80000D600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_3
Address	80000D610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_3
Address	80000D620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_3
Address	80000D630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_3
Address	80000D640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_3
Address	80000D650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_3
Address	80000D660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_3
Address	80000D670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_3
Address	80000D680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_3
Address	80000D690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_3
Address	80000D6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_3
Address	80000D6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_3
Address	80000D7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_3
Address	80000D7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_3
Address	80000D7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_3
Address	80000E040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_3
Address	80000E050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_3
Address	80000E090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_3
Address	80000E0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_3
Address	80000E0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_3
Address	80000E130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_3
Address	80000E300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_3
Address	80000E310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_3
Address	80000E380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_3
Address	80000E390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_3
Address	80000E3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_3
Address	80000E3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_3
Address	80000E3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_3
Address	80000E3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_3
Address	80000E3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_3
Address	80000E3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_3
Address	80000E400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_3
Address	80000E410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_3
Address	80000E420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_3
Address	80000E430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_3
Address	80000E440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_3
Address	80000E450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_3
Address	80000E460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_3
Address	80000E470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_3
Address	80000E480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_3
Address	80000E4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_3
Address	80000E4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_3
Address	80000E4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_3
Address	80000E500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_3
Address	80000E510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_3
Address	80000E520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_3
Address	80000E530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_3
Address	80000E540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_3
Address	80000E550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_3
Address	80000E560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_3
Address	80000E570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P0_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_3
Address	80000E5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_3
Address	80000E5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_3
Address	80000E600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_3
Address	80000E610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_3
Address	80000E620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_3
Address	80000E630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_3
Address	80000E640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_3
Address	80000E650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_3
Address	80000E660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_3
Address	80000E670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_3
Address	80000E680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_3
Address	80000E690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_3
Address	80000E6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_3
Address	80000E6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_3
Address	80000E7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_3
Address	80000E7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_3
Address	80000E7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_3
Address	80000F040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_3
Address	80000F050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P0_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_3
Address	80000F090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_3
Address	80000F0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_3
Address	80000F0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_3
Address	80000F130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P0_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_3
Address	80000F300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_3
Address	80000F310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P0_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_3
Address	80000F380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_3
Address	80000F390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_3
Address	80000F3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_3
Address	80000F3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_3
Address	80000F3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_3
Address	80000F3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_3
Address	80000F3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_3
Address	80000F3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_3
Address	80000F400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_3
Address	80000F410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_3
Address	80000F420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_3
Address	80000F430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_3
Address	80000F440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_3
Address	80000F450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_3
Address	80000F460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_3
Address	80000F470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_3
Address	80000F480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_3
Address	80000F4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_3
Address	80000F4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_3
Address	80000F4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_3
Address	80000F500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_3
Address	80000F510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_3
Address	80000F520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_3
Address	80000F530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_3
Address	80000F540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_3
Address	80000F550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_3
Address	80000F560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_3
Address	80000F570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P0_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_3
Address	80000F5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_3
Address	80000F5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_3
Address	80000F600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_3
Address	80000F610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_3
Address	80000F620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_3
Address	80000F630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_3
Address	80000F640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_3
Address	80000F650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_3
Address	80000F660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_3
Address	80000F670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_3
Address	80000F680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_3
Address	80000F690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_3
Address	80000F6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_3
Address	80000F6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_3
Address	80000F7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P0_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_3
Address	80000F7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P0_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_3
Address	80000F7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P0_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	*DP18 Data Bit Enable 0*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P0_4
Address	800010000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE0_P0_DP18_4_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Enable 1*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P0_4
Address	800010010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P0_DP18_4_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P0_4
Address	800010020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DIR0_P0_DP18_4_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P0_4
Address	800010030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P0_DP18_4_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P0_4
Address	800010040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P0_4
Address	800010050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P0_4
Address	800010060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P0_DP18_4_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P0_4
Address	800010070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_4_SYSCLK_PR_P0_DP18_4_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P0_4
Address	800010080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P0_DP18_4_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_4
Address	800010090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P0_4
Address	8000100A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P0_DP18_4_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P0_DP18_4_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P0_4
Address	8000100B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_4_DEBUG_SEL_P0_DP18_4_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P0_4
Address	8000100C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P0_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P0_4
Address	8000100D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P0_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P0_4
Address	8000100E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS0_P0_DP18_4_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P0_4
Address	8000100F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS1_P0_DP18_4_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P0_4
Address	800010100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS2_P0_DP18_4_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P0_4
Address	800010110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS3_P0_DP18_4_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P0_4
Address	800010120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P0_DP18_4_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P0_4
Address	800010130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P0_4
Address	800010140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_4_RD_STATUS0_P0_DP18_4_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P0_4
Address	800010150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P0_DP18_4_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P0_4
Address	800010170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P0_DP18_4_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P0_4
Address	800010180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P0_DP18_4_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P0_4
Address	800010190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS1_P0_DP18_4_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P0_4
Address	8000101A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS2_P0_DP18_4_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P0_4
Address	8000101B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P0_DP18_4_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P0_4
Address	8000101C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P0_DP18_4_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P0_4
Address	8000101D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P0_DP18_4_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P0_DP18_4_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P0_DP18_4_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P0_4
Address	800010300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P0_4
Address	800010310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P0_4
Address	800010320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_0_P0_DP18_4_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P0_4
Address	800010330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_1_P0_DP18_4_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P0_4
Address	800010340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_2_P0_DP18_4_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P0_4
Address	800010370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_OFFSET_P0_DP18_4_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P0_4
Address	800010380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P0_4
Address	800010390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P0_4
Address	8000103A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P0_4
Address	8000103B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P0_4
Address	8000103C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P0_4
Address	8000103D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P0_4
Address	8000103E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P0_4
Address	8000103F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P0_4
Address	800010400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P0_4
Address	800010410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P0_4
Address	800010420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P0_4
Address	800010430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P0_4
Address	800010440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P0_4
Address	800010450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P0_4
Address	800010460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P0_4
Address	800010470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P0_4
Address	800010480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P0_4
Address	8000104A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P0_4
Address	8000104C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P0_4
Address	8000104E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP0_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P0_4
Address	800010500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P0_4
Address	800010510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P0_4
Address	800010520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P0_4
Address	800010530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P0_4
Address	800010540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P0_4
Address	800010550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P0_4
Address	800010560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P0_4
Address	800010570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P0_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P0_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_4
Address	8000105C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_4
Address	8000105D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P0_4
Address	800010600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P0_4
Address	800010610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P0_4
Address	800010620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P0_4
Address	800010630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P0_4
Address	800010640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P0_4
Address	800010650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P0_4
Address	800010660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P0_4
Address	800010670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P0_4
Address	800010680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P0_4
Address	800010690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P0_4
Address	8000106A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P0_4
Address	8000106B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P0_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P0_4
Address	8000106D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_4_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P0_DP18_4_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4
Address	8000106F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P0_4_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P0_4
Address	800010700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P0_DP18_4_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P0_DP18_4_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P0_4
Address	800010710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P0_DP18_4_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P0_DP18_4_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P0_4
Address	800010720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DQS_TIMING_REFERENCE_P0_DP18_4_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P0_4
Address	800010730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P0_DP18_4_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P0_DP18_4_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P0_4
Address	800010740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_WRCLK_PR_P0_DP18_4_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P0_4
Address	800010750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P0_DP18_4_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P0_DP18_4_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P0_DP18_4_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P0_4
Address	800010760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_4_PLL_CONFIG0_P0_DP18_4_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P0_4
Address	800010770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_4_PLL_CONFIG1_P0_DP18_4_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P0_4
Address	800010780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P0_DP18_4_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P0_DP18_4_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P0_4
Address	800010790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P0_DP18_4_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P0_DP18_4_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P0_4
Address	8000107A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P0_DP18_4_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P0_DP18_4_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P0_4
Address	8000107B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P0_DP18_4_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P0_DP18_4_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P0_4
Address	8000107C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP0_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P0_4
Address	8000107D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP0_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P0_4
Address	8000107E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P0_4
Address	800011040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P0_4
Address	800011050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_4
Address	800011090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P0_4
Address	8000110C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P0_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P0_4
Address	8000110D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P0_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P0_4
Address	800011130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P0_4
Address	800011300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P0_4
Address	800011310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P0_4
Address	800011380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P0_4
Address	800011390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P0_4
Address	8000113A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P0_4
Address	8000113B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P0_4
Address	8000113C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P0_4
Address	8000113D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P0_4
Address	8000113E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P0_4
Address	8000113F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P0_4
Address	800011400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P0_4
Address	800011410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P0_4
Address	800011420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P0_4
Address	800011430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P0_4
Address	800011440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P0_4
Address	800011450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P0_4
Address	800011460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P0_4
Address	800011470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P0_4
Address	800011480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P0_4
Address	8000114A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P0_4
Address	8000114C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P0_4
Address	8000114E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP1_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P0_4
Address	800011500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P0_4
Address	800011510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P0_4
Address	800011520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P0_4
Address	800011530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P0_4
Address	800011540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P0_4
Address	800011550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P0_4
Address	800011560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P0_4
Address	800011570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P0_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P0_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_4
Address	8000115C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_4
Address	8000115D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P0_4
Address	800011600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P0_4
Address	800011610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P0_4
Address	800011620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P0_4
Address	800011630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P0_4
Address	800011640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P0_4
Address	800011650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P0_4
Address	800011660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P0_4
Address	800011670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P0_4
Address	800011680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P0_4
Address	800011690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P0_4
Address	8000116A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P0_4
Address	8000116B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P0_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P0_4
Address	8000117C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP1_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P0_4
Address	8000117D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP1_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P0_4
Address	8000117E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P0_4
Address	800012040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P0_4
Address	800012050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_4
Address	800012090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P0_4
Address	8000120C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P0_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P0_4
Address	8000120D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P0_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P0_4
Address	800012130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P0_4
Address	800012300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P0_4
Address	800012310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P0_4
Address	800012380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P0_4
Address	800012390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P0_4
Address	8000123A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P0_4
Address	8000123B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P0_4
Address	8000123C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P0_4
Address	8000123D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P0_4
Address	8000123E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P0_4
Address	8000123F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P0_4
Address	800012400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P0_4
Address	800012410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P0_4
Address	800012420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P0_4
Address	800012430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P0_4
Address	800012440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P0_4
Address	800012450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P0_4
Address	800012460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P0_4
Address	800012470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P0_4
Address	800012480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P0_4
Address	8000124A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P0_4
Address	8000124C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P0_4
Address	8000124E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP2_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P0_4
Address	800012500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P0_4
Address	800012510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P0_4
Address	800012520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P0_4
Address	800012530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P0_4
Address	800012540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P0_4
Address	800012550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P0_4
Address	800012560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P0_4
Address	800012570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P0_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P0_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_4
Address	8000125C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_4
Address	8000125D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P0_4
Address	800012600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P0_4
Address	800012610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P0_4
Address	800012620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P0_4
Address	800012630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P0_4
Address	800012640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P0_4
Address	800012650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P0_4
Address	800012660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P0_4
Address	800012670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P0_4
Address	800012680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P0_4
Address	800012690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P0_4
Address	8000126A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P0_4
Address	8000126B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P0_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P0_4
Address	8000127C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP2_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P0_4
Address	8000127D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP2_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P0_4
Address	8000127E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P0_4
Address	800013040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P0_4
Address	800013050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P0_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_4
Address	800013090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P0_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P0_4
Address	8000130C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P0_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P0_4
Address	8000130D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P0_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P0_4
Address	800013130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P0_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P0_4
Address	800013300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P0_4
Address	800013310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P0_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P0_4
Address	800013380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P0_4
Address	800013390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P0_4
Address	8000133A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P0_4
Address	8000133B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P0_4
Address	8000133C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P0_4
Address	8000133D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P0_4
Address	8000133E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P0_4
Address	8000133F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P0_4
Address	800013400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P0_4
Address	800013410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P0_4
Address	800013420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P0_4
Address	800013430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P0_4
Address	800013440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P0_4
Address	800013450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P0_4
Address	800013460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P0_4
Address	800013470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P0_4
Address	800013480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P0_4
Address	8000134A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P0_4
Address	8000134C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P0_4
Address	8000134E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP3_REG_P0_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P0_4
Address	800013500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P0_4
Address	800013510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P0_4
Address	800013520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P0_4
Address	800013530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P0_4
Address	800013540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P0_4
Address	800013550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P0_4
Address	800013560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P0_4
Address	800013570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P0_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P0_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_4
Address	8000135C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_4
Address	8000135D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P0_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P0_4
Address	800013600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P0_4
Address	800013610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P0_4
Address	800013620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P0_4
Address	800013630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P0_4
Address	800013640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P0_4
Address	800013650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P0_4
Address	800013660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P0_4
Address	800013670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P0_4
Address	800013680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P0_4
Address	800013690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P0_4
Address	8000136A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P0_4
Address	8000136B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P0_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P0_4
Address	8000137C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP3_P0_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P0_4
Address	8000137D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP3_P0_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P0_4
Address	8000137E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P0_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR0
Address	800040000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR0_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR0_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR0
Address	800040010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR0_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P0_ADR0
Address	800040040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P0_ADR0_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P0_ADR0_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P0_ADR0
Address	800040050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P0_ADR0_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P0_ADR0_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P0_ADR0
Address	800040060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY2_P0_ADR0_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P0_ADR0_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P0_ADR0
Address	800040070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P0_ADR0_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P0_ADR0_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P0_ADR0
Address	800040080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P0_ADR0_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P0_ADR0_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P0_ADR0
Address	800040090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P0_ADR0_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P0_ADR0_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P0_ADR0
Address	8000400A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY6_P0_ADR0_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P0_ADR0_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P0_ADR0
Address	8000400B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY7_P0_ADR0_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P0_ADR0_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR0
Address	8000400C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR0_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR0
Address	8000401A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR0_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR0
Address	800040200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR0_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR0
Address	800040210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR0_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0
Address	8000402A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR0_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0
Address	8000402B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR0_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR0
Address	8000402C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR0_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR0_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR1
Address	800044000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR1_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P0_ADR1_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR1
Address	800044010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P0_ADR1_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P0_ADR1
Address	800044040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P0_ADR1_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P0_ADR1_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P0_ADR1
Address	800044050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P0_ADR1_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P0_ADR1_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P0_ADR1
Address	800044060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY2_P0_ADR1_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P0_ADR1_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P0_ADR1
Address	800044070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P0_ADR1_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P0_ADR1_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P0_ADR1
Address	800044080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P0_ADR1_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P0_ADR1_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P0_ADR1
Address	800044090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P0_ADR1_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P0_ADR1_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P0_ADR1
Address	8000440A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY6_P0_ADR1_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P0_ADR1_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P0_ADR1
Address	8000440B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY7_P0_ADR1_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P0_ADR1_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR1
Address	8000440C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P0_ADR1_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR1
Address	8000441A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P0_ADR1_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR1
Address	800044200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P0_ADR1_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR1
Address	800044210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P0_ADR1_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1
Address	8000442A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P0_ADR1_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1
Address	8000442B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P0_ADR1_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR1
Address	8000442C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR1_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P0_ADR1_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR2
Address	800048000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR2_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR2_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR2
Address	800048010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR2_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P0_ADR2
Address	800048040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P0_ADR2_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P0_ADR2_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P0_ADR2
Address	800048050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P0_ADR2_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P0_ADR2_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P0_ADR2
Address	800048060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY2_P0_ADR2_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P0_ADR2_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P0_ADR2
Address	800048070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P0_ADR2_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P0_ADR2_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P0_ADR2
Address	800048080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P0_ADR2_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P0_ADR2_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P0_ADR2
Address	800048090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P0_ADR2_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P0_ADR2_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P0_ADR2
Address	8000480A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY6_P0_ADR2_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P0_ADR2_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P0_ADR2
Address	8000480B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY7_P0_ADR2_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P0_ADR2_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR2
Address	8000480C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR2_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR2
Address	8000481A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR2_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR2
Address	800048200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR2_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR2
Address	800048210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR2_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2
Address	8000482A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR2_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2
Address	8000482B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR2_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR2
Address	8000482C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR2_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR2_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P0_ADR3
Address	80004C000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR3_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P0_ADR3_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P0_ADR3
Address	80004C010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P0_ADR3_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P0_ADR3
Address	80004C040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P0_ADR3_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P0_ADR3_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P0_ADR3
Address	80004C050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P0_ADR3_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P0_ADR3_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P0_ADR3
Address	80004C060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY2_P0_ADR3_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P0_ADR3_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P0_ADR3
Address	80004C070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P0_ADR3_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P0_ADR3_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P0_ADR3
Address	80004C080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P0_ADR3_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P0_ADR3_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P0_ADR3
Address	80004C090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P0_ADR3_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P0_ADR3_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P0_ADR3
Address	80004C0A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY6_P0_ADR3_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P0_ADR3_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 7***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P0_ADR3
Address	80004C0B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY7_P0_ADR3_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P0_ADR3_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR DFT Wrap Status And Control***
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P0_ADR3
Address	80004C0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P0_ADR3_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P0_ADR3
Address	80004C1A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P0_ADR3_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P0_ADR3
Address	80004C200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P0_ADR3_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P0_ADR3
Address	80004C210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P0_ADR3_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3
Address	80004C2A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P0_ADR3_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3
Address	80004C2B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P0_ADR3_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P0_ADR3
Address	80004C2C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR3_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P0_ADR3_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	*ADR PLL/VREG Configuration 0*
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S0
Address	800080300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	*ADR PLL/VREG Configuration 1*
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S0
Address	800080310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100

Bits	SCOM	Field Mnemonic: Description
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR0_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S0
Address	800080320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in are asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR0_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S0
Address	800080330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	*ADR SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S0
Address	800080340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field.
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR0_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	*ADR Output Driver Force And ATEST Control*
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S0
Address	800080350301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_FORCE_EN: Output Force Enable Bit.
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR0_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	*ADR Output Driver Force Value 0*
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S0
Address	800080360301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Output Driver Force Value 1*
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S0
Address	800080370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Slew Calibration Control***
Mnemonic	DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S0
Address	800080390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR0_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	***ADR PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR32S1
Address	800084300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P0_ADR1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***ADR PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR32S1
Address	800084310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P0_ADR1_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR32S1
Address	800084320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in are asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P0_ADR1_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR32S1
Address	800084330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P0_ADR1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	***ADR SysClk Phase Rotator Value***
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR32S1
Address	800084340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field.
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P0_ADR1_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	***ADR Output Driver Force And ATEST Control***
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR32S1
Address	800084350301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_FORCE_EN: Output Force Enable Bit.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P0_ADR1_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	***ADR Output Driver Force Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR32S1
Address	800084360301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P0_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Output Driver Force Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR32S1
Address	800084370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P0_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Slew Calibration Control*
Mnemonic	DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR32S1
Address	800084390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P0_ADR1_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	*PC DP18 PLL Lock Status*
Mnemonic	DPHY23.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P0
Address	8000C0000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:62	ROX	DDRPHY_PC_DP18_PLL_LOCK_STATUS_P0_DP18_PLL_LOCK: One bit for each DP18 in the DDR PHY Core. When the core contains less than 15 DP18s, then bits with an index value greater than NUM_DP18 - 1 are reserved. '0'b - PLL in the bit indexed DP18 is not locked. '1'b - PLL in the bit indexed DP18 is locked. When the PHY is configured in TDM Mode, this register reports the PLL Lock Status of all the DP18s in the PHY.
63	RO	constant=0b0

Register Name	*PC AD32S PLL Lock Status*
Mnemonic	DPHY23.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P0
Address	8000C0010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	ROX	DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P0_AD32S_PLL_LOCK: One bit for each ADR Support Block in the DDR PHY Core. When the core contains less than 2 AD32Ss, bits with an index value greater than NUM_AD32S-1 are reserved. '0'b - PLL in the bit indexed AD32S is not locked. '1'b - PLL in the bit indexed AD32S is locked.
50:63	RO	constant=0b00000000000000

Register Name	*PC Rank Pair 0*
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR0_P0
Address	8000C0020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_PRI: Primary Rank of Rank Pair 0 When configured for a protocol that only supports a single rank system, this field must be set to 0.
51	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_PRI_V: Value in the RANK_PAIR0_PRI field is valid
52:54	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_SEC: Secondary Rank of Rank Pair 0
55	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR0_SEC_V: Value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_PRI: Primary Rank of Rank Pair 1
59	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_PRI_V: Value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_SEC: Secondary Rank of Rank Pair 1
63	RW	DDRPHY_PC_RANK_PAIR0_P0_RANK_PAIR1_SEC_V: Value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	*PC Rank Pair 1*
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR1_P0
Address	8000C0030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_PRI: Primary Rank of Rank Pair 2
51	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_PRI_V: Value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the register defined in.
52:54	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_SEC: Secondary Rank of Rank Pair 2
55	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR2_SEC_V: Value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_PRI: Primary Rank of Rank Pair 3

Bits	SCOM	Field Mnemonic: Description
59	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_PRI_V: Value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_SEC: Secondary Rank of Rank Pair 3
63	RW	DDRPHY_PC_RANK_PAIR1_P0_RANK_PAIR3_SEC_V: Value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	*PC Periodic Base Counter 0*
Mnemonic	DPHY23.DDRPHY_PC_BASE_CNTR0_P0
Address	8000C0040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_BASE_CNTR0_P0_PERIODIC_BASE_CNTR0: Periodic Base Counter 0. When enabled via PERIODIC_CAL_REQ_EN counter is free running (counts every dphy_nclk clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & '0'} from the register described in.

Register Name	*PC Periodic Reload Value 0*
Mnemonic	DPHY23.DDRPHY_PC_RELOAD_VALUE0_P0
Address	8000C0050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RELOAD_VALUE0_P0_PERIODIC_CAL_REQ_EN: '1'b - Enable Periodic Calibration request generation from the PHY. '0'b - Disable Periodic Calibration request generation from the PHY.
49:63	RW	DDRPHY_PC_RELOAD_VALUE0_P0_PERIODIC_RELOAD_VALUE0: Periodic Reload Value 0. This value is loaded into bits 0 through 14 of the when it rolls over. Bit 15 is always loaded with '0'b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to '1'b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	*PC Periodic Base Counter 1*
Mnemonic	DPHY23.DDRPHY_PC_BASE_CNTR1_P0
Address	8000C0060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	DDRPHY_PC_BASE_CNTR1_P0_PERIODIC_BASE_CNTR1: Periodic Base Counter 1. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set it is reloaded with the value 'FFFF'h. This register enables the and the every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set it is reloaded with the value '00FF'h. When the FAST_SIM_PER_CNTR bit is set this register enables and the every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer*
Mnemonic	DPHY23.DDRPHY_PC_CAL_TIMER_P0
Address	8000C0070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_CAL_TIMER_P0_PERIODIC_CAL_TIMER: Periodic Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_TIMER_RELOAD_VALUE from the register described in. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer Reload Value*
Mnemonic	DPHY23.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0
Address	8000C0080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P0_PERIODIC_TIMER_RELOAD_VALUE: Periodic Reload Value 0. This value is loaded into the when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Impedance Calibration Timer*
Mnemonic	DPHY23.DDRPHY_PC_ZCAL_TIMER_P0
Address	8000C0090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	DDRPHY_PC_ZCAL_TIMER_P0_PERIODIC_ZCAL_TIMER: Periodic Impedance Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the register described in. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Impedance Calibration Timer Reload Value*
Mnemonic	DPHY23.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0
Address	8000C00A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P0_PERIODIC_TIMER_RELOAD_VALUE: Periodic Impedance Calibration Timer Reload Value. This value is loaded into the when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Calibration Configuration*
Mnemonic	DPHY23.DDRPHY_PC_PER_CAL_CONFIG_P0
Address	8000C00B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_ENA_RANK_PAIR: '1'b indicates periodic calibration is enabled '0'b indicates periodic calibration is disabled Bit 0 contains the enable bit for rank pair 0Bit 1 contains the enable bit for rank pair 1Bit 2 contains the enable bit for rank pair 2Bit 3 contains the enable bit for rank pair 3
52	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_ENA_ZCAL: Enables the periodic impedance calibration logic.
53	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SysClk with the Memory Controller Clock (dphy_nclkSysClk Alignment).
54	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ENA_PER_READ_CTR: '1'b - Enable the updating of the registers described in during periodic read centering. '0'b - Prevent the updating of the registers described in during periodic read centering.
55	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ENA_PER_RDCLK_ALIGN: '1'b - Enable the updating of the register described in at the conclusion of periodic read centering on a nibble of DQ lanes. '0'b - Prevent the updating of the register described in at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS Alignment).
57:58	RWX	DDRPHY_PC_PER_CAL_CONFIG_P0_PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.

Bits	SCOM	Field Mnemonic: Description
59	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_FAST_SIM_PER_CNTR: This bit must be '0'b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. '1'b causes the register described in to roll over to '00FF'h. '0'b has no effect on the behavior of the register described in.
60	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_START_INIT_CAL: When this bit is written to '1'b, the DDR PHY initiates an initial calibration for all ranks enabled in the register defined in. When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_START_PER_CAL: When this bit is written to '1'b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ABORT_ON_ERR_EN: Periodic Calibration Abort on Error Enable. '1'b - Enable the detection of the pc_errn_in. '0'b - Disable the detection of the pc_errn_in.
63	RW	DDRPHY_PC_PER_CAL_CONFIG_P0_ZCAL_UPDATE_MODE: Reserved. See PC Config 0 ZCAL_NOT_CONT bit.

Register Name	***PC Configuration 0***
Mnemonic	DPHY23.DDRPHY_PC_CONFIG0_P0
Address	8000C00C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG0_P0_PROTOCOL: Values: DDR3=>0b0000 DDR4=>0b0001 RLDRAM2_CIO=>0b0010
52	RW	DDRPHY_PC_CONFIG0_P0_DATA_MUX4_1MODE: Data Multiplexer Mode 4:1 Enable. '0'b - Data Multiplexer Mode is 2:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) is two times as wide as the data and control signals (pins) on the Memory Interface (MEMINT) Interface. '1'b - Data Multiplexer Mode is 4:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to one half of the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) are four times as wide as the data and control signals (pins) on the Memory Interface (MEMINT Interface).
53	RW	DDRPHY_PC_CONFIG0_P0_SPAM_EN: '1'b - The PC only snoops read and write commands for primary ranks of each rank pair (IE reads and writes to secondary ranks are ignored). '0'b - Split Access Mode is not enabled.
54	RW	DDRPHY_PC_CONFIG0_P0_DDR4_CMD_SIG_REDUCTION: Values: DDR3=>0b0 DDR4=>0b1
55	RW	DDRPHY_PC_CONFIG0_P0_SYSCLK_2X_MEMINTCLKO: Always write this bit to '0'b. This function is not supported. '0'b - The internal SysClk frequency equals the MEMINTCLKO (memory interface clock) frequency. '1'b - The internal SysClk frequency is 2* the MEMINTCLKO (memory interface clock) frequency. Support of this function requires this register to be written during the reset sequence when the PLL values are configured.
56	RW	DDRPHY_PC_CONFIG0_P0_RANK_OVERRIDE: Rank Override Mode '0'b - The DDR PHY uses the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface to determine the rank pair and hence the configuration registers for each read or write command. '1'b - The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all readwrite commands regardless of the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface. When this bit is '1'b, the following assumptions/restrictions apply:

Bits	SCOM	Field Mnemonic: Description
57:59	RW	DDRPHY_PC_CONFIG0_P0_RANK_OVERRIDE_VALUE: Rank Override Value
60	RW	DDRPHY_PC_CONFIG0_P0_LOW_LATENCY: '1'b - Force Early Read Start Mode (ERS Mode) off. '0'b - ERS Mode on/off determined by CL value. When CL = 5 or 6, ERS Mode is automatically off. Otherwise, ERS Mode is automatically on.
61	RW	
62	RW	DDRPHY_PC_CONFIG0_P0_DDR4_VLEVEL_BANK_GROUP: In DDR4: '1'b - enable Voltage Level and Bank Group Arch(DDR4 ballot 1716.23). '0'b - disable Voltage Level and Bank Group Arch. For all other protocols, this bit must be '0'b.
63	RW	DDRPHY_PC_CONFIG0_P0_ZCAL_NOT_CONT: '1'b - IO PVT values are only updated when an internal ZQ cal is requested. '0'b - IO PVT values are updated continuously.

Register Name	***PC Configuration 1***
Mnemonic	DPHY23.DDRPHY_PC_CONFIG1_P0
Address	8000C00D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG1_P0_WRITE_LATENCY_OFFSET: Write Latency Offset (WLO) is used to adjust the delay through the internal write command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipeline latches are added. This value is twos compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path.
52:55	RW	DDRPHY_PC_CONFIG1_P0_READ_LATENCY_OFFSET: Read Latency Offset (RLO) is used to adjust the delay through the internal read command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipeline latches are added. This value is two's compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path. The value for this field must be: RLO less than equal min{RoundDown(System_Delay)} System_Delay and min{RoundDown(System_Delay)} is defined in the GLOBAL_PHY_OFFSET field description.
56	RW	DDRPHY_PC_CONFIG1_P0_MEMCTL_CIC_FAST: '0'b - memctl_cic_o is deasserted ('0'b) in response to memctl_cis_i being asserted ('1'b) and remains deasserted until the calibration completes. '1'b - memctl_cic_o is deasserted ('0'b) in response to memctl_cis_i being asserted ('1'b) and is asserted ('1'b) in response to memctl_cis_i being deasserted ('0'b).
57	RW	DDRPHY_PC_CONFIG1_P0_MEMCTL_CTRN_IGNORE: '0'b - DDR PHY responds to the memctl_ctrn_i input. '1'b - DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a 'don't care'.
58	RW	DDRPHY_PC_CONFIG1_P0_DISABLE_MEMCTL_CAL: Reserved. This bit must be '0'b. When set to '1'b, the DFI request ack handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.
59:61	RW	DDRPHY_PC_CONFIG1_P0_MEMORY_TYPE: '001'b - DDR3 RDIMM '011'b - DDR3 LRDIMM '101'b - DDR4 RDIMM '111'b - DDR4 LRDIMM Other values are reserved.
62	RW	DDRPHY_PC_CONFIG1_P0_DDR4_LATENCY_SW: DDR4 Latency debug Switch. Should be '1'b for normal operation.
63	RW	DDRPHY_PC_CONFIG1_P0_RETRAIN_PERCAL_SW: Retrain Percal debug Switch. Affects behavior of memctl_cup_o during periodic read calibrations. '0'b - rank is requested rank and may not be the rank that was executed. '1'b - rank is next rank that requires calibration.

Register Name	*PC Resets*
Mnemonic	DPHY23.DDRPHY_PC_RESETS_P0
Address	8000C00E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RESETS_P0_PLL_RESET: '1'b - Resets the Internal PLLs
49	RW	DDRPHY_PC_RESETS_P0_SYSCLK_RESET: '1'b - Reset all logic in the internal sysclk domain.
50:63	RO	constant=0b00000000000000

Register Name	*PC Periodic Z-Cal Configuration*
Mnemonic	DPHY23.DDRPHY_PC_PER_ZCAL_CONFIG_P0
Address	8000C00F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P0_PER_ZCAL_ENA_RANK: '1'b indicates periodic external impedance calibration is enabled '0'b indicates periodic external impedance calibration is disabled Bit 0 contains the enable bit for rank 0Bit 1 contains the enable bit for rank 1Bit 2 contains the enable bit for rank 2Bit 3 contains the enable bit for rank 3Bit 4 contains the enable bit for rank 4Bit 5 contains the enable bit for rank 5Bit 6 contains the enable bit for rank 6Bit 7 contains the enable bit for rank 7
56:58	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P0_PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 next rank scheduled to run z cal001 = rank_1 next rank scheduled to run z cal010 = rank_2 next rank scheduled to run z cal011 = rank_3 next rank scheduled to run z cal100 = rank_4 next rank scheduled to run z cal101 = rank_5 next rank scheduled to run z cal110 = rank_6 next rank scheduled to run z cal111 = rank_7 next rank scheduled to run z cal
59	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P0_START_PER_ZCAL: When this bit is written to '1'b, the DDR PHY initiate a single periodic impedance calibration (equivalent to a periodic z cal timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	constant=0b0000

Register Name	*PC Power Down 1*
Mnemonic	DPHY23.DDRPHY_PC_POWERDOWN_1_P0
Address	8000C0100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_PC_POWERDOWN_1_P0_MASTER_PD_CNTL: Master Powerdown Control '0'b - DDR port is in functional mode regardless of PDR1 bits {1:15} '1'b - Powerdown status of DDR port is determined by PDR bits {1:15}
49	RW	DDRPHY_PC_POWERDOWN_1_P0_ANALOG_INPUT_STAB2: Analog Input Stabilization #2 (Separate from bit 7 to allow for separation of behavior in PDS3) '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
50	RW	DDRPHY_PC_POWERDOWN_1_P0_EYEDAC_PD: EYEDAC powerdown '0'b - EYEDAC controlled by functional mode register '1'b - EYEDAC powered down
51	RW	DDRPHY_PC_POWERDOWN_1_P0_PHYTOP_CLK_GATE: Reserved.
52	RW	DDRPHY_PC_POWERDOWN_1_P0_EXT_VREF_PD: External VREF Powerdown '0'b - Functional Mode control of External VREF Drivers '1'b - External VREF Drivers Powered Down
53	RW	DDRPHY_PC_POWERDOWN_1_P0_RESET_STAB: RESET# Stabilization '0'b - Functional Mode Control of RESET# PHY IO '1'b - Powerdown Stabilization of RESET# Signals
54	RW	DDRPHY_PC_POWERDOWN_1_P0_ANALOG_OUTPUT_STAB: Analog Output Stabilization '0'b - Functional Mode Control of Analog Outputs '1'b - Analog Outputs Forced to Known Values Immediately on Digital Side of Boundary
55	RW	DDRPHY_PC_POWERDOWN_1_P0_ANALOG_INPUT_STAB1: Analog Input Stabilization #1 '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
56	RW	DDRPHY_PC_POWERDOWN_1_P0_SYSCLK_CLK_GATE: Reserved.
57	RW	DDRPHY_PC_POWERDOWN_1_P0_DELAY_LINE_CTL_OVERRIDE: '0'b - DP18 Delay Line Power Control register is read only and is updated by hardware. '1'b - DP18 Delay Line Power Control register is read/write and is not updated by hardware.
58	RW	DDRPHY_PC_POWERDOWN_1_P0_WR_FIFO_STAB: Write FIFO & Logic Circuit Stabilization '0'b - Write FIFO and Logic Circuits under Functional Control '1'b - Write FIFO clock disabled, Flush mode set
59	RW	DDRPHY_PC_POWERDOWN_1_P0_ADR_RX_PD: Reserved.
60:61	RW	DDRPHY_PC_POWERDOWN_1_P0_DP18_RX_PD: DP18 Receiver Powerdown Control '00'b - Functional Mode Control of DP Receivers '01'b - DP Receivers in Standby Mode (RG) '10'b - Reserved. '11'b - DP Receivers in Low Power Mode (RE)
62	RW	DDRPHY_PC_POWERDOWN_1_P0_TX_TRISTATE_CNTL: Driver Tristate Control '0'b - Functional Mode Control of Drivers '1'b - DP18 Drivers in Tristate, ADR Drivers selectively either in Tristate or Pulldown under control of PDR2 For the ADR12 and ADR16 cores, this bit operates in conjunction with the register described in to determine the state of the IO during powerdown.
63	RW	DDRPHY_PC_POWERDOWN_1_P0_VCC_REG_PD: VCC Domain Regulation Powerdown '0'b - Functional Mode: VCC Voltage Regulators are on '1'b - Powerdown Mode: Voltage Regulators powered down, VCC=0v

Register Name	***PC Rank Group***
Mnemonic	DPHY23.DDRPHY_PC_RANK_GROUP_P0
Address	8000C0110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP0_PRI: '1'b - Enable Address Mirroring Rank Pair 0 Primary
49	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP0_SEC: '1'b - Enable Address Mirroring Rank Pair 0 Secondary

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP1_PRI: '1'b - Enable Address Mirroring Rank Pair 1 Primary
51	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP1_SEC: '1'b - Enable Address Mirroring Rank Pair 1 Secondary
52	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP2_PRI: '1'b - Enable Address Mirroring Rank Pair 2 Primary
53	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP2_SEC: '1'b - Enable Address Mirroring Rank Pair 2 Secondary
54	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP3_PRI: '1'b - Enable Address Mirroring Rank Pair 3 Primary
55	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_RP3_SEC: '1'b - Enable Address Mirroring Rank Pair 3 Secondary
56:57	RW	DDRPHY_PC_RANK_GROUP_P0_RANK_GROUPING: Reserved.
58	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A3_A4: '1'b - mirror A3 & A4 signals on mirrored ranks.
59	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A5_A6: '1'b - mirror A5 & A6 signals on mirrored ranks.
60	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A7_A8: '1'b - mirror A7 & A8 signals on mirrored ranks.
61	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_A11_A13: '1'b - mirror A11 & A13 signals on mirrored ranks.
62	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_BA0_BA1: '1'b - mirror BA0 & BA1 signals on mirrored ranks.
63	RW	DDRPHY_PC_RANK_GROUP_P0_ADDR_MIRROR_BG0_BG1: '1'b - mirror BG0 & BG1 signals on mirrored ranks.

Register Name	***PC Error Status 0***
Mnemonic	DPHY23.DDRPHY_PC_ERROR_STATUS0_P0
Address	8000C0120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_ERROR_STATUS0_P0_RC_ERROR: '1'b - Error in Read Control logic.
49	ROX	DDRPHY_PC_ERROR_STATUS0_P0_WC_ERROR: '1'b - Error in Write Control logic.
50	ROX	DDRPHY_PC_ERROR_STATUS0_P0_SEQ_ERROR: '1'b - Error in Sequencer Control logic.
51	ROX	DDRPHY_PC_ERROR_STATUS0_P0_CC_ERROR: Reserved.
52	ROX	DDRPHY_PC_ERROR_STATUS0_P0_APB_ERROR: '1'b - Error in Register interface logic.
53	ROX	DDRPHY_PC_ERROR_STATUS0_P0_PC_ERROR: '1'b - Error in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	*PC Error Mask 0*
Mnemonic	DPHY23.DDRPHY_PC_ERROR_MASK0_P0
Address	8000C0130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_ERROR_MASK0_P0_RC_ERROR_MASK: '1'b - Mask errors in Read Control logic.
49	RW	DDRPHY_PC_ERROR_MASK0_P0_WC_ERROR_MASK: '1'b - Mask errors in Write Control logic.
50	RW	DDRPHY_PC_ERROR_MASK0_P0_SEQ_ERROR_MASK: '1'b - Mask errors in Sequencer Control logic.
51	RW	DDRPHY_PC_ERROR_MASK0_P0_CC_ERROR_MASK: Reserved.
52	RW	DDRPHY_PC_ERROR_MASK0_P0_APB_ERROR_MASK: '1'b - Mask errors in Register Interface logic.
53	RW	DDRPHY_PC_ERROR_MASK0_P0_PC_ERROR_MASK: '1'b - Mask errors in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	*PC IO PVT N/P FET Driver Control*
Mnemonic	DPHY23.DDRPHY_PC_IO_PVT_FET_CONTROL_P0
Address	8000C0140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_PVTP: PFET Driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
53:57	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_PVTN: NFET Driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
58	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_PVT_OVERRIDE: '1'b - All drivers are updated with the PVTP and PVTN values in this register immediately. '0'b - All drivers are updated with the PVTP and PVTN values from the impedance calibration state machine.
59	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_ENABLE_ZCAL: '1'b - Enable Impedance Controller. '0'b - Disable Impedance Controller.
60	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P0_RESET_ZCAL: Reset Impedance Controller. The value of this field is driven to the zcntl_reset_o output for optional connection to the reset of an Impedance Controller.
61:63	RO	constant=0b000

Register Name	*PC VREF Driver Control*
Mnemonic	DPHY23.DDRPHY_PC_VREF_DRV_CONTROL_P0
Address	8000C0150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ0DSGN: VREF sign bit enable. This value is driven to the vrefdq0_sign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
49:52	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ0D: VREF bit enables. This value is driven to the vrefdq0_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
53	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ1DSGN: VREF sign bit enable. This value is driven to the vrefdq1_sign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
54:57	RW	DDRPHY_PC_VREF_DRV_CONTROL_P0_VREFDQ1D: VREF bit enables. This value is driven to the vrefdq1_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
58:63	RO	constant=0b000000

Register Name	***PC Initial Calibration Config0***
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_CONFIG0_P0
Address	8000C0160301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_WR_LEVEL: Enable Write Leveling during initial calibration
49	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_INITIAL_PAT_WR: Enable Initial Pattern Write during initial calibration. This bit must be set when performing Read Centering or Write Centering on memory devices that do not generate an MPR pattern. This bit must be set when performing Custom Read Centering or Custom Write Centering. If Custom Read Centering or Custom Write Centering was performed, an Initial Pattern Write of '5555' hex, the reset value of the SEQ Read/Write Data0-1 registers, must be performed before any periodic calibration routines are performed.
50	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_RDCLK_ALIGN: Enable the alignment of the internal SysClk to the Read clock during initial calibration. This calibration step requires the DQS (read) Alignment calibration step to have been performed.
52	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_READ_CTR: Enable Read Centering during initial calibration. This calibration step requires the SysClk to Read Clock alignment to have been performed.
53	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_WRITE_CTR: Enable Write Centering during initial calibration. This calibration step requires the Read Centering calibration step to have been performed.
54	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_INITIAL_COARSE_WR: Enable Initial Coarse Pattern Write during initial calibration. This calibration step requires the Write Centering calibration step to have been performed.
55	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_COARSE_RD: Enable Coarse Read Centering during initial calibration. This calibration step requires the Initial Coarse Pattern Write calibration step to have been performed.
56	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0, 2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation
57	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0,2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes.
59	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P0_ENA_RANK_PAIR: Enable Rank Pair ('1'b = Enabled, '0'b = disabled) Bit 12 contains the enable for rank pair 0.Bit 13 contains the enable for rank pair 1.Bit 14 contains the enable for rank pair 2.Bit 15 contains the enable for rank pair 3.

Register Name	***PC Initial Calibration Config1***
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_CONFIG1_P0
Address	8000C0170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_COUNT: Refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: '00'b: Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. '01'b: Use the internal Refresh Interval timer to determine when refresh commands are sent; allow refreshes to occur between calibration routines. '10'b: Reserved '11'b: Use the internal Refresh Interval timer to determine when refresh commands should be sent; in addition to allowing refreshes commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_ALL_RANKS: '1'b Indicates that all ranks should be refreshed during initial calibration. When a refresh is generated by the DDR PHY all of the chip selects are asserted at the same time during one refresh command. '0'b indicates only the rank currently being calibrated should be refreshed. When a refresh is generated by the DDR PHY, only the chip select of the rank being calibrated are asserted during the refresh command.
55:56	RW	
57:63	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P0_REFRESH_INTERVAL: Refresh Interval - This value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (min. value) = 256 MEMINTCLKO cycles between refreshes 1111111 (max value) = 32512 MEMINTCLKO cycle between refreshes For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 ('0011000'b) provides a tREFI setting of 7.68 us (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 us).The minimum value for this field is 6. If a value less than 6 is written to this field, this field will be set to 6 by hardware. When the Refresh Interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes will be issued and the internal counter will be decremented to zero. The internal pending refresh counter is a 4 bit counter with a maximum value of '15'd. An error bit will be set in the register if the internal pending refresh counter overflows.

Register Name	*PC Initial Calibration Error*
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_ERROR_P0
Address	8000C0180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_WR_LEVEL: Write leveling error occurred during initial calibration.
49	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_INITIAL_PAT_WRITE: Initial Pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
50	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_DQS_ALIGN: DQS Alignment error occurred during initial calibration.
51	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_RDCLK_ALIGN: RDCLK to SysClk alignment error occurred during initial calibration.
52	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_READ_CTR: Read centering error occurred during initial calibration.
53	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_WRITE_CTR: Write centering error occurred during initial calibration.
54	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_INITIAL_COARSE_WR: Initial Coarse Pattern Write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
55	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_COARSE_RD: Coarse read centering error occurred during initial calibration.
56	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_CUSTOM_RD: Custom pattern read centering error occurred during initial calibration.
57	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_CUSTOM_WR: Custom pattern write centering error occurred during initial calibration.
58	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_DIGITAL_EYE: Digital eye error occurred during initial calibration.
59	RO	constant=0b0
60:63	ROX	DDRPHY_PC_INIT_CAL_ERROR_P0_ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 12 reflects the status of rank pair 0.Bit 13 reflects the status of rank pair 1.Bit 14 reflects the status of rank pair 2.Bit 15 reflects the status of rank pair 3.

Register Name	*PC Initial Calibration Status*
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_STATUS_P0
Address	8000C0190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	ROX	DDRPHY_PC_INIT_CAL_STATUS_P0_INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration, '1'b indicates the rank pair has completed an initial calibration sequence. bit 0 reflects the status of rank pair 0bit 1 reflects the status of rank pair 1bit 2 reflects the status of rank pair 2bit 3 reflects the status of rank pair 3

Bits	SCOM	Field Mnemonic: Description
52:56	ROX	
57	ROX	DDRPHY_PC_INIT_CAL_STATUS_P0_PER_CAL_ABORT: Reserved. This reserved field might contain information that is helpful for hardware debugging. Do not assume that it is read as zeros Periodic Calibration Abort. Read Only. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress and the ABORT_ON_ERR_EN bit is set. This bit is reset at the start of every new calibration.
58:63	ROX	

Register Name	***PC Initial Calibration Mask***
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_MASK_P0
Address	8000C01A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_WR_LEVEL_MASK: Mask Write leveling error
49	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_INITIAL_PAT_WRITE_MASK: Mask Initial Pattern write error
50	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_DQS_ALIGN_MASK: Mask DQS Alignment error
51	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_RDCLK_ALIGN_MASK: Mask RDCLK to SysClk alignment error
52	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_READ_CTR_MASK: Mask Read centering error
53	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_WRITE_CTR_MASK: Mask Write centering error
54	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_INITIAL_COARSE_WR_MASK: Mask Initial Coarse Pattern Write centering error
55	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_COARSE_RD_MASK: Mask Coarse read centering error
56	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_CUSTOM_RD_MASK: Mask Custom pattern read centering error
57	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_CUSTOM_WR_MASK: Mask Custom pattern write centering error
58	RW	DDRPHY_PC_INIT_CAL_MASK_P0_ERROR_DIGITAL_EYE_MASK: Mask Digital Eye error
59:63	RO	constant=0b00000

Register Name	***PC IO PVT N/P FET Driver Status***
Mnemonic	DPHY23.DDRPHY_PC_IO_PVT_FET_STATUS_P0
Address	8000C01B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P0_PVTP: PFET Driver PVTP value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
53:57	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P0_PVTN: NFET Driver PVTN value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.
58:63	RO	constant=0b000000

Register Name	*PC Mode 0 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP0_P0
Address	8000C01C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP0_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP0_P0
Address	8000C01D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP0_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP0_P0
Address	8000C01E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP0_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP0_P0
Address	8000C01F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP0_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	***PC Mode 0 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP0_P0
Address	8000C0200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP0_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP0_P0
Address	8000C0210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP0_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP0_P0
Address	8000C0220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_PC_MR2_SEC_RP0_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP0_P0
Address	8000C0230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP0_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	***PC Rank Pair 2***
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR2_P0
Address	8000C0300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_TER: Tertiary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_TER_V: Value in the RANK_PAIR0_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_QUA: Quaternary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR0_QUA_V: Value in the RANK_PAIR0_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_TER: Tertiary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_TER_V: Value in the RANK_PAIR1_TER field is valid.
60:62	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_QUA: Quaternary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR2_P0_RANK_PAIR1_QUA_V: Value in the RANK_PAIR1_QUA field is valid.

Register Name	*PC Rank Pair 3*
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR3_P0
Address	8000C0310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_TER: Tertiary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_TER_V: Value in the RANK_PAIR2_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_QUA: Quaternary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR2_QUA_V: Value in the RANK_PAIR2_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_TER: Tertiary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_TER_V: Value in the RANK_PAIR3_TER field is valid.
60:62	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_QUA: Quaternary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR3_P0_RANK_PAIR3_QUA_V: Value in the RANK_PAIR3_QUA field is valid.

Register Name	*PC Chip Select ID Configuration*
Mnemonic	DPHY23.DDRPHY_PC_CSID_CFG_P0
Address	8000C0330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_CSID_CFG_P0_CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair registers, then CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
49	RW	DDRPHY_PC_CSID_CFG_P0_CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair registers, then CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
50	RW	DDRPHY_PC_CSID_CFG_P0_CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair registers, then CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
51	RW	DDRPHY_PC_CSID_CFG_P0_CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair registers, then CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
52	RW	DDRPHY_PC_CSID_CFG_P0_CS4_INIT_CAL_VALUE: If CS4 is not selected by any of the Rank Pair registers, then CS4 is driven to this value during initial calibration. If CS4 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
53	RW	DDRPHY_PC_CSID_CFG_P0_CS5_INIT_CAL_VALUE: If CS5 is not selected by any of the Rank Pair registers, then CS5 is driven to this value during initial calibration. If CS5 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.

Bits	SCOM	Field Mnemonic: Description
54	RW	DDRPHY_PC_CSID_CFG_P0_CS6_INIT_CAL_VALUE: If CS6 is not selected by any of the Rank Pair registers, then CS6 is driven to this value during initial calibration. If CS6 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
55	RW	DDRPHY_PC_CSID_CFG_P0_CS7_INIT_CAL_VALUE: If CS7 is not selected by any of the Rank Pair registers, then CS7 is driven to this value during initial calibration. If CS7 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
56:63	RO	constant=0b00000000

Register Name	***PC Rank Group Extension***
Mnemonic	DPHY23.DDRPHY_PC_RANK_GROUP_EXT_P0
Address	8000C0350301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP0_TER: '1'b - Enable Address Mirroring Rank Pair 0 Tertiary
49	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP0_QUA: '1'b - Enable Address Mirroring Rank Pair 0 Quaternary
50	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP1_TER: '1'b - Enable Address Mirroring Rank Pair 1 Tertiary
51	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP1_QUA: '1'b - Enable Address Mirroring Rank Pair 1 Quaternary
52	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP2_TER: '1'b - Enable Address Mirroring Rank Pair 2 Tertiary
53	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP2_QUA: '1'b - Enable Address Mirroring Rank Pair 2 Quaternary
54	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP3_TER: '1'b - Enable Address Mirroring Rank Pair 3 Tertiary
55	RW	DDRPHY_PC_RANK_GROUP_EXT_P0_ADDR_MIRROR_RP3_QUA: '1'b - Enable Address Mirroring Rank Pair 3 Quaternary
56:63	RO	constant=0b00000000

Register Name	***PC Mode 0 Primary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP1_P0
Address	8000C11C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP1_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP1_P0
Address	8000C11D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP1_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP1_P0
Address	8000C11E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP1_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP1_P0
Address	8000C11F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP1_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP1_P0
Address	8000C1200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_PC_MR0_SEC_RP1_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP1_P0
Address	8000C1210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP1_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP1_P0
Address	8000C1220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP1_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP1_P0
Address	8000C1230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP1_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP2_P0
Address	8000C21C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP2_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP2_P0
Address	8000C21D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP2_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP2_P0
Address	8000C21E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP2_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP2_P0
Address	8000C21F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP2_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP2_P0
Address	8000C2200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP2_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP2_P0
Address	8000C2210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP2_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP2_P0
Address	8000C2220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP2_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP2_P0
Address	8000C2230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP2_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP3_P0
Address	8000C31C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP3_P0_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP3_P0
Address	8000C31D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP3_P0_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	***PC Mode 2 Primary RP3***
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP3_P0
Address	8000C31E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP3_P0_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	***PC Mode 3 Primary RP3***
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP3_P0
Address	8000C31F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP3_P0_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	***PC Mode 0 Secondary RP3***
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP3_P0
Address	8000C3200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP3_P0_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP3_P0
Address	8000C3210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP3_P0_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP3_P0
Address	8000C3220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP3_P0_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP3_P0
Address	8000C3230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP3_P0_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*SEQ Read/Write Data 0*
Mnemonic	DPHY23.DDRPHY_SEQ_RD_WR_DATA0_P0
Address	8000C4000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA0_P0_RD_WR_DATA_REG0: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0 described inare written to MPR0. - bits 8:15 of register 0 described in are written to MPR1. - bits 0:7 of register 1 described in are written to MPR2. - bits 8:15 of register 1 described in are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	*SEQ Read/Write Data 1*
Mnemonic	DPHY23.DDRPHY_SEQ_RD_WR_DATA1_P0
Address	8000C4010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA1_P0_RD_WR_DATA_REG1: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0 described inare written to MPR0. - bits 8:15 of register 0 described in are written to MPR1. - bits 0:7 of register 1 described in are written to MPR2. - bits 8:15 of register 1 described in are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	*SEQ Configuration 0*
Mnemonic	DPHY23.DDRPHY_SEQ_CONFIG0_P0
Address	8000C4020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_CONFIG0_P0_MPR_PATTERN_BIT: Read and write calibration algorithms are based on eight-beat bursts. This register controls the readwrite burst data pattern. For Write data: The MPR_PATTERN_BIT value is available on all bit lanes of beat 1, 3, 5 and 7 and the inverse of the MPR_PATTERN_BIT on all bit lanes of beat 2, 3, 6 and 8, ensuring all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For Read data: Bit 0 is brought out as output of Sequencer and DP18 composes the expected pattern from this output.
49	RW	DDRPHY_SEQ_CONFIG0_P0_TWO_CYCLE_ADDR_EN: DDR3 and DDR4: '1'b - During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles while the appropriate chip selects are active only during the second memory clock cycle of the command. '0'b - During calibration, the address and command and chip selects are driven and active for one memory clock cycle. All other protocols: This bit must be set to '0'b. The address and command and chip selects are driven active for one memory clock cycle.
50:53	RW	DDRPHY_SEQ_CONFIG0_P0_MR_MASK_EN: Mode Register mask enable. This register masks, or disables, the mode register access by the calibration algorithms. Bits 0- 3 map to mode register 0 - 3.
54	RW	DDRPHY_SEQ_CONFIG0_P0_DELAYED_PAR: '0'b - DDR4 PAR signal is generated coincident with addresscommand signals during init cal '1'b - DDR4 PAR signal is generated one clock cycle later than addresscommand signals during init cal Bit applies to DDR4 only and is don't care for DDR3
55	RW	DDRPHY_SEQ_CONFIG0_P0_LRDIMM_CONTEXT: Value of context bit to be used during F[0]RC12 LRDIMM Control Word commands.
56	RW	DDRPHY_SEQ_CONFIG0_P0_FORCE_RESERVED: '0'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will use the DDR4 MPR registers. '1'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory. If the PROTOCOL field in the register described in does not equal DDR4, this bit is not used and is a 'don't care'.
57	RW	DDRPHY_SEQ_CONFIG0_P0_HALT_ROTATION: '0'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will rotate through the use of all 4 MPR registers by changing BA[0:1] during the calibration. '1'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will set BA[0:1] = '00'b. The same 8 beats will be read repeatedly on a particular DQ lane and the expect data will not be rotated through the 4 bytes of the register every 8 beats. If the PROTOCOL field in the register described in does not equal DDR4, this bit is not used and is a 'don't care'.
58	RW	DDRPHY_SEQ_CONFIG0_P0_FORCE_MPR: '0'b - When the PROTOCOL field in the register described in equals DDR3, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory, allowing a custom 8 bit repeating pattern to be compared during read centering. '1'b - When the PROTOCOL field in the register described in equals DDR3, Custom Read Centering and Initial Pattern Write will use 4 DRAM MPR registers, allowing Custom Read Centering to read the 4 MPR registers. This is not a mode described by the DDR3 JEDEC standard. If the PROTOCOL field in the register described in does not equal DDR3, this bit is not used and is a 'don't care'.
59:63	RW	

Register Name	*SEQ Reserved Address 0*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR0_P0
Address	8000C4030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR0_P0_RESERVED_ADDR0: Reserved Address Field 0. Exact definition is protocol dependent DDR3DDR4: Bits 0-15 map to A0-A15. The lower 2 bytes of row address are used. RLDRAM2RLDRAM3: Bits 0-15 map to A0-A15. Lower 2 bytes of the row and column address are used.

Register Name	*SEQ Reserved Address 1*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR1_P0
Address	8000C4040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR1_P0_RESERVED_ADDR1: Reserved Address Field 1. The exact definition is protocol dependent For DDR3: bits 0 - 15 are reserved. For DDR4: Bits 0 - 4 map to A16 - A20; bits 5 - 15 are reserved. This protocol uses the upper bit of the row address. For RLDRAM2 and RLDRAM3: Bits 0 - 6 map to A16 - A22; bits 7 - 15 are reserved. This protocol uses the upper bits of the row and column address.

Register Name	*SEQ Reserved Address 2*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR2_P0
Address	8000C4050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR2_P0_RESERVED_ADDR2: Reserved Address Field 2. This register controls the lower 2 bytes of the column address. Exact definition is protocol and command dependent Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION. DDR3 writes with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR3 reads with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 writes with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '1'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR4 reads with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '0'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 Refresh: A11:A15 = bits 11:15 A10 (AP) = '1'b A0:A9 = bits 0:9 DDR3 Refresh: A0:A15 = bits 0:15

Register Name	*SEQ Reserved Address 3*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR3_P0
Address	8000C4060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR3_P0_RESERVED_ADDR3: Reserved Address Field 3. The exact definition is protocol dependent For DDR3DDR4RLDRAM2RLDRAM3: bits 0-15 are reserved

Register Name	*SEQ Reserved Address 4*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR4_P0
Address	8000C4070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR4_P0_RESERVED_ADDR4: Reserved Address Field 4. Bank Address. The exact definition is protocol dependent For DDR3RLDRAM2: Bits 0 - 2 map to BA0-BA2. Bits 3 - 15 are reserved. For DDR4: Bits 0 - 1 map to BA0-BA1 and bits 2 - 3 map to BG0 - BG1. Bits 4 - 15 are reserved. MPR Reads performed by the internal calibration routines: BA0-BA1 are forced to '00'b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0-BA1 addressed used/reserved). For RLDRAM2: Bits 0 - 2 map to BA0 - BA2. Bits 3 - 15 are reserved. For RLDRAM3: Bits 0 - 3 map to BA0 - BA3. Bits 4 - 15 are reserved.

Register Name	*SEQ Error Status 0*
Mnemonic	DPHY23.DDRPHY_SEQ_ERROR_STATUS0_P0
Address	8000C4080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_MULTIPLE_REQ_ERROR: '1'b - Error: Multiple requests received at same time.
49	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_INVALID_REQTYPE_ERROR: '1'b - Error: In the current state, this request is not expected.
50	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_EARLY_REQ_ERROR: '1'b - Error: A new request arrived before acknowledge of previous request.
51:53	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 3:5 = {PC_REQ, RC_REQ, WC_REQ}
54:57	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register. See functional description section of Sequence generator for request types from each source.

Bits	SCOM	Field Mnemonic: Description
58:60	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 10:12 = {PC_REQ, RC_REQ, WC_REQ}
61:63	ROX	DDRPHY_SEQ_ERROR_STATUS0_P0_EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 13:15 = {PC_REQ, RC_REQ, WC_REQ}

Register Name	***SEQ Error Mask 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ERROR_MASK0_P0
Address	8000C4090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ERROR_MASK0_P0_MULT_REQ_ERR_MASK: '1'b - Prevent the MULTIPLE_REQ_ERROR bit from being set in the register. '0'b - Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	DDRPHY_SEQ_ERROR_MASK0_P0_INVALID_REQTYPE_ERR_MASK: '1'b - Prevent the INVALID_REQTYPE_ERROR bit from being set in the register. '0'b - Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	DDRPHY_SEQ_ERROR_MASK0_P0_EARLY_REQ_ERR_MASK: '1'b - Prevent the EARLY_REQ_ERROR bit from being set in the register. '0'b - Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	

Register Name	***SEQ ODT Write Configuration 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG0_P0
Address	8000C40A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P0_ODT_WR_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P0_ODT_WR_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Write Configuration 1***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG1_P0
Address	8000C40B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P0_ODT_WR_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P0_ODT_WR_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Write Configuration 2***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG2_P0
Address	8000C40C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P0_ODT_WR_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P0_ODT_WR_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Write Configuration 3***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG3_P0
Address	8000C40D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P0_ODT_WR_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P0_ODT_WR_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Read Configuration 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG0_P0
Address	8000C40E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P0_ODT_RD_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P0_ODT_RD_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 1*
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG1_P0
Address	8000C40F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P0_ODT_RD_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P0_ODT_RD_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 2*
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG2_P0
Address	8000C4100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P0_ODT_RD_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P0_ODT_RD_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 3*
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG3_P0
Address	8000C4110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P0_ODT_RD_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P0_ODT_RD_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ Memory Timing Parameter 0*
Mnemonic	DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM0_P0
Address	8000C4120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TMOD_CYCLES: For DDR3 and DDR4: max(tMRD, tMOD) For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TRCD_CYCLES: For DDR3 and DDR4: tRCD For RLD2 and RLD3: reserved
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TRP_CYCLES: For DDR3 and DDR4 tRP For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P0_TRFC_CYCLES: For DDR3 and DDR4: tRFC For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 1*
Mnemonic	DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM1_P0
Address	8000C4130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TZQINIT_CYCLES: For DDR3, DDR4, RLD2, and RLD3: max(tZQINIT,tZQOPER)
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TZQCS_CYCLES: For DDR3, DDR4, RLD2, and RLD3: tZQCS
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TWLDQSEN_CYCLES: For DDR3 and DDR4: tWLDQSEN For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P0_TWRMRD_CYCLES: For DDR3 and DDR4: tWLMRD For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 2*
Mnemonic	DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM2_P0
Address	8000C4140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P0_TODTLON_OFF_CYCLES: For DDR3 and DDR4: max(ODTLon, ODTLoff) When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES ^ 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change or a change from read ODT values to write ODT values, or because an MRS command is issued. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window and waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued and the DDR PHY waits for tMOD cycles and then restores the ODT pins to their prior state. For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P0_TRC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tRC
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P0_TMRSC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tMRSC
60:63	RW	

Register Name	***SEQ Low Power Termination Address 2***
Mnemonic	DPHY23.DDRPHY_SEQ_LPT_ADDR2_P0
Address	8000C4170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR2_P0_LPT_ADDR2: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ Low Power Termination Address 3***
Mnemonic	DPHY23.DDRPHY_SEQ_LPT_ADDR3_P0
Address	8000C4180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_SEQ_LPT_ADDR3_P0_LPT_ADDR3: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ Low Power Termination Address 4***
Mnemonic	DPHY23.DDRPHY_SEQ_LPT_ADDR4_P0
Address	8000C4190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR4_P0_LPT_ADDR4: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ ZQCal Encoded Rank Control 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0
Address	8000C41A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P0_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ZQCal Encoded Rank Control 1***
Mnemonic	DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0
Address	8000C41B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P0_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ODT Default Configuration***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_DEFAULT_CFG_P0
Address	8000C4240301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_DEFAULT_CFG_P0_ODT_DEF_VALUES: The eight ODT values in this register are driven to the ODT pins during MRS commands. Typically the PDT value should be set to 0 during MRS commands. However if the ODT is an ODTCID function pin, then the corresponding bit in this register should be set to the desired CID value, and the corresponding bits in the ODT Write and Read Configuration registers should be set to similar values. Where: bit 0 - ODT value for ODT pin 0 during MRS command bit 1 - ODT value for ODT pin 1 during MRS command bit 2 - ODT value for ODT pin 2 during MRS command ... bit 7 - ODT value for ODT pin 7 during MRS command
56:63	RW	

Register Name	*RC Configuration 0*
Mnemonic	DPHY23.DDRPHY_RC_CONFIG0_P0
Address	8000C8000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_RC_CONFIG0_P0_GLOBAL_PHY_OFFSET: Global PHY Offset, GPO. This field is the number of memory clock cycles added to the total read latency in the PHY. Minimum Value: When ADVANCE_RD_VALID = '0'b, the minimum value for this field is 5 + max{RoundUp(System_Delay)} - RLO. When ADVANCE_RD_VALID = '1'b, the minimum value for this field is 6 + max{RoundUp(System_Delay)} - RLO. When SPAM_EN = '1'b the minimum value calculated for this field is increased by 1. Where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1128th of a MEMINTCLKO clock cycle}) 128) + {number of pipeline stages in the addrcmd path} + {number of pipeline stages in the read data path} max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. RLO is the READ_LATENCY_OFFSET field. Maximum Value: In 2:1 mode, the maximum value for this field is 'B'h. In 4:1 mode, the maximum value for this field is 'D'h.
52	RW	DDRPHY_RC_CONFIG0_P0_ADVANCE_RD_VALID: Number of MEMCTLCLKI clock cycles MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted before the associated read data. '0'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted during the same MEMCTLCLKI clock cycle the associated read data is valid. '1'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted one MEMCTLCLKI clock cycle before the associated read data is valid. In 4:1 Data Multiplexer mode, this field must be '0'b.
53	RW	DDRPHY_RC_CONFIG0_P0_PER_DUTY_CYCLE_SW: Set to '0' for normal function. Read commands are generated during periodic cal with a 50% duty cycle. When set to '1', periodic cal issues read commands continuously.
54:56	RW	DDRPHY_RC_CONFIG0_P0_PER_REPEAT_COUNT: If this field is 000 then the number of additional periodic cals performed per request is zero. A nonzero value in this field will preform additional periodic calibrations for each request per below: 000 is No additional periodic cal iterations are performed per request. 001 is One additional periodic cal iteration is performed per request. 010 is Two additional periodic cal iterations are performed per request. .... 111 is Seven additional periodic cal iterations are performed per request.
57	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP0: '1'b - Single bit MPR pattern memory devices in Rank Pair 0. '0'b - All bit MPR pattern memory devices in Rank Pair 0.
58	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP1: '1'b - Single bit MPR pattern memory devices in Rank Pair 1. '0'b - All bit MPR pattern memory devices in Rank Pair 1.
59	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP2: '1'b - Single bit MPR pattern memory devices in Rank Pair 2. '0'b - All bit MPR pattern memory devices in Rank Pair 2.
60	RW	DDRPHY_RC_CONFIG0_P0_SINGLE_BIT_MPR_RP3: '1'b - Single bit MPR pattern memory devices in Rank Pair 3. '0'b - All bit MPR pattern memory devices in Rank Pair 3.
61	RW	DDRPHY_RC_CONFIG0_P0_ALIGN_ON_EVEN_CYCLES: This bit is only valid in 4:1 Data Multiplexer Mode. In 2:1 Data Multiplexer Mode it must be '0'b. When set, latency is added, if required, to have the read data returned on the MEMCTL Interface with the first four beats of read data returned in the same dphy_nclk cycle on the R, F, RX, and FX pins. '1'b = The first beat of a read data burst is always returned on the R pin, second beat on the F pin, third beat on the RX pin, and fourth beat on the FX pin. '0'b = The first beat of a read data burst may be returned on the R or RX pin, second beat on the F or FX pin, third beat on the RX or R pin, and fourth beat on the FX or F pin. This bit must be '0'b when a burst length that is not a multiple of four is used.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_RC_CONFIG0_P0_PERFORM_RDCLK_ALIGN: This bit must be set to '1'b in hardware. This bit is a method for behavioral simulations to skip the calibration step described in. '1'b - The calibration described in must be performed for correct operation. '0'b - In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClkRdClk Alignment. Values in the register described in have no effect. The calibration described in fails if it is run.
63	RW	DDRPHY_RC_CONFIG0_P0_STAGGERED_PATTERN: '0'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Serial mode by the DDR PHY during Custom Read Centering. '1'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Staggered mode by the DDR PHY during Custom Read Centering.

Register Name	***RC Configuration 1***
Mnemonic	DPHY23.DDRPHY_RC_CONFIG1_P0
Address	8000C8010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:61	RW	DDRPHY_RC_CONFIG1_P0_OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. Outer loop iteration count for digital eye. This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	constant=0b00

Register Name	***RC Configuration 2***
Mnemonic	DPHY23.DDRPHY_RC_CONFIG2_P0
Address	8000C8020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_RC_CONFIG2_P0_CONSEQ_PASS: The number of consecutive passes required when determining the left edge of the data eye when stepping the read strobeclock through the phase rotator. When DIGITAL_EYE_EN is '1'b this field, DIGEYE_MIN_SPACING, specifies the minimum number of cycles between outer loop iterations of digital eye (0-31 tCK cycles). This field must be set to minimum value of 6 when sampling 8 beats of data, and a minimum value of 12 when sampling 4 beats of data.
53:56	RW	
57:58	RW	DDRPHY_RC_CONFIG2_P0_BURST_WINDOW: Beats of data used for INIT and Periodic Read Eye Centering
59	RW	DDRPHY_RC_CONFIG2_P0_ALLOW_RD_FIFO_AUTO_RESET: Automatic Reset Control for RD FIFO
60:63	RO	constant=0b0000

Register Name	*RC Error Status 0*
Mnemonic	DPHY23.DDRPHY_RC_ERROR_STATUS0_P0
Address	8000C8050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_RC_ERROR_STATUS0_P0_RD_CNTL_ERROR: '1'b - Read Control Error.
49:63	RO	constant=0b000000000000000

Register Name	*RC Error Mask 0*
Mnemonic	DPHY23.DDRPHY_RC_ERROR_MASK0_P0
Address	8000C8060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_RC_ERROR_MASK0_P0_RD_CNTL_ERROR_MASK: '1'b - Mask RD_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*RC Configuration 3*
Mnemonic	DPHY23.DDRPHY_RC_CONFIG3_P0
Address	8000C8070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_RC_CONFIG3_P0_FINE_CAL_STEP_SIZE: Fine Calibration step size:000 = 1128, 001 = 164, 010 = 3128, 011 = 132100 = 5128, 101 = 364, 110 = 7128, 111 = 116
51:54	RW	DDRPHY_RC_CONFIG3_P0_COARSE_CAL_STEP_SIZE: Coarse Calibration step size:0000 = 1128, 0001 =164, 0010 = 3128, 0011 = 1320100 = 5128, 0101 = 364, 0110 = 7128, 0111 = 1161000 through 1111 = Reserved. When DIGITAL_EYE_EN is '1'b in the register described in: bit 3:4 Reserved. bit 5: DIGEYE_16_NOT_1: '1'b - Block of 16 BL8 is issued during each outer loop iteration of digital eye. '0'b - One BL8 read is issued during each outer loop iteration of digital eye. bit 6: DIGEYE_REFRESH: '1' b - Issues a precharge and refresh during every outer loop iteration of digital eye. '0'b - Issues a precharge and refresh at least once every 16 outer loop iteration of digital eye.
55:56	RWX	DDRPHY_RC_CONFIG3_P0_DQ_SEL_QUAD: The quadrant within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that will automatically increment during some types of calibrations.
57:59	RWX	DDRPHY_RC_CONFIG3_P0_DQ_SEL_LANE: The data bit within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	constant=0b0000

Register Name	*WC Configuration 0*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG0_P0
Address	8000CC000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_WC_CONFIG0_P0_TWLO_TWLOE: Number of memory clock cycles which equals: 12 + {The greater of (Twldqsen - Tmod) converted to and rounded up to the nearest integer number of memory clock cycles or (Twlo + Twloe) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {Plus: The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} Used during Write Leveling.
56	RW	DDRPHY_WC_CONFIG0_P0_WL_ONE_DQS_PULSE: '0'b - continuous DQS pulses during Write Leveling. In 2:1 mode, 32 continuous pulses are sent. In 4:1 mode, 64 continuous pulses are sent. '1'b - one DQS pulse during each Write Leveling adjustment.
57:62	RW	DDRPHY_WC_CONFIG0_P0_FW_WR_RD: Number of memory clock cycles to wait between the write and read command pairs during Write Centering.
63	RW	DDRPHY_WC_CONFIG0_P0_CUSTOM_INIT_WRITE: '1'b - Write the data pattern in the registers described in during the Initial Pattern Write algorithm. '0'b - Write the MPR like pattern defined by the field MPR_PATTERN_BIT in the register defined in during the Initial Pattern Write algorithm.

Register Name	*WC Configuration 1*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG1_P0
Address	8000CC010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG1_P0_BIG_STEP: The amount the phase rotator value is adjusted during a big step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (BIG_STEP + 1) 128th of a memory clock.
52:54	RW	DDRPHY_WC_CONFIG1_P0_SMALL_STEP: The amount the phase rotator value is adjusted during a small step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (SMALL_STEP + 1)128th of a memory clock. Note: The Write Leveling and Write Centering algorithms will achieve the most accurate results when this field is set to zero.
55:60	RW	DDRPHY_WC_CONFIG1_P0_WR_PRE_DLY: The number of dphy_nclk cycles between a write command and a precharge command in the Coarse Initial Pattern Write, Initial Write, and Write Centering calibration algorithms.
61:63	RO	constant=0b000

Register Name	*WC Configuration 2*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG2_P0
Address	8000CC020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG2_P0_NUM_VALID_SAMPLES: The Write Leveling and Write Centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The Write Leveling algorithm performs the second to last sample at the current sample point plus 12 UI to ensure that the current sample point is at the '0'b to '1'b transition.
52:57	RW	DDRPHY_WC_CONFIG2_P0_FW_RD_WR: This delay value is used in two places in the write centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as AL + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3)
58:62	RW	
63	RW	DDRPHY_WC_CONFIG2_P0_EN_RESET_WR_DELAY_WL: '1'b - The registers described in are reset at the start of the Write Leveling Calibration algorithm for rank pair 0. '0'b - The registers described in are not reset at the start of the Write Leveling Calibration algorithm.

Register Name	*WC Error Status 0*
Mnemonic	DPHY23.DDRPHY_WC_ERROR_STATUS0_P0
Address	8000CC030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_WC_ERROR_STATUS0_P0_WR_CNTL_ERROR: '1'b - Write Control Error.
49:63	RO	constant=0b000000000000000

Register Name	*WC Error Mask 0*
Mnemonic	DPHY23.DDRPHY_WC_ERROR_MASK0_P0
Address	8000CC040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_ERROR_MASK0_P0_WR_CNTL_ERROR_MASK: '1'b - Mask WR_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*WC Configuration 3*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG3_P0
Address	8000CC050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_CONFIG3_P0_DDR4_MRS_CMD_DQ_EN: In DDR4: '1'b - When a DDR4 MRS command is detected passing through the DDR PHY, the values in the MRS_CMD_DATA_N{0,1,2,3} fields in the register described in will be driven out on the DQ pins. '0'b - DQ pins are not driven when an MRS command passes through the DDR PHY. (DDR4 ballot 1716.52) For all other protocols, this bit must be '0'b.
49:54	RW	DDRPHY_WC_CONFIG3_P0_MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. WL_per_DRAM_addr = 10 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode WL_per_DRAM_addr = 18 + 2 * MRS_CMD_DQ_ON memory clock cycles in 4:1 mode
55:60	RW	DDRPHY_WC_CONFIG3_P0_MRS_CMD_DQ_OFF: MRS_CMD_DQ_OFF = the number of dphy_nclks after the DQ pin are driven the DQ pins are not set to high impedance.
61:63	RO	constant=0b000

Register Name	*APB Configuration 0*
Mnemonic	DPHY23.DDRPHY_APB_CONFIG0_P0
Address	8000D0000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_CONFIG0_P0_DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = False), this bit is reserved. If the core was configured for parity (APB_PARITY = True), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers and the PSLVERRO is not asserted due to bad write data parity.
49	RW	DDRPHY_APB_CONFIG0_P0_RESET_ERR_RPT: Write this bit to '1'b then write this bit to '0'b (toggle) to reset the registers defined in and.
50	RW	DDRPHY_APB_CONFIG0_P0_FORCE_ON_CLK_GATE: When set to '1'b, the clock gate in the APB Control Logic Block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB Control Logic Block to go to other logic blocks when the PHY is active.
51	RW	DDRPHY_APB_CONFIG0_P0_DEBUG_BUS_SEL_LO: Reserved.
52:55	RW	DDRPHY_APB_CONFIG0_P0_DEBUG__BUS_SEL_HI: Selects DP18 driving the high order half (bits 0:43) of the debugbus_o outputs.
56:63	RO	constant=0b00000000

Register Name	*APB Error Status 0*
Mnemonic	DPHY23.DDRPHY_APB_ERROR_STATUS0_P0
Address	8000D0010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_ERROR_STATUS0_P0_INVALID_ADDRESS: '1'b - Register read or write to an invalid, undefined, or unused address.
49	ROX	DDRPHY_APB_ERROR_STATUS0_P0_WR_PAR_ERR: '1'b - Write data during a write operation on the APB Interface did not have odd parity (parity error).
50:63	RO	constant=0b00000000000000

Register Name	*APB Error Mask 0*
Mnemonic	DPHY23.DDRPHY_APB_ERROR_MASK0_P0
Address	8000D0020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_ERROR_MASK0_P0_INVALID_ADDRESS_MASK: '1'b - Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	DDRPHY_APB_ERROR_MASK0_P0_WR_PAR_ERR_MASK: '1'b - Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	constant=0b00000000000000

Register Name	*APB ATEST Multiplexer Select*
Mnemonic	DPHY23.DDRPHY_APB_ATEST_MUX_SEL_P0
Address	8000D0050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_ATEST_CNTL: bit 0: Enable ATEST1 bits 1:2: Select ATEST1 source: '00'b - DP18 #0 '01'b - DP18 #1 '10'b - DP18 #2 '11'b - Reserved bit 3: Enable ATEST2 bits 4:5: Select ATEST2 source '00'b - DP18 #3 '01'b - DP18 #4 '10'b - ADR52S '11'b - Reserved
54	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR0: Inject error on FIR bit 0 (ports 02) or 32 (ports 13).
55	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR1: Inject error on FIR bit 1 (ports 02) or 33 (ports 13).
56	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR2: Inject error on FIR bit 2 (ports 02) or 34 (ports 13).

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR3: Inject error on FIR bit 3 (ports 02) or 35 (ports 13).
58	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_INJECT_FIR_ERR4: Inject error on FIR bit 4 (ports 02) or 36 (ports 13).
59:63	RW	DDRPHY_APB_ATEST_MUX_SEL_P0_VPROTH_CTL: VPROTH ATEST Register Control used during manufacturing test. Set to 0 for normal function.

Register Name	***APB FIR Error 0***
Mnemonic	DPHY23.DDRPHY_APB_FIR_ERR0_P0
Address	8000D0060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET0: Indicates a non-recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 48 on ports 0 or 2; FIR bit 56 on ports 1 or 3. Reset by RESET_ERR_RPT in.
49	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET1: Indicates a non-recoverable register parity error in PHYTOP logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
50	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET2: Indicates a recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 51 on ports 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
51	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET3: Indicates a recoverable register parity error in PHYTOP logic. Sets FIR bit 52 on ports 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.
52	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET4: Indicates a non-recoverable register parity error in ADR52 master side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
53	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_SET5: Indicates a non-recoverable register parity error in ADR52 slave side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
54:58	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_FSM_DP18: Indicates a recoverable FSM state checker error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 51 on port 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
59:63	ROX	DDRPHY_APB_FIR_ERR0_P0_FIR_ERR_REG_DP18: Indicates a recoverable register parity error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 52 on port 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***APB FIR Error 1***
Mnemonic	DPHY23.DDRPHY_APB_FIR_ERR1_P0
Address	8000D0070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_APB_FIR_ERR1_P0_PC_ERR_STATUS0: Indicates a calibration error was latched in bits 0:2, 4:5 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Bits	SCOM	Field Mnemonic: Description
53:63	ROX	DDRPHY_APB_FIR_ERR1_P0_PC_INIT_CAL_ERR: Indicates a calibration error was latched in bits 0:10 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_0
Address	800100000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P1_DP18_0_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_0
Address	800100010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_HW_VALUE:
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_0_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_0
Address	800100020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P1_DP18_0_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_0
Address	800100030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	

Bits	SCOM	Field Mnemonic: Description
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_0_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_0
Address	800100040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_0
Address	800100050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_0
Address	800100060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_0_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_0
Address	800100070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_0
Address	800100080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_0_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_0
Address	800100090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_0
Address	8001000A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_0_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_0_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_0
Address	8001000B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_0_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_0
Address	8001000C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_0
Address	8001000D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_0_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_0_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_0
Address	8001000E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P1_DP18_0_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_0
Address	8001000F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P1_DP18_0_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_0
Address	800100100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P1_DP18_0_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_0
Address	800100110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P1_DP18_0_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_0
Address	800100120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_0_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_0
Address	800100130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P1_0
Address	800100140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_0_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_0
Address	800100150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_0_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_0
Address	800100170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_0_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_0
Address	800100180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_0_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_0
Address	800100190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P1_DP18_0_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_0
Address	8001001A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P1_DP18_0_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P1_0
Address	8001001B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_0_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_0
Address	8001001C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_0_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_0
Address	8001001D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_0_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_0_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_0_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_0
Address	800100300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_0
Address	800100310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_0
Address	800100320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_0_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_0
Address	800100330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_0_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_0
Address	800100340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_0_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_0
Address	800100370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P1_DP18_0_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_0
Address	800100380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_0
Address	800100390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_0
Address	8001003A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_0
Address	8001003B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_0
Address	8001003C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_0
Address	8001003D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_0
Address	8001003E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_0
Address	8001003F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_0
Address	800100400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_0
Address	800100410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_0
Address	800100420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_0
Address	800100430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_0
Address	800100440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_0
Address	800100450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_0
Address	800100460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_0
Address	800100470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_0
Address	800100480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_0
Address	8001004A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_0
Address	8001004C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_0
Address	8001004E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_0
Address	800100500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_0
Address	800100510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_0
Address	800100520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_0
Address	800100530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_0
Address	800100540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_0
Address	800100550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_0
Address	800100560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_0
Address	800100570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_0_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_0_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_0
Address	8001005C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_0
Address	8001005D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_0
Address	800100600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_0
Address	800100610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_0
Address	800100620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_0
Address	800100630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_0
Address	800100640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_0
Address	800100650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_0
Address	800100660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_0
Address	800100670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_0
Address	800100680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_0
Address	800100690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_0
Address	8001006A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_0
Address	8001006B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_0_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_0
Address	8001006D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_0_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_0_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0
Address	8001006F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_0_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	*DP18 Read Timing Reference 0*
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_0
Address	800100700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_0_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_0_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read Timing Reference 1*
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_0
Address	800100710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_0_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_0_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	*DP18 Read DQS Timing Reference*
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_0
Address	800100720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P1_DP18_0_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_0
Address	800100730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_0_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P1_0
Address	800100740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P1_DP18_0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_0
Address	800100750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_0_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_0_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_0_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_0
Address	800100760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_0
Address	800100770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_0_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_0
Address	800100780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_0_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_0_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_0
Address	800100790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_0_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_0_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_0
Address	8001007A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_0_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_0_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_0
Address	8001007B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_0_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_0_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_0
Address	8001007C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_0
Address	8001007D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_0
Address	8001007E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_0
Address	800101040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_0
Address	800101050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_0
Address	800101090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_0
Address	8001010C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_0
Address	8001010D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_0_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_0_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_0
Address	800101130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_0
Address	800101300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_0
Address	800101310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_0
Address	800101380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_0
Address	800101390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_0
Address	8001013A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_0
Address	8001013B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_0
Address	8001013C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_0
Address	8001013D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_0
Address	8001013E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_0
Address	8001013F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_0
Address	800101400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_0
Address	800101410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_0
Address	800101420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_0
Address	800101430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_0
Address	800101440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_0
Address	800101450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_0
Address	800101460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_0
Address	800101470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_0
Address	800101480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_0
Address	8001014A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_0
Address	8001014C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_0
Address	8001014E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_0
Address	800101500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_0
Address	800101510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_0
Address	800101520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_0
Address	800101530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_0
Address	800101540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_0
Address	800101550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_0
Address	800101560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_0
Address	800101570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_0_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_0_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_0
Address	8001015C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_0
Address	8001015D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_0
Address	800101600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_0
Address	800101610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_0
Address	800101620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_0
Address	800101630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_0
Address	800101640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_0
Address	800101650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_0
Address	800101660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_0
Address	800101670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_0
Address	800101680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_0
Address	800101690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_0
Address	8001016A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_0
Address	8001016B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_0_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_0
Address	8001017C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_0
Address	8001017D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_0
Address	8001017E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_0
Address	800102040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_0
Address	800102050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_0
Address	800102090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_0
Address	8001020C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_0
Address	8001020D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_0_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_0_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_0
Address	800102130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_0
Address	800102300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_0
Address	800102310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_0
Address	800102380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_0
Address	800102390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_0
Address	8001023A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_0
Address	8001023B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_0
Address	8001023C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_0
Address	8001023D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_0
Address	8001023E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_0
Address	8001023F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_0
Address	800102400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_0
Address	800102410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_0
Address	800102420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_0
Address	800102430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_0
Address	800102440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_0
Address	800102450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_0
Address	800102460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_0
Address	800102470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_0
Address	800102480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_0
Address	8001024A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_0
Address	8001024C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_0
Address	8001024E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_0
Address	800102500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_0
Address	800102510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_0
Address	800102520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_0
Address	800102530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_0
Address	800102540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_0
Address	800102550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_0
Address	800102560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_0
Address	800102570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_0_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_0_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_0
Address	8001025C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_0
Address	8001025D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_0
Address	800102600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_0
Address	800102610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_0
Address	800102620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_0
Address	800102630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_0
Address	800102640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_0
Address	800102650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_0
Address	800102660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_0
Address	800102670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_0
Address	800102680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_0
Address	800102690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_0
Address	8001026A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_0
Address	8001026B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_0_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_0
Address	8001027C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_0
Address	8001027D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_0
Address	8001027E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_0
Address	800103040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_0
Address	800103050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_0_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_0
Address	800103090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_0_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_0
Address	8001030C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_0
Address	8001030D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_0_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_0_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_0
Address	800103130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_0_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_0
Address	800103300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_0
Address	800103310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_0_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_0
Address	800103380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_0
Address	800103390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_0
Address	8001033A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_0
Address	8001033B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_0
Address	8001033C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_0
Address	8001033D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_0
Address	8001033E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_0
Address	8001033F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_0
Address	800103400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_0
Address	800103410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_0
Address	800103420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_0
Address	800103430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_0
Address	800103440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_0
Address	800103450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_0
Address	800103460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_0
Address	800103470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_0
Address	800103480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_0
Address	8001034A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_0
Address	8001034C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_0
Address	8001034E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_0_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_0
Address	800103500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_0
Address	800103510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_0
Address	800103520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_0
Address	800103530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_0
Address	800103540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_0
Address	800103550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_0
Address	800103560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_0
Address	800103570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_0_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_0_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_0
Address	8001035C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_0
Address	8001035D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_0_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_0
Address	800103600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_0
Address	800103610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_0
Address	800103620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_0
Address	800103630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_0
Address	800103640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_0
Address	800103650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_0
Address	800103660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_0
Address	800103670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_0
Address	800103680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_0
Address	800103690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_0
Address	8001036A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_0
Address	8001036B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_0_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_0
Address	8001037C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P1_DP18_0_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_0
Address	8001037D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P1_DP18_0_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_0
Address	8001037E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_0_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Data Bit Enable 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_1
Address	800104000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE0_P1_DP18_1_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Enable 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_1
Address	800104010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_01_DATA_BIT_ENABLE1_P1_DP18_1_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_1
Address	800104020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DIR0_P1_DP18_1_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_1
Address	800104030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_01_DATA_BIT_DIR1_P1_DP18_1_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_1
Address	800104040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR0_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_1
Address	800104050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP0_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_1
Address	800104060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_01_RX_PEAK_AMP_P1_DP18_1_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_1
Address	800104070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_01_SYSCLK_PR_P1_DP18_1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_1
Address	800104080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_01_DFT_DIG_EYE_P1_DP18_1_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_1
Address	800104090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_1
Address	8001040A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_1_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_01_DRIFT_LIMITS_P1_DP18_1_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_1
Address	8001040B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_01_DEBUG_SEL_P1_DP18_1_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_1
Address	8001040C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_1
Address	8001040D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_1_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_1_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_1
Address	8001040E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS0_P1_DP18_1_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_1
Address	8001040F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS1_P1_DP18_1_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_1
Address	800104100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_01_RD_LVL_STATUS2_P1_DP18_1_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_1
Address	800104110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_01_RD_LVL_STATUS3_P1_DP18_1_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_1
Address	800104120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_1_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_1
Address	800104130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP0_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P1_1
Address	800104140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_01_RD_STATUS0_P1_DP18_1_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_1
Address	800104150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_01_RD_ERROR_MASK0_P1_DP18_1_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_1
Address	800104170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_01_WR_LVL_STATUS0_P1_DP18_1_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_1
Address	800104180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS0_P1_DP18_1_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_1
Address	800104190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS1_P1_DP18_1_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_1
Address	8001041A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_01_WR_CNTR_STATUS2_P1_DP18_1_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P1_1
Address	8001041B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_01_WR_ERROR0_P1_DP18_1_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_1
Address	8001041C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_01_WR_ERROR_MASK0_P1_DP18_1_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_1
Address	8001041D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_1_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_1_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_01_DFT_WRAP_STATUS_P1_DP18_1_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_1
Address	800104300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_1
Address	800104310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR0_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_1
Address	800104320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_0_P1_DP18_1_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_1
Address	800104330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_1_P1_DP18_1_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_1
Address	800104340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_01_PATTERN_POS_2_P1_DP18_1_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_1
Address	800104370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_OFFSET_P1_DP18_1_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_1
Address	800104380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_1
Address	800104390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_1
Address	8001043A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_1
Address	8001043B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_1
Address	8001043C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_1
Address	8001043D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_1
Address	8001043E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_1
Address	8001043F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_1
Address	800104400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_1
Address	800104410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_1
Address	800104420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_1
Address	800104430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_1
Address	800104440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_1
Address	800104450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_1
Address	800104460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_1
Address	800104470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_1
Address	800104480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_1
Address	8001044A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_1
Address	8001044C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_1
Address	8001044E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_1
Address	800104500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_1
Address	800104510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_1
Address	800104520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_1
Address	800104530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_1
Address	800104540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_1
Address	800104550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_1
Address	800104560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_1
Address	800104570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_1_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR0_P1_DP18_1_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_1
Address	8001045C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_1
Address	8001045D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_1
Address	800104600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_1
Address	800104610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_1
Address	800104620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_1
Address	800104630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_1
Address	800104640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_1
Address	800104650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_1
Address	800104660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_1
Address	800104670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_1
Address	800104680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_1
Address	800104690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_1
Address	8001046A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_1
Address	8001046B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_1_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_1
Address	8001046D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_1_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_1_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1
Address	8001046F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_1_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_1
Address	800104700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_1_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE0_P1_DP18_1_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_1
Address	800104710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_1_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_TIMING_REFERENCE1_P1_DP18_1_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_1
Address	800104720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DQS_TIMING_REFERENCE_P1_DP18_1_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_1
Address	800104730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_1_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_01_SYSCLK_PR_VALUE_P1_DP18_1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P1_1
Address	800104740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_WRCLK_PR_P1_DP18_1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_1
Address	800104750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_1_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_1_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_01_IO_TX_CONFIG0_P1_DP18_1_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_1
Address	800104760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_01_PLL_CONFIG0_P1_DP18_1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_1
Address	800104770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_01_PLL_CONFIG1_P1_DP18_1_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_1
Address	800104780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_1_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_SLICE_P1_DP18_1_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_1
Address	800104790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_1_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_SLICE_P1_DP18_1_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_1
Address	8001047A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_1_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_NFET_TERM_P1_DP18_1_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_1
Address	8001047B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_1_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_01_IO_TX_PFET_TERM_P1_DP18_1_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_1
Address	8001047C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP0_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_1
Address	8001047D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP0_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_1
Address	8001047E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP0_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_1
Address	800105040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR1_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_1
Address	800105050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP1_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_1
Address	800105090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_1
Address	8001050C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_1
Address	8001050D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_1_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_1_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_1
Address	800105130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP1_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_1
Address	800105300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_1
Address	800105310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR1_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_1
Address	800105380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_1
Address	800105390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_1
Address	8001053A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_1
Address	8001053B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_1
Address	8001053C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_1
Address	8001053D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_1
Address	8001053E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_1
Address	8001053F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_1
Address	800105400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_1
Address	800105410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_1
Address	800105420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_1
Address	800105430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_1
Address	800105440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_1
Address	800105450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_1
Address	800105460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_1
Address	800105470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_1
Address	800105480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_1
Address	8001054A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_1
Address	8001054C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_1
Address	8001054E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_1
Address	800105500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_1
Address	800105510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_1
Address	800105520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_1
Address	800105530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_1
Address	800105540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_1
Address	800105550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_1
Address	800105560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_1
Address	800105570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_1_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR1_P1_DP18_1_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_1
Address	8001055C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_1
Address	8001055D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_1
Address	800105600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_1
Address	800105610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_1
Address	800105620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_1
Address	800105630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_1
Address	800105640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_1
Address	800105650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_1
Address	800105660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_1
Address	800105670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_1
Address	800105680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_1
Address	800105690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_1
Address	8001056A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_1
Address	8001056B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_1_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_1
Address	8001057C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP1_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_1
Address	8001057D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP1_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_1
Address	8001057E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP1_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_1
Address	800106040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR2_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_1
Address	800106050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP2_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_1
Address	800106090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_1
Address	8001060C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_1
Address	8001060D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_1_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_1_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_1
Address	800106130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP2_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_1
Address	800106300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_1
Address	800106310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR2_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_1
Address	800106380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_1
Address	800106390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_1
Address	8001063A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_1
Address	8001063B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_1
Address	8001063C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_1
Address	8001063D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_1
Address	8001063E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_1
Address	8001063F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_1
Address	800106400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_1
Address	800106410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_1
Address	800106420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_1
Address	800106430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_1
Address	800106440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_1
Address	800106450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_1
Address	800106460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_1
Address	800106470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_1
Address	800106480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_1
Address	8001064A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_1
Address	8001064C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_1
Address	8001064E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_1
Address	800106500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_1
Address	800106510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_1
Address	800106520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_1
Address	800106530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_1
Address	800106540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_1
Address	800106550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_1
Address	800106560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_1
Address	800106570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_1_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR2_P1_DP18_1_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_1
Address	8001065C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_1
Address	8001065D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_1
Address	800106600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_1
Address	800106610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_1
Address	800106620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_1
Address	800106630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_1
Address	800106640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_1
Address	800106650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_1
Address	800106660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_1
Address	800106670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_1
Address	800106680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_1
Address	800106690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_1
Address	8001066A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_1
Address	8001066B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_1_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_1
Address	8001067C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP2_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_1
Address	8001067D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP2_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_1
Address	8001067E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP2_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_1
Address	800107040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_READ_CLOCK_RANK_PAIR3_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_1
Address	800107050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_01_WRCLK_EN_RP3_P1_DP18_1_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_1
Address	800107090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_01_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_1_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_1
Address	8001070C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_1
Address	8001070D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_1_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_1_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_1
Address	800107130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_01_DQS_GATE_DELAY_RP3_P1_DP18_1_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_1
Address	800107300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR0_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_1
Address	800107310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_01_DQSCLK_PR1_RANK_PAIR3_P1_DP18_1_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_1
Address	800107380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_1
Address	800107390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_1
Address	8001073A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_1
Address	8001073B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_1
Address	8001073C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_1
Address	8001073D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_1
Address	8001073E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_1
Address	8001073F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_1
Address	800107400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_1
Address	800107410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_1
Address	800107420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_1
Address	800107430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_1
Address	800107440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_1
Address	800107450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_1
Address	800107460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_1
Address	800107470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_1
Address	800107480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_1
Address	8001074A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_1
Address	8001074C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 22 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_1
Address	8001074E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_01_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_1_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_1
Address	800107500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY0_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_1
Address	800107510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY1_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_1
Address	800107520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY2_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_1
Address	800107530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY3_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_1
Address	800107540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY4_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_1
Address	800107550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY5_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_1
Address	800107560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY6_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_1
Address	800107570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_1_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_01_READ_DELAY7_RANK_PAIR3_P1_DP18_1_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_1
Address	8001075C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_1
Address	8001075D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_01_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_1_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_1
Address	800107600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_1
Address	800107610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_1
Address	800107620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_1
Address	800107630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_1
Address	800107640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_1
Address	800107650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_1
Address	800107660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_1
Address	800107670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_1
Address	800107680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_1
Address	800107690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_1
Address	8001076A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_1
Address	8001076B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_01_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_1_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_1
Address	8001077C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE0_RP3_P1_DP18_1_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_1
Address	8001077D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_01_DATA_BIT_DISABLE1_RP3_P1_DP18_1_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_1
Address	8001077E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_01_DQ_WR_OFFSET_RP3_P1_DP18_1_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	*DP18 Data Bit Enable 0*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_2
Address	800108000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P1_DP18_2_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Enable 1*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_2
Address	800108010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_2_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_2
Address	800108020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P1_DP18_2_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_2
Address	800108030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_2_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_2
Address	800108040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_2
Address	800108050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_2
Address	800108060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_2_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_2
Address	800108070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_2_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_2
Address	800108080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_2_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_2
Address	800108090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_2
Address	8001080A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_2_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_2_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_2
Address	8001080B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_2_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_2
Address	8001080C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_2
Address	8001080D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_2_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_2_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_2
Address	8001080E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P1_DP18_2_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_2
Address	8001080F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P1_DP18_2_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_2
Address	800108100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P1_DP18_2_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_2
Address	800108110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P1_DP18_2_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_2
Address	800108120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_2_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_2
Address	800108130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P1_2
Address	800108140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_2_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_2
Address	800108150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_2_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_2
Address	800108170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_2_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_2
Address	800108180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_2_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_2
Address	800108190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P1_DP18_2_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_2
Address	8001081A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P1_DP18_2_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P1_2
Address	8001081B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_2_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_2
Address	8001081C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_2_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_2
Address	8001081D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_2_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_2_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_2_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_2
Address	800108300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_2
Address	800108310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_2
Address	800108320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_2_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_2
Address	800108330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_2_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_2
Address	800108340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_2_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_2
Address	800108370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P1_DP18_2_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_2
Address	800108380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_2
Address	800108390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_2
Address	8001083A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_2
Address	8001083B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_2
Address	8001083C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_2
Address	8001083D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_2
Address	8001083E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_2
Address	8001083F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_2
Address	800108400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_2
Address	800108410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_2
Address	800108420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_2
Address	800108430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_2
Address	800108440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_2
Address	800108450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_2
Address	800108460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_2
Address	800108470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_2
Address	800108480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_2
Address	8001084A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_2
Address	8001084C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_2
Address	8001084E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_2
Address	800108500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_2
Address	800108510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_2
Address	800108520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_2
Address	800108530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_2
Address	800108540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_2
Address	800108550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_2
Address	800108560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_2
Address	800108570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_2_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_2_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_2
Address	8001085C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_2
Address	8001085D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_2
Address	800108600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_2
Address	800108610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_2
Address	800108620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_2
Address	800108630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_2
Address	800108640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_2
Address	800108650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_2
Address	800108660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_2
Address	800108670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_2
Address	800108680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_2
Address	800108690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_2
Address	8001086A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_2
Address	8001086B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_2_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_2
Address	8001086D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_2_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_2_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2
Address	8001086F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_2_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_2
Address	800108700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_2_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_2_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_2
Address	800108710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_2_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_2_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_2
Address	800108720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P1_DP18_2_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_2
Address	800108730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_2_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_2_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P1_2
Address	800108740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P1_DP18_2_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_2
Address	800108750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_2_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_2_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_2_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_2
Address	800108760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_2_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_2
Address	800108770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_2_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_2
Address	800108780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_2_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_2_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_2
Address	800108790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_2_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_2_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver N FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_2
Address	8001087A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_2_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_2_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Termination Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_2
Address	8001087B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_2_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_2_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_2
Address	8001087C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_2
Address	8001087D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_2
Address	8001087E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_2
Address	800109040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_2
Address	800109050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_2
Address	800109090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_2
Address	8001090C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_2
Address	8001090D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_2_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_2_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_2
Address	800109130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_2
Address	800109300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_2
Address	800109310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_2
Address	800109380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_2
Address	800109390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_2
Address	8001093A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_2
Address	8001093B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_2
Address	8001093C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_2
Address	8001093D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_2
Address	8001093E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_2
Address	8001093F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_2
Address	800109400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_2
Address	800109410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_2
Address	800109420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_2
Address	800109430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_2
Address	800109440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_2
Address	800109450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_2
Address	800109460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_2
Address	800109470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_2
Address	800109480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_2
Address	8001094A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_2
Address	8001094C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_2
Address	8001094E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_2
Address	800109500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_2
Address	800109510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_2
Address	800109520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_2
Address	800109530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_2
Address	800109540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_2
Address	800109550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_2
Address	800109560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_2
Address	800109570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_2_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_2_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_2
Address	8001095C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_2
Address	8001095D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_2
Address	800109600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_2
Address	800109610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_2
Address	800109620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_2
Address	800109630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_2
Address	800109640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_2
Address	800109650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_2
Address	800109660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_2
Address	800109670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_2
Address	800109680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_2
Address	800109690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_2
Address	8001096A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_2
Address	8001096B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_2_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_2
Address	8001097C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_2
Address	8001097D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_2
Address	8001097E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_2
Address	80010A040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_2
Address	80010A050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_2
Address	80010A090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_2
Address	80010A0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_2
Address	80010A0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_2_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_2_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_2
Address	80010A130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_2
Address	80010A300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_2
Address	80010A310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_2
Address	80010A380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_2
Address	80010A390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_2
Address	80010A3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_2
Address	80010A3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_2
Address	80010A3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_2
Address	80010A3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_2
Address	80010A3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_2
Address	80010A3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_2
Address	80010A400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_2
Address	80010A410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_2
Address	80010A420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_2
Address	80010A430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_2
Address	80010A440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_2
Address	80010A450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_2
Address	80010A460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_2
Address	80010A470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_2
Address	80010A480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_2
Address	80010A4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_2
Address	80010A4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_2
Address	80010A4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_2
Address	80010A500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_2
Address	80010A510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_2
Address	80010A520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_2
Address	80010A530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_2
Address	80010A540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_2
Address	80010A550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_2
Address	80010A560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_2
Address	80010A570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_2_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_2_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_2
Address	80010A5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_2
Address	80010A5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_2
Address	80010A600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_2
Address	80010A610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_2
Address	80010A620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_2
Address	80010A630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_2
Address	80010A640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_2
Address	80010A650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_2
Address	80010A660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_2
Address	80010A670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_2
Address	80010A680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_2
Address	80010A690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_2
Address	80010A6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_2
Address	80010A6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_2_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_2
Address	80010A7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_2
Address	80010A7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_2
Address	80010A7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_2
Address	80010B040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_2
Address	80010B050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_2_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_2
Address	80010B090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_2_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_2
Address	80010B0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_2
Address	80010B0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_2_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_2_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_2
Address	80010B130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_2_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_2
Address	80010B300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_2
Address	80010B310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_2_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_2
Address	80010B380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_2
Address	80010B390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_2
Address	80010B3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_2
Address	80010B3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_2
Address	80010B3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_2
Address	80010B3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_2
Address	80010B3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_2
Address	80010B3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_2
Address	80010B400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_2
Address	80010B410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_2
Address	80010B420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_2
Address	80010B430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_2
Address	80010B440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_2
Address	80010B450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_2
Address	80010B460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_2
Address	80010B470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_2
Address	80010B480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_2
Address	80010B4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_2
Address	80010B4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_2
Address	80010B4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_2_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_2
Address	80010B500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_2
Address	80010B510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_2
Address	80010B520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_2
Address	80010B530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_2
Address	80010B540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_2
Address	80010B550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_2
Address	80010B560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_2
Address	80010B570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_2_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_2_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	*DP18 Initial DQS Alignment 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_2
Address	80010B5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Initial DQS Alignment 1 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_2
Address	80010B5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_2_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	*DP18 Read Eye Size 0 RP3*
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_2
Address	80010B600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_2
Address	80010B610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_2
Address	80010B620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_2
Address	80010B630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_2
Address	80010B640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_2
Address	80010B650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_2
Address	80010B660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_2
Address	80010B670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_2
Address	80010B680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_2
Address	80010B690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_2
Address	80010B6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_2
Address	80010B6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_2_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_2
Address	80010B7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P1_DP18_2_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_2
Address	80010B7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P1_DP18_2_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_2
Address	80010B7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_2_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	*DP18 Data Bit Enable 0*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_3
Address	80010C000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE0_P1_DP18_3_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Enable 1*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_3
Address	80010C010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_23_DATA_BIT_ENABLE1_P1_DP18_3_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_3
Address	80010C020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DIR0_P1_DP18_3_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_3
Address	80010C030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_23_DATA_BIT_DIR1_P1_DP18_3_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_3
Address	80010C040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR0_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_3
Address	80010C050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP0_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_3
Address	80010C060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_23_RX_PEAK_AMP_P1_DP18_3_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_3
Address	80010C070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_23_SYSCLK_PR_P1_DP18_3_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_3
Address	80010C080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_23_DFT_DIG_EYE_P1_DP18_3_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	*DP18 DQS Read Phase Select RP0*
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_3
Address	80010C090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	*DP18 Drift Limits*
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_3
Address	80010C0A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_3_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_23_DRIFT_LIMITS_P1_DP18_3_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_3
Address	80010C0B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_23_DEBUG_SEL_P1_DP18_3_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_3
Address	80010C0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_3
Address	80010C0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_3_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_3_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_3
Address	80010C0E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS0_P1_DP18_3_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_3
Address	80010C0F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS1_P1_DP18_3_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_3
Address	80010C100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_23_RD_LVL_STATUS2_P1_DP18_3_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_3
Address	80010C110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_23_RD_LVL_STATUS3_P1_DP18_3_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_3
Address	80010C120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_3_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_3
Address	80010C130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP0_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P1_3
Address	80010C140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_23_RD_STATUS0_P1_DP18_3_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_3
Address	80010C150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_23_RD_ERROR_MASK0_P1_DP18_3_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_3
Address	80010C170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_23_WR_LVL_STATUS0_P1_DP18_3_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_3
Address	80010C180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS0_P1_DP18_3_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_3
Address	80010C190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS1_P1_DP18_3_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_3
Address	80010C1A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_23_WR_CNTR_STATUS2_P1_DP18_3_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P1_3
Address	80010C1B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_23_WR_ERROR0_P1_DP18_3_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_3
Address	80010C1C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_23_WR_ERROR_MASK0_P1_DP18_3_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_3
Address	80010C1D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_3_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_3_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_23_DFT_WRAP_STATUS_P1_DP18_3_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_3
Address	80010C300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_3
Address	80010C310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR0_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_3
Address	80010C320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_0_P1_DP18_3_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_3
Address	80010C330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_1_P1_DP18_3_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_3
Address	80010C340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_23_PATTERN_POS_2_P1_DP18_3_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_3
Address	80010C370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_OFFSET_P1_DP18_3_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_3
Address	80010C380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_3
Address	80010C390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_3
Address	80010C3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_3
Address	80010C3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_3
Address	80010C3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_3
Address	80010C3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_3
Address	80010C3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_3
Address	80010C3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_3
Address	80010C400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_3
Address	80010C410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_3
Address	80010C420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_3
Address	80010C430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_3
Address	80010C440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_3
Address	80010C450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_3
Address	80010C460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_3
Address	80010C470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_3
Address	80010C480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_3
Address	80010C4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_3
Address	80010C4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_3
Address	80010C4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_3
Address	80010C500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_3
Address	80010C510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_3
Address	80010C520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_3
Address	80010C530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_3
Address	80010C540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_3
Address	80010C550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_3
Address	80010C560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_3
Address	80010C570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_3_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR0_P1_DP18_3_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_3
Address	80010C5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_3
Address	80010C5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_3
Address	80010C600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_3
Address	80010C610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_3
Address	80010C620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_3
Address	80010C630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_3
Address	80010C640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_3
Address	80010C650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_3
Address	80010C660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_3
Address	80010C670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_3
Address	80010C680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_3
Address	80010C690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_3
Address	80010C6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_3
Address	80010C6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_3_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_3
Address	80010C6D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_3_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_3_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3
Address	80010C6F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_3_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_3
Address	80010C700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_3_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE0_P1_DP18_3_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_3
Address	80010C710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_3_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_TIMING_REFERENCE1_P1_DP18_3_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_3
Address	80010C720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DQS_TIMING_REFERENCE_P1_DP18_3_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_3
Address	80010C730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_3_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_23_SYSCLK_PR_VALUE_P1_DP18_3_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P1_3
Address	80010C740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_WRCLK_PR_P1_DP18_3_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_3
Address	80010C750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_3_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_3_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_23_IO_TX_CONFIG0_P1_DP18_3_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_3
Address	80010C760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_23_PLL_CONFIG0_P1_DP18_3_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_3
Address	80010C770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_23_PLL_CONFIG1_P1_DP18_3_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_3
Address	80010C780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_3_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_SLICE_P1_DP18_3_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_3
Address	80010C790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_3_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_SLICE_P1_DP18_3_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_3
Address	80010C7A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_3_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_NFET_TERM_P1_DP18_3_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_3
Address	80010C7B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_3_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_23_IO_TX_PFET_TERM_P1_DP18_3_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_3
Address	80010C7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP0_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_3
Address	80010C7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP0_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_3
Address	80010C7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP0_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_3
Address	80010D040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR1_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_3
Address	80010D050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP1_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_3
Address	80010D090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_3
Address	80010D0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_3
Address	80010D0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_3_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_3_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_3
Address	80010D130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP1_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_3
Address	80010D300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_3
Address	80010D310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR1_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_3
Address	80010D380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_3
Address	80010D390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_3
Address	80010D3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_3
Address	80010D3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_3
Address	80010D3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_3
Address	80010D3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_3
Address	80010D3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_3
Address	80010D3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_3
Address	80010D400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_3
Address	80010D410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_3
Address	80010D420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_3
Address	80010D430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_3
Address	80010D440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_3
Address	80010D450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_3
Address	80010D460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_3
Address	80010D470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_3
Address	80010D480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_3
Address	80010D4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_3
Address	80010D4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_3
Address	80010D4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_3
Address	80010D500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_3
Address	80010D510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_3
Address	80010D520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_3
Address	80010D530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_3
Address	80010D540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_3
Address	80010D550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_3
Address	80010D560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_3
Address	80010D570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_3_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR1_P1_DP18_3_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_3
Address	80010D5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_3
Address	80010D5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_3
Address	80010D600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_3
Address	80010D610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_3
Address	80010D620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_3
Address	80010D630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_3
Address	80010D640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_3
Address	80010D650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_3
Address	80010D660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_3
Address	80010D670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_3
Address	80010D680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_3
Address	80010D690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_3
Address	80010D6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_3
Address	80010D6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_3_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_3
Address	80010D7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP1_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_3
Address	80010D7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP1_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_3
Address	80010D7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP1_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_3
Address	80010E040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR2_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_3
Address	80010E050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP2_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_3
Address	80010E090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_3
Address	80010E0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_3
Address	80010E0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_3_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_3_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_3
Address	80010E130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP2_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_3
Address	80010E300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_3
Address	80010E310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR2_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_3
Address	80010E380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 1 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_3
Address	80010E390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 2 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_3
Address	80010E3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_3
Address	80010E3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_3
Address	80010E3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_3
Address	80010E3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_3
Address	80010E3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_3
Address	80010E3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_3
Address	80010E400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_3
Address	80010E410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_3
Address	80010E420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_3
Address	80010E430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_3
Address	80010E440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_3
Address	80010E450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_3
Address	80010E460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_3
Address	80010E470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_3
Address	80010E480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_3
Address	80010E4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_3
Address	80010E4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_3
Address	80010E4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_3
Address	80010E500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_3
Address	80010E510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_3
Address	80010E520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_3
Address	80010E530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_3
Address	80010E540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_3
Address	80010E550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_3
Address	80010E560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_3
Address	80010E570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_3_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR2_P1_DP18_3_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_3
Address	80010E5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_3
Address	80010E5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_3
Address	80010E600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_3
Address	80010E610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_3
Address	80010E620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_3
Address	80010E630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_3
Address	80010E640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_3
Address	80010E650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_3
Address	80010E660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_3
Address	80010E670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_3
Address	80010E680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_3
Address	80010E690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_3
Address	80010E6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_3
Address	80010E6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_3_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_3
Address	80010E7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP2_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_3
Address	80010E7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP2_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_3
Address	80010E7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP2_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_3
Address	80010F040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_READ_CLOCK_RANK_PAIR3_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_3
Address	80010F050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_23_WRCLK_EN_RP3_P1_DP18_3_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_3
Address	80010F090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_23_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_3_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_3
Address	80010F0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_3
Address	80010F0D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_3_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_3_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_3
Address	80010F130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_23_DQS_GATE_DELAY_RP3_P1_DP18_3_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_3
Address	80010F300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR0_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_3
Address	80010F310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_23_DQSCLK_PR1_RANK_PAIR3_P1_DP18_3_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_3
Address	80010F380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_3
Address	80010F390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_3
Address	80010F3A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_3
Address	80010F3B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_3
Address	80010F3C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_3
Address	80010F3D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_3
Address	80010F3E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_3
Address	80010F3F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_3
Address	80010F400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 9 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_3
Address	80010F410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_3
Address	80010F420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_3
Address	80010F430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_3
Address	80010F440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_3
Address	80010F450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_3
Address	80010F460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_3
Address	80010F470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_3
Address	80010F480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_3
Address	80010F4A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_3
Address	80010F4C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_3
Address	80010F4E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_23_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_3_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_3
Address	80010F500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY0_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_3
Address	80010F510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY1_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_3
Address	80010F520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY2_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_3
Address	80010F530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY3_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_3
Address	80010F540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY4_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_3
Address	80010F550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY5_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_3
Address	80010F560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY6_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_3
Address	80010F570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_3_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_23_READ_DELAY7_RANK_PAIR3_P1_DP18_3_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_3
Address	80010F5C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_3
Address	80010F5D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_23_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_3_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_3
Address	80010F600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_3
Address	80010F610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_3
Address	80010F620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_3
Address	80010F630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_3
Address	80010F640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_3
Address	80010F650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_3
Address	80010F660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_3
Address	80010F670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_3
Address	80010F680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_3
Address	80010F690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_3
Address	80010F6A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_3
Address	80010F6B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_23_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_3_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_3
Address	80010F7C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE0_RP3_P1_DP18_3_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_3
Address	80010F7D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_23_DATA_BIT_DISABLE1_RP3_P1_DP18_3_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_3
Address	80010F7E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_23_DQ_WR_OFFSET_RP3_P1_DP18_3_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	*DP18 Data Bit Enable 0*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE0_P1_4
Address	800110000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE0_P1_DP18_4_DATA_BIT_ENABLE_0_15: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send or receive data. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	*DP18 Data Bit Enable 1*
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_ENABLE1_P1_4
Address	800110010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_DATA_BIT_ENABLE_16_23: '1'b Indicates the DP18 bit is enabled, and is used for sending or receiving data to or from the memory device. This bit is calibrated as a data bit. '0'b Indicates the DP18 bit is not used to send/receive data. Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number. If DATA_BIT_ENABLE16 or if DATA_BIT_ENABLE17 is '1'b, none of the QUAD*_CLK16 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE18 or if DATA_BIT_ENABLE19 is '1'b, none of the QUAD*_CLK18 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE20 or if DATA_BIT_ENABLE21 is '1'b, none of the QUAD*_CLK20 bits can be '1'b in the registers defined in and can be '1'b. If DATA_BIT_ENABLE22 or if DATA_BIT_ENABLE23 is '1'b, none of the QUAD*_CLK22 bits can be '1'b in the registers defined in and can be '1'b This field must remain at the reset value.
56	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_DFT_FORCE_OUTPUTS: '1'b - The 24 outputs of the DP18 are forced to a low-impedance state when the corresponding DATA_BIT_ENABLE bit is '1'b and forced to a high-imp eden ce state when the corresponding DATA_BIT_ENABLE bit is '0'b. When a DP18 output is forced to a low-z state, the value driven out, '1'b or '0'b, is determined by the corresponding DATA_BIT_DIR bit value in the registers described in and. '0'b - The 24 outputs of the DP18 are not forced.
57	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_DFT_PRBS7_GEN_EN: '1'b - The 24 outputs of the DP18 are forced to a low-z state when the corresponding DATA_BIT_ENABLE bit is '1'b or when enabled as a write clock in the register defined in. An output is forced to a high-z state when the corresponding DATA_BIT_ENABLE bit is '0'b and not enabled as a write clock. When a pin is enabled via the corresponding DATA_BIT_ENABLE bit, the PRBS7 pattern is driven out. When a pin is enabled as a clock, a free running clock is driven out. Note: when a clock is enabled as differential, both outputs drive out the same free running clock. The two clocks are in phase, synchronous clocks, edge aligned clocks, and are not differential. '0'b - The 24 outputs of the DP18 are not forced.
58	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_WRAPSEL: This bit is connected directly to the S0WRAPSEL and S1WRAPSEL input pins of the analog core. This bit is used during wrap tests of the analog core. This bit must be '0'b for proper functional operation.
59	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_HW_VALUE:

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N0: This is the value that is driven by memint_d00_b - memint_d03_b, memint_d16_b, and memint_d17_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
61	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N1: This is the value that is driven by memint_d04_b - memint_d07_b, memint_d18_b, and memint_d19_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
62	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N2: This is the value that is driven by memint_d08_b - memint_d11_b, memint_d20_b, and memint_d21_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.
63	RW	DDRPHY_DP18_4_DATA_BIT_ENABLE1_P1_DP18_4_MRS_CMD_DATA_N3: This is the value that is driven by memint_d12_b - memint_d15_b, memint_d22_b, and memint_d23_b if they are enabled as DQ bits when a DDR4 MRS command is detected and this function is enabled in the register defined in. During DDR4 calibrations (initial and periodic) when this function is enabled, all data bits are driven to '0'b.

Register Name	***DP18 Data Bit Direction 0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR0_P1_4
Address	800110020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DIR0_P1_DP18_4_DATA_BIT_DIR_0_15: '1'b Indicates the DP18 bit is an output and continuously drives out a signal. A given bit must only be set when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with bidirectional data buses, '0'b indicates that the DP18 bit is bidirectional and is used to send data to the memory device and to receive data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. For protocols with unidirectional data buses, '0'b indicates the DP18 bit in an input and is used for receiving data from the memory device when the corresponding bit is set in the DP18 Data Bit Enable 0 Register. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number. This field must remain at the reset value.

Register Name	***DP18 Data Bit Direction 1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DIR1_P1_4
Address	800110030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RW	
54	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
55	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_WL_ADVANCE_DISABLE: '1'b - Disable the 12 UI advance of the second to last sample in the Write Leveling calibration algorithm. '0'b - The second to last sample in the Write Leveling calibration algorithm is 14 of a memory clock cycle delayed.
57	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_DISABLE_PING_PONG: Reserved. This bit must always be written to zero. '0'b - The DQS (write strobe) write phase rotator values toggles between the two possible phase rotator values when the rank pair written is not the same as the last rank pair that was written. '1'b - The DQS (write strobe) write phase rotator values does not toggle. Each DQS (write strobe) output uses the corresponding phase rotator.
58	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_DELAY_PING_PONG_HALF: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator multipex select is not delayed. '1'b - The DQS (write strobe) phase rotator mux select is not 12 SysClk clock cycle later. When this bit is set to '1'b, and the ADVANCE_PING_PONG bit is set to '1'b, the phase rotator mux select switches 12 a SysClk clock cycle early.
59	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ADVANCE_PING_PONG: This bit must be set to '1'b due to the timing requirements of the analog core. '0'b - The DQS (write strobe) phase rotator mux select is not advanced. '1'b - The DQS (write strobe) phase rotator mux select switches 1 SysClk clock cycle early.
60	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL0: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL0 pin on the analog core.
61	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL1: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL1 pin on the analog core.
62	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL2: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL2 pin on the analog core.
63	RW	DDRPHY_DP18_4_DATA_BIT_DIR1_P1_DP18_4_ATEST_MUX_CTL3: For correct functional operation, this bit must be '0'b. This bit is connected directly to the ATEST1CTL3 pin on the analog core.

Register Name	***DP18 Read Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR0_P1_4
Address	800110040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR0_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP0***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP0_P1_4
Address	800110050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP0_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 IO RX Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_RX_PEAK_AMP_P1_4
Address	800110060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_PEAK_AMP_CTL_SIDE0: Peaking amplifier control bits for side 0 of the DP18. This includes the following DP18 pins: MEMINTD00B - MEMINTD07B and MEMINTD16B - MEMINTD19B This field controls the AC peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
51	RW	
52:54	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_PEAK_AMP_CTL_SIDE1: Peaking amplifier control bits for side 1 of the DP18. This includes the following DP18 pins: MEMINTD08B - MEMINTD15B and MEMINTD20B - MEMINTD23B This field controls the ac peaking of the receiver. 000 is No Peaking - Default 001 - 111 is 7 steps of peaking Peaking step Min is .3 dB, Nom is .5 dB, Max is .9 dB
55	RW	
56:59	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_SXMCVREF_0_3: VREF Trim control signals. This field is connected directly to the S0MCVREF{0:3} and S1MCVREF{0:3} input pins on the analog core.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_SXPODVREF: Receiver VREF Pseudo-Open Drain mode. '0'b - 0.5*DVDD '1'b - POD mode (0.7*DVDD) This field is connected directly to the S0PODVREF and S1PODVREF inputs on the analog core.
61	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_DISABLE_TERMINATION: '0'b - Data and Strobe pins termination resistors are turned on during read data transfer. '1'b - Data and Strobe pins termination resistors are always off.
62:63	RW	DDRPHY_DP18_4_RX_PEAK_AMP_P1_DP18_4_READ_CENTERING_MODE: '00'b - Data read from memory is compared to the value of bits 0:7 of register 0 of the registers described in. '01'b - Reserved. Do not execute Custom Read Centering with this value. '10'b - Reserved. Do not execute Custom Read Centering with this value. '11'b - Data read from memory is compared to the value of the registers described in, staggered across DQ lanes as specified by the registers described in,, and and rotated through the four bytes of the registers described in every 8 beats. Use this setting for staggered, serial, and parallel modes. The values in the registers described in,, and determine whether staggered or serial mode is being used. Parallel mode is supported with firmware assist, but should not be used for calibration. These bits are not used if Custom read Centering is not enabled. these bits are not used during Periodic Read Centering. The expected read data is always an alternating 01010101 pattern during Periodic Read Centering. For all protocols except DDR3 and DDR4, Custom Read Centering must not be enabled. the value of the reserved location in DDR3 and DDR4 devices, and the value of the MPR registers in DDR4 memories, is written during Initial Pattern Write. See the CUSTOM_INIT_WRITE field. For reference, the alternating 01010101 pattern used during initial read centering and periodic read centering is typically read from the MPR0 register of DDR3 and DDR4 devices and is read from the reserved location of RLDRAM devices. The first bit of the expected 01010101 data pattern is controlled by the MPR_PATTERN_BIT of the register described in

Register Name	***DP18 SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_P1_4
Address	800110070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSZCLKPDOWN input on NEOANA18)
49:55	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select: Selects between lock status and sticky lock. '0'b - Selects the status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in is asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. Once the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE field rather than the internally calculated SYSCLK_ROT value when set to '1'b. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provides the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in resets to zero.
57	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input to the dphy_nclk to SysClk alignment circuit) Must be asserted low at least 25 SysClk cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller. (xsel_w_fence_i input to the dphy_nclk to SysClk alignment circuit) Should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input to the dphy_nclk to SysClk alignment circuit) '1'b - Positive edge alignment of SysClk to positive edge of dphy_nclk '0'b - Negative edge alignment of SysClk to positive edge of dphy_nclk
61	RW	DDRPHY_DP18_4_SYSCLK_PR_P1_DP18_4_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously align the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller only updates periodically under hardware control when an update does not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RO	constant=0b00

Register Name	***DP18 DFT Digital Eye***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_DIG_EYE_P1_4
Address	800110080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_DIGITAL_EYE_EN: '0'b - Normal operation. '1'b - Digital Eye function is enabled.
49	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_BUMP: When written to '1', capture the next beat every period (bump to the next bit in the pattern). When read, this bit always returns '0'b.
50	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_TRIG_PERIOD: '0'b = trigger every 8 beats of data. '1'b = trigger every 128 beats of data.
51	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_CNTL_POL: When the eyedac is controlled by hardware, this bit controls the polarity of the feedback to the eyedac. This bit should be left at 0 for normal operation.
52:54	RO	constant=0b000
55	RWX	DDRPHY_DP18_4_DFT_DIG_EYE_P1_DP18_4_CNTL_SRC: '0'b indicates control source is from register. '1'b indicates that the control source is a hardware algorithm.
56:63	RO	constant=0b00000000

Register Name	***DP18 DQS Read Phase Select RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_4
Address	800110090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR0_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Drift Limits***
Mnemonic	DPHY23.DDRPHY_DP18_DRIFT_LIMITS_P1_4
Address	8001100A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	
50:55	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P1_DP18_4_MIN_RD_EYE_SIZE: This is the minimum allowable read eye size for any data bit measured in the same units as RD_EYE_SIZE.
56:57	RW	
58:63	RW	DDRPHY_DP18_4_DRIFT_LIMITS_P1_DP18_4_MAX_DQS_DRIFT: This is the maximum acceptable drift of any received DQS either earlier or later than the DQS arrival time determined during initial DQS alignment. A value of 0 disables this check.

Register Name	***DP18 Debug Bus Select***
Mnemonic	DPHY23.DDRPHY_DP18_DEBUG_SEL_P1_4
Address	8001100B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_HS_PROBE_A_SEL: High Speed Probe A Select
53:57	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_HS_PROBE_B_SEL: High Speed Probe B Select
58:60	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_RD_DEBUG_SEL: Selects signals that drive the 44-bit debug bus output of DP18.
61:63	RW	DDRPHY_DP18_4_DEBUG_SEL_P1_DP18_4_WR_DEBUG_SEL: Reserved.

Register Name	***DP18 Read Delay Offset 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR0_P1_4
Address	8001100C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR0_P1_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR0_P1_4
Address	8001100D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_4_OFFSET0: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR0_P1_DP18_4_OFFSET1: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS0_P1_4
Address	8001100E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS0_P1_DP18_4_LEADING_EDGE_NOT_FOUND_0_15: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	***DP18 Read Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS1_P1_4
Address	8001100F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS1_P1_DP18_4_LEADING_EDGE_NOT_FOUND_16_23: Leading edge (left side) transition of data eye not found during read centering of the data bits on the MEMINTD{16-23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	***DP18 Read Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS2_P1_4
Address	800110100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RO	DDRPHY_DP18_4_RD_LVL_STATUS2_P1_DP18_4_TRAILING_EDGE_NOT_FOUND_0_15: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{0-15}B pin when enabled as receiving data bits.

Register Name	*DP18 Read Centering Status 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_LVL_STATUS3_P1_4
Address	800110110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:55	RO	DDRPHY_DP18_4_RD_LVL_STATUS3_P1_DP18_4_TRAILING_EDGE_NOT_FOUND_16_23: Trailing edge (right side) transition of data eye not found during read centering of the data bits on the MEMINTD{16- 23}B pin when enabled as receiving data bits.
56:63	RO	constant=0b00000000

Register Name	*DP18 Read Diagnostic Configuration 3*
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG5_P1_4
Address	800110120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_DYN_POWER_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
49	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_DYN_MCTERM_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
50	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_DYN_RX_GATE_CNTL_EN: Reserved. This bit must be set to 0 for normal operation.
51	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_CALGATE_ON: Reserved. This bit must be set to 0 for normal operation.
52	RW	DDRPHY_DP18_RD_DIA_CONFIG5_P1_DP18_4_PER_CAL_UPDATE_DISABLE: Reserved. This bit must be set to 0 for normal operation.
53:59	RW	
60:63	RO	constant=0b0000

Register Name	***DP18 DQS Gate Delay RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP0_P1_4
Address	800110130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP0_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 Read Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_STATUS0_P1_4
Address	800110140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_NO_EYE_DETECTED: Read Centering Error. No eye detected on at least one of the data pins by one of the DP18 logic blocks.
49	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_LEADING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the leading edges of the data eyes of the data bits are not found during a calibration.
50	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_TRAILING_EDGE_NOT_FOUND: Read Centering Error. Set when at least one of the trailing edges of the data eyes of the data bits are not found during a calibration.
51	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N0: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
52	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N1: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.

Bits	SCOM	Field Mnemonic: Description
53	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N2: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a a read calibration operation on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
54	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_INCOMPLETE_RD_CAL_N3: Read CenteringDQS AlignmentCoarse Read Alignment Error: Set when bit 0, 1, 2, 7, 8, 9, 10, 11, 12, or 13 of this register is set, or would be set if masked, due to a read calibration operation on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
55	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N0: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD00B-MEMINTD03B or MEMINTD16B-MEMINTD17B.
56	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N1: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD04B-MEMINTD07B or MEMINTD18B-MEMINTD19B.
57	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N2: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD08B-MEMINTD11B or MEMINTD20B-MEMINTD21B.
58	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_COARSE_PATTERN_ERR_N3: Coarse Read Alignment Error. Set when the Coarse Read Alignment algorithm does not receive a valid pattern fragment on pins MEMINTD12B-MEMINTD15B or MEMINTD22B-MEMINTD23B.
59	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_EYE_CLIPPING: Read Centering ErrorStatus. This bit activates whenever the eye center is out of the range of the strobe delay line. This is an expected condition for negative values of Trdqsdq (DQ arrives before DQS). The DDR PHY is usually capable of compensating for this. In a typical configuration, set the EYE_CLIPPLING_MASK bit be set to '1'b so that this condition is not reported as an error. When EYE_CLIPPING_MAKS is '1'b, the read centering algorithm continues calibration by using an adjacent DQS edge to perform centering. This configures normal operation of the DDR PHY in most cases with the margin for inter-symbol interference and random noise is reduced. The extent of margin reduction is dependent on jitter and the DCD characteristics of the DRAM.
60	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_NO_DQS: DQS Alignment ErrorStatus. Set when a strobe edge was not detected during DQS Alignment calibration. If a strobe is stuck or broken, its location cannot be determined. Thus, it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI. Therefore, an extra cycle of gap on rank-to-rank switching must be maintained. You can use the firmware to recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings that are associated with stuck or broken strobes to maintain the 12 UI rank-to-rank compression rule.
61	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_NO_LOCK: DQS Alignment Error and Status. Set when a phase rotator lock could not be attained on a strobe during DQS Alignment calibration. The No Lock error detect circuit detects a DQS strobe which is always '1'b or always '0'b. When a DQS strobe is always '1'b or '0'b it is considered missing or stuck. The No Lock circuit sets this bit when: a) never have a valid strobe for more than 30 samples (that is, 30 samples x 27 tCK per sample = 810 tCK)andb) the strobe then goes missing or stuck for at least 13 samples (that is, 13 samples x 27 tCK per sample = 351 tCK) If a strobe is stuck or broken, its location cannot be determined and thus it is not possible to guarantee that rank-to- rank switching delays differ by no more than 12 UI and thus an extra cycle of gap on rank-to-rank switching must be maintained. Firmware can optionally recover this extra cycle of gap on rank-to-rank switching by manually aligning all DQSaClk phase rotator settings associated with stuckbroken strobes in a way that maintains the 12 UI rank-to-rank compression rule.
62	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_DRIFT_ERROR: Periodic Read Calibration ErrorStatus: Set when a DQS signal has drifted further than the limit set in the MAX_DQS_DRIFT field of the register described in. The drift limit can be configured very tightly, in which case the activation of this bit is typically informational. Alternatively, it can be configured to a larger value that might indicate rank to rank switching is unreliable. Even in such a case, it can be ignored if the application uses a parity of ECC code as the final arbiter.
63	RWX	DDRPHY_DP18_4_RD_STATUS0_P1_DP18_4_MIN_EYE: Periodic Read Calibration ErrorStatus: Set when a data eye has closed to a value less than the value set in the MIN_RD_EYE_SIZE field of the register described in. The minimum eye size can be configured to a value that would be informational or it could be configured to a limit that reflects a customers maximum tolerance for errors in which case it could be considered to be an error.

Register Name	***DP18 Read Error Mask 0***
Mnemonic	DPHY23.DDRPHY_DP18_RD_ERROR_MASK0_P1_4
Address	800110150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_NO_EYE_DETECTED_MASK: '1'b - Mask NO_EYE_DETECTED error.
49	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_LEADING_EDGE_FOUND_MASK: '1'b - Mask LEADING_EDGE_FOUND error.
50	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_TRAILING_EDGE_FOUND_MASK: '1'b - Mask TRAILING_EDGE_FOUND error.
51	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N0_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N0 error.
52	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N1_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N1 error.
53	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N2_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N2 error.
54	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_INCOMPLETE_RD_CAL_N3_MASK: '1'b - Mask INCOMPLETE_RD_CAL_N3 error.
55	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N0_MASK: Mask COARSE_PATTERN_ERR_N0 error.
56	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N1_MASK: Mask COARSE_PATTERN_ERR_N1 error.
57	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N2_MASK: Mask COARSE_PATTERN_ERR_N2 error.
58	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_COARSE_PATTERN_ERR_N3_MASK: Mask COARSE_PATTERN_ERR_N3 error.
59	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_EYE_CLIPPING_MASK: Mask EYE_CLIPPING error.
60	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_NO_DQS_MASK: Mask NO_DQS error.
61	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_NO_LOCK_MASK: Mask NO_LOCK error.
62	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_DRIFT_ERROR_MASK: Mask DRIFT_ERROR error.
63	RW	DDRPHY_DP18_4_RD_ERROR_MASK0_P1_DP18_4_MIN_EYE_MASK: Mask MIN_EYE error.

Register Name	***DP18 Write Leveling Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_LVL_STATUS0_P1_4
Address	800110170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_CLK_LEVEL: This field is valid when the DONE bit is set. This field indicates which DQS strobeclock completed write leveling. '00'b - CLK16 '01'b - CLK18 '10'b - CLK20 '11'b - CLK22
50	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_FINE_STEPPING: '0'b - Write Leveling algorithm is doing the BIG_STEP portion of the algorithm. '1'b - Write Leveling algorithm is doing the SMALL_STEP portion of the algorithm.
51	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_DONE: Set when the Write Leveling algorithm completes.
52	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK16: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
53	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK18: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
54	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK20: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
55	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_WL_ERR_CLK22: Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
56	RW	DDRPHY_DP18_4_WR_LVL_STATUS0_P1_DP18_4_ZERO_DETECTED: '0'b - Write Leveling algorithm has not detected a low ('0'b) sample. '1'b - Write Leveling algorithm has detected a low ('0'b) sample.
57:63	RO	constant=0b0000000

Register Name	***DP18 Write Centering Status 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS0_P1_4
Address	800110180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_BIT_CENTERED: When the DONE bit is set, this field contains the bit number (0 to 23) on which the Write Centering algorithm has been applied.
53	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_SMALL_STEP_LEFT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right to find the 1st valid data sample. When this bit is set, the Write Centering algorithm will begin to small step to the left to find the left edge of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
54	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_BIG_STEP_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the left and finds the left edge of the eye. When this bit is set, the Write Centering algorithm will begin to big step to the right to find valid data again. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
55	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_MATCH_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the right after finding the left edge of the eye. When this bit is set, the Write Centering algorithm will continue to big step to the right to find the right edge of the eye. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
56	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_JUMP_BACK_RIGHT: This bit is set when invalid data is sampled when the Write Centering algorithm is big stepping to the right to find the right side of the eye. When this bit is set, the Write Centering algorithm will big step to the left to find valid data. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).

Bits	SCOM	Field Mnemonic: Description
57	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_SMALL_STEP_RIGHT: This bit is set when valid data is sampled when the Write Centering algorithm is big stepping to the left to find valid data. When this bit is set, the Write Centering algorithm will small step to the right to find the right side of the eye, the 1st invalid data sample. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS0_P1_DP18_4_DONE: This bit is set when invalid data is sampled when the Write Centering algorithm is small stepping to the right to find the right side of the eye. When the Write Centering algorithm completes successfully, this bit is set and the average of the left side and right side delay values is loaded into the register defined in which corresponds to the bit being write centered. When the Write Centering algorithm finds an error, this bit is set and the current delay value being used by the algorithm is loaded into the register defined in. The bit number being write centered loaded into the BIT_CENTERED field when this bit is set. This bit is reset when Write Centering starts on a new bit (DONE = '0'b or BIT_CENTERED = bit being Write Centered).
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 1***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS1_P1_4
Address	800110190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS1_P1_DP18_4_FW_LEFT_SIDE: Delay value of the left edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Centering Status 2***
Mnemonic	DPHY23.DDRPHY_DP18_WR_CNTR_STATUS2_P1_4
Address	8001101A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:58	RO	DDRPHY_DP18_4_WR_CNTR_STATUS2_P1_DP18_4_FW_RIGHT_SIDE: Delay value of the right edge of the write data eye found by the Write Centering algorithm.
59:63	RO	constant=0b00000

Register Name	***DP18 Write Error 0***
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR0_P1_4
Address	8001101B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK16: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 16.
49	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK18: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 18.
50	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK20: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 20.
51	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_WL_ERR_CLK22: Write Leveling Error. Set when the Write Leveling algorithm cannot find a write leveling solution for CLK 22.
52:55	RWX_RCLRPART	
56	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_VALID_NS_BIG_L: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the left edge of the eye.
57	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_INVALID_NS_SMALL_L: Write Centering ErrorStatus. Set when the Write Centering algorithm did not sample invalid data during small steps to the left to find the left edge of the eye. This status bit will not cause the Write Centering algorithm to stop. It will use the starting delay point as the left edge of the eye. This bit lane might be functional, but it might not be an optimal centering solution.
58	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_VALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample valid data during big steps to the right to find the right side of the eye.
59	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_INVALID_NS_BIG_R: Write Centering Error. Set when the Write Centering algorithm did not sample invalid data during big steps to the right to find the right side of the eye.
60	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_VALID_NS_JUMP_BACK: Write Centering Error. Set when the Write Centering Algorithm did not sample valid data during big steps to the left to find the right side of the eye.
61	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_INVALID_NS_SMALL_R: Write Centering Error. Set when the Write Centering Algorithm did not sample invalid data during small steps to the right to find the right side of the eye.
62	RWX_RCLRPART	DDRPHY_DP18_4_WR_ERROR0_P1_DP18_4_OFFSET_ERR: Write Centering Error. Set when the sum of the DQ_WR_OFFSET_N* value in the register defined in and the center value determined by the Write Centering algorithm is a negative number.
63	RWX_RCLRPART	

Register Name	*DP18 Write Error Mask 0*
Mnemonic	DPHY23.DDRPHY_DP18_WR_ERROR_MASK0_P1_4
Address	8001101C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WL_ERR_CLK16_MASK: '1'b - Mask WL_ERR_CLK16 error.
49	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WL_ERR_CLK18_MASK: '1'b - Mask WL_ERR_CLK18 error.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WL_ERR_CLK20_MASK: '1'b - Mask WL_ERR_CLK20 error.
51	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_WR_ERR_CLK22_MASK: '1'b - Mask WL_ERR_CLK22 error.
52:55	RW	
56	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_VALID_NS_BIG_L_MASK: '1'b - Mask VALID_NS_BIG_L error.
57	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_INVALID_NS_SMALL_L_MASK: '1'b - Mask INVALID_SMALL_NS_L error.
58	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_VALID_NS_BIG_R_MASK: '1'b - Mask VALID_NS_BIG_R error.
59	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_INVALID_NS_BIG_R_MASK: '1'b - Mask INVALID_NS_BIG_R error.
60	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_VALID_NS_JUMP_BACK_MASK: '1'b - Mask VALID_NS_JUMP_BACK error.
61	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_INVALID_NS_SMALL_R_MASK: '1'b - Mask INVALID_NS_SMALL_R error.
62	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_OFFSET_ERR_MASK: '1'b - Mask OFFSET_ERR error.
63	RW	DDRPHY_DP18_4_WR_ERROR_MASK0_P1_DP18_4_ADVANCE_PR_VALUE: ADVANCE_PR_VALUE Control Switch '0'b - Normal operation '1'b - Change phase rotator values going to analog core 1 SysClk clock cycle earlier on pins 0 through 15 inclusive. This provides more settling and propagation time of the phase rotator values before OE, Edat, and Odat values are driven to the analog core.

Register Name	***DP18 DFT Wrap Status***
Mnemonic	DPHY23.DDRPHY_DP18_DFT_WRAP_STATUS_P1_4
Address	8001101D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49	RWX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P1_DP18_4_CHECKER_RESET: Writing this bit to a '1' causes the SYNC and ERROR fields to clear to zero and this field self-clears.
50:51	RO	constant=0b00
52:57	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P1_DP18_4_SYNC: Each bit of this field is set during wrap testing when PRBS7 pattern is detected on the corresponding receive bit. The bits are tested in the following groups: 4 MEMINTD00B MEMINTD04B MEMINTD08B MEMINTD12B 5 MEMINTD01B MEMINTD05B MEMINTD09B MEMINTD13B 6 MEMINTD02B MEMINTD06B MEMINTD10B MEMINTD14B 7 MEMINTD03B MEMINTD07B MEMINTD11B MEMINTD15B 8 MEMINTD16B MEMINTD18B MEMINTD20B MEMINTD22B 9 MEMINTD17B MEMINTD19B MEMINTD21B MEMINTD23B
58:63	ROX	DDRPHY_DP18_4_DFT_WRAP_STATUS_P1_DP18_4_ERROR: Each bit of this field is set during wrap testing when the corresponding SYNC bit has been set but a subsequent received data bit does not match the PRBS7 pattern.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR0_P1_4
Address	800110300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR0_P1_4
Address	800110310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR0_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Pattern Position 0***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_0_P1_4
Address	800110320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD00_POS: MEMINTD00 pattern starting position.

Bits	SCOM	Field Mnemonic: Description
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD01_POS: MEMINTD01 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD02_POS: MEMINTD02 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD03_POS: MEMINTD03 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD04_POS: MEMINTD04 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD05_POS: MEMINTD05 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD06_POS: MEMINTD06 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_0_P1_DP18_4_MEMINTD07_POS: MEMINTD07 pattern starting position.

Register Name	***DP18 Pattern Position 1***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_1_P1_4
Address	800110330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD08_POS: MEMINTD08 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD09_POS: MEMINTD09 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD10_POS: MEMINTD10 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD11_POS: MEMINTD11 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD12_POS: MEMINTD12 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD13_POS: MEMINTD13 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD14_POS: MEMINTD14 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_1_P1_DP18_4_MEMINTD15_POS: MEMINTD15 pattern starting position.

Register Name	***DP18 Pattern Position 2***
Mnemonic	DPHY23.DDRPHY_DP18_PATTERN_POS_2_P1_4
Address	800110340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD16_POS: MEMINTD16 pattern starting position.
50:51	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD17_POS: MEMINTD17 pattern starting position.
52:53	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD18_POS: MEMINTD18 pattern starting position.
54:55	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD19_POS: MEMINTD19 pattern starting position.
56:57	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD20_POS: MEMINTD20 pattern starting position.
58:59	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD21_POS: MEMINTD21 pattern starting position.
60:61	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD22_POS: MEMINTD22 pattern starting position.
62:63	RW	DDRPHY_DP18_4_PATTERN_POS_2_P1_DP18_4_MEMINTD23_POS: MEMINTD23 pattern starting position.

Register Name	***DP18 DQSClk Offset***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_OFFSET_P1_4
Address	800110370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_OFFSET_P1_DP18_4_DQS_OFFSET: Prevents switching to the live DQS too early in RLDRAM or DDR4 modes, or during calibration routines of all protocols. Set this field to: DQS_OFFSET = 10 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) or more specifically: DQS_OFFSET= 2 + ceiling(peak_to_peak_jitter_magnitude_in_ticks 2) + (peak_to_peak_periodic_drift_in_ticks2)Where peak_to_peak_jitter_magnitude_in_ticks is a whole number equal to the read clock strobe (DQS) peak to peak jitter rounded up to the nearest 128th memory clock. And, peak_to_peak_periodic_drift_in_ticks is the peak to peak drift of the read clock strobe (DQS) rounded up to the nearest 128th memory clock. The + 2 term in the equation accounts for the jitter sources within the DDR PHY.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write Delay Value 0 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP0_REG_P1_4
Address	800110380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP0_REG_P1_4
Address	800110390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP0_REG_P1_4
Address	8001103A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP0_REG_P1_4
Address	8001103B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP0_REG_P1_4
Address	8001103C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 5 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP0_REG_P1_4
Address	8001103D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 6 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP0_REG_P1_4
Address	8001103E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP0_REG_P1_4
Address	8001103F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP0_REG_P1_4
Address	800110400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP0_REG_P1_4
Address	800110410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP0_REG_P1_4
Address	800110420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP0_REG_P1_4
Address	800110430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP0_REG_P1_4
Address	800110440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP0_REG_P1_4
Address	800110450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP0_REG_P1_4
Address	800110460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP0_REG_P1_4
Address	800110470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP0_REG_P1_4
Address	800110480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP0_REG_P1_4
Address	8001104A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP0_REG_P1_4
Address	8001104C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP0***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP0_REG_P1_4
Address	8001104E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP0_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR0_P1_4
Address	800110500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR0_P1_4
Address	800110510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR0_P1_4
Address	800110520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR0_P1_4
Address	800110530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR0_P1_4
Address	800110540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR0_P1_4
Address	800110550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR0_P1_4
Address	800110560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR0_P1_4
Address	800110570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P1_DP18_4_RD_DELAY0: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR0_P1_DP18_4_RD_DELAY1: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_4
Address	8001105C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b0000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_4
Address	8001105D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR0_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR0_P1_4
Address	800110600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR0_P1_4
Address	800110610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR0_P1_4
Address	800110620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR0_P1_4
Address	800110630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR0_P1_4
Address	800110640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR0_P1_4
Address	800110650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR0_P1_4
Address	800110660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR0_P1_4
Address	800110670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR0_P1_4
Address	800110680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR0_P1_4
Address	800110690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR0_P1_4
Address	8001106A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR0_P1_4
Address	8001106B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE0: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR0_P1_DP18_4_RD_EYE_SIZE1: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Diagnostic Configuration 3***
Mnemonic	DPHY23.DDRPHY_DP18_RD_DIA_CONFIG3_P1_4
Address	8001106D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_4_DESIRED_EDGE_CNTR_TARGET_HIGH: Allows firmware control over the maximum edges required before the Initial DQS Alignment algorithm stays locked into Tracking mode. A larger count value makes the algorithm work harder before declaring that a phase lock between DRAM DQS and internal DQSCLK has occurred. This count value must always be greater than the DESIRED_EDGE_CNTR_TARGET_LOW value. Use the DESIRED_EDGE_CNTR_TARGET_HIGH value 12 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.
56:63	RWX	DDRPHY_DP18_RD_DIA_CONFIG3_P1_DP18_4_DESIRED_EDGE_CNTR_TARGET_LOW: Allows firmware control over the minimum edges required before the Initial DQS Alignment algorithm toggles between Coarse Search and Tracking mode. A larger count value makes is simpler for the algorithm return to Coarse Search mode, and harder to enter Tracking mode. This count value must always be smaller than the DESIRED_EDGE_CNTR_TARGET_HIGH value and greater than zero. Use the DESIRED_EDGE_CNTR_TARGET_LOW value 8 to improve jitter filtering characteristics during the INitial DQS Alignment algorithm. This field is not used during the Periodic DQS Alignment algorithm.

Register Name	***DP18 Delay Line Power Control***
Mnemonic	DPHY23.DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4
Address	8001106F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD0_PWR_CTL: Quadrant 0 Delay Line Control.
52:55	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD1_PWR_CTL: Quadrant 1 Delay Line Control.
56:59	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD2_PWR_CTL: Quadrant 2 Delay Line Control.
60:63	RWX	DDRPHY_DP18_DELAY_LINE_PWR_CTL_P1_4_QUAD3_PWR_CTL: Quadrant 3 Delay Line Control.

Register Name	***DP18 Read Timing Reference 0***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE0_P1_4
Address	800110700301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P1_DP18_4_REFERENCE0: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE0_P1_DP18_4_REFERENCE1: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read Timing Reference 1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_TIMING_REFERENCE1_P1_4
Address	800110710301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P1_DP18_4_REFERENCE2: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17 and nn{1} = 08, 09, 10, 11, 20, 21 during calibration. This value should not be altered via the programming interface, except for diagnostic use.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_TIMING_REFERENCE1_P1_DP18_4_REFERENCE3: A reference value used by hardware for pins MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23 during calibration. This value should not be altered via the programming interface, except for diagnostic use.

Register Name	***DP18 Read DQS Timing Reference***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DQS_TIMING_REFERENCE_P1_4
Address	800110720301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DQS_TIMING_REFERENCE_P1_DP18_4_REFERENCE: A reference value used by hardware for the DQS pins. This value should not be altered via the programming interface except for diagnostic use.

Bits	SCOM	Field Mnemonic: Description
56:63	RO	constant=0b00000000

Register Name	*DP18 SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_DP18_SYSCLK_PR_VALUE_P1_4
Address	800110730301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	ROX	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P1_DP18_4_SYSCLK_ROT: Internally calculated value of Memory Controller Clock (MEMCTLCLKI) Phase to SysClock (SYSCLK) phase offset. Used to set the SysClk phase rotator when SYSCLK_ROT_OVERRIDE_EN=0. These bits reset, but are continually loaded with the value that is calculated by the dphy_nclk to SysClk alignment circuit for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_DP18_4_SYSCLK_PR_VALUE_P1_DP18_4_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. See the SYSCLK_ROT_OVERRIDE field.
57:63	RO	constant=0b0000000

Register Name	*DP18 WrClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_PR_P1_4
Address	800110740301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_WRCLK_PR_P1_DP18_4_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RO	constant=0b00000000

Register Name	*DP18 IO TX Configuration 0*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_CONFIG0_P1_4
Address	800110750301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P1_DP18_4_INTERP_SIG_SLEW: Interpolated Signal Slew Control Bits 0:3 are connected to inputs SxPRSTGH{0-3} and SYSPRSTGH{0-3} on the analog core. This field provides slew rate control to phase rotators. Set this field as follows for the given Transfer rate: '1000'b - 666 MTs '0100'b - 800 MTs '1100'b - 1066 MTs '0010'b - 1333 MTs '1010'b - 1600 MTs '0110'b - 1866 MTs '1001'b - 2133 MTs '1001'b - 2400 MTs All other values reserved. When this field is set to '0000'b, the DDR PHY is not operational.
52:55	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P1_DP18_4_POST_CURSOR: Post Cursor Bits 4:7 are connected to inputs SxPOSTCURSOR{0-3} on the analog core. This field selects the amount of equalization enabled in the data drivers. While this vector determines whether a subset of the slices in each IO operate in either a normal data or post cursor data regime, it is the data history which determines the amount of equalization provided at the driver output at any time. 0001 to 1111 = Equalization Equalization determined by the impedance of the driver, The number of P an N slices on and the value of the post cursor. Equalization is determined by the following formula: Values: NORMAL_FUNCTIONAL_MODE__NO_EQUALIZATION_=>0b0000
56:59	RW	DDRPHY_DP18_4_IO_TX_CONFIG0_P1_DP18_4_SLEW_CTL: Slew Control Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings do not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 34 Ohms, Nominal process 0110 - 1111 = approximately a 180 mV increment per step. Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101
60:63	RO	constant=0b0000 Values: 2_83_VNS_AVERAGE=>0b0000 3_35_VNS_AVERAGE=>0b0001 4_35_VNS_AVERAGE=>0b0010 5_16_VNS_AVERAGE=>0b0011 6_16_VNS_AVERAGE=>0b0100 6_50_VNS_AVERAGE=>0b0101

Register Name	***DP18 PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG0_P1_4
Address	800110760301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111

Bits	SCOM	Field Mnemonic: Description
51:53	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_DP18_4_PLL_CONFIG0_P1_DP18_4_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***DP18 PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_DP18_PLL_CONFIG1_P1_4
Address	800110770301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b0 CMFB_INTERNAL=>0b1
54:55	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_CE0DLTVCCA: This register bit is logically OR'ed with CE0DLTVCCA input of the DP18 Hardcore then connect to the CE0DLTVCCA input of the analog core. For proper functional operation this bit must be 1'b0.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_CE0DLTVCC1: This register bit is logically OR'ed with the CE0DLTVCCD1I input of the DP18 Hardcore then connected to the CE0DLTVCCD1 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
60	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_CE0DLTVCC2: This register bit is logically OR'ed with the CE0DLTVCCD2I input of the DP18 Hardcore then connected to the CE0DLTVCCD2 input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
61	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_S0INSDLYTAP: This register bit is connected to the D0INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
62	RW	DDRPHY_DP18_4_PLL_CONFIG1_P1_DP18_4_S1INSDLYTAP: This register bit is connected to the D1INSDLYTAP input of the DP18 analog core. For proper functional operation, this bit must be '0'b.
63	RO	constant=0b0

Register Name	***DP18 IO Driver N FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_SLICE_P1_4
Address	800110780301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P1_DP18_4_EN_SLICE_N_WR: Driver N FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICENDRV{0-7} and S1ENSLICENDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_SLICE_P1_DP18_4_EN_SLICE_N_WR_FFE: Driver N FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFEDRV{0-3} and S1ENSLICENFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 IO Driver P FET Slice Enable***
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_SLICE_P1_4
Address	800110790301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P1_DP18_4_EN_SLICE_P_WR: Driver P FET slice enable, non-FFE, at 240 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICEPDRV{0-7} and S1ENSLICEPDRV{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_SLICE_P1_DP18_4_EN_SLICE_P_WR_FFE: Driver P FET slice enable, FFE, at 480 ohmsslice. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFEDRV{0-3} and S1ENSLICEFFEDRV{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver N FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_NFET_TERM_P1_4
Address	8001107A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P1_DP18_4_EN_TERM_N_WR: Driver N FET slice termination enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice 0:7 are connected to inputs S0ENSLICENTERM{0-7} and S1ENSLICENTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_NFET_TERM_P1_DP18_4_EN_TERM_N_WR_FFE: Driver N FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICENFFETERM{0-3} and S1ENSLICENFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	*DP18 IO Driver P FET Slice Termination Enable*
Mnemonic	DPHY23.DDRPHY_DP18_IO_TX_PFET_TERM_P1_4
Address	8001107B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P1_DP18_4_EN_TERM_P_WR: Driver P FET slice enable, non-FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 0:7 are connected to inputs S0ENSLICEPTERM{0-7} and S1ENSLICEPTERM{0-7} on the analog core.
56:59	RW	DDRPHY_DP18_4_IO_TX_PFET_TERM_P1_DP18_4_EN_TERM_P_WR_FFE: Driver P FET slice enable, FFE. Each bit in this multi-bit field controls one slice. '1'b - Enable FET slice '0'b - Disable FET slice bits 8:11 are connected to inputs S0ENSLICEPFFETERM{0-3} and S1ENSLICEPFFETERM{0-3} on the analog core.
60:63	RO	constant=0b0000

Register Name	***DP18 Data Bit Disable 0 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP0_P1_4
Address	8001107C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP0_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP0_P1_4
Address	8001107D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP0_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP0***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP0_P1_4
Address	8001107E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Bits	SCOM	Field Mnemonic: Description
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP0_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR1_P1_4
Address	800111040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR1_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP1***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP1_P1_4
Address	800111050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP1_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_4
Address	800111090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR1_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR1_P1_4
Address	8001110C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR1_P1_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR1_P1_4
Address	8001110D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_4_OFFSET2: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR1_P1_DP18_4_OFFSET3: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP1_P1_4
Address	800111130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP1_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR1_P1_4
Address	800111300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR1_P1_4
Address	800111310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR1_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP1_REG_P1_4
Address	800111380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP1_REG_P1_4
Address	800111390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP1_REG_P1_4
Address	8001113A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 3 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP1_REG_P1_4
Address	8001113B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP1_REG_P1_4
Address	8001113C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP1_REG_P1_4
Address	8001113D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP1_REG_P1_4
Address	8001113E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP1_REG_P1_4
Address	8001113F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 8 RP1*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP1_REG_P1_4
Address	800111400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP1_REG_P1_4
Address	800111410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP1_REG_P1_4
Address	800111420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 11 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP1_REG_P1_4
Address	800111430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 12 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP1_REG_P1_4
Address	800111440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 13 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP1_REG_P1_4
Address	800111450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 14 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP1_REG_P1_4
Address	800111460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 15 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP1_REG_P1_4
Address	800111470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 16 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP1_REG_P1_4
Address	800111480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP1_REG_P1_4
Address	8001114A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP1_REG_P1_4
Address	8001114C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP1***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP1_REG_P1_4
Address	8001114E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP1_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR1_P1_4
Address	800111500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR1_P1_4
Address	800111510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR1_P1_4
Address	800111520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.

Bits	SCOM	Field Mnemonic: Description
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR1_P1_4
Address	800111530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR1_P1_4
Address	800111540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR1_P1_4
Address	800111550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR1_P1_4
Address	800111560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR1_P1_4
Address	800111570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P1_DP18_4_RD_DELAY2: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR1_P1_DP18_4_RD_DELAY3: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_4
Address	8001115C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_4
Address	8001115D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR1_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR1_P1_4
Address	800111600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR1_P1_4
Address	800111610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR1_P1_4
Address	800111620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR1_P1_4
Address	800111630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR1_P1_4
Address	800111640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR1_P1_4
Address	800111650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR1_P1_4
Address	800111660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR1_P1_4
Address	800111670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR1_P1_4
Address	800111680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR1_P1_4
Address	800111690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR1_P1_4
Address	8001116A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR1_P1_4
Address	8001116B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE2: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR1_P1_DP18_4_RD_EYE_SIZE3: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP1_P1_4
Address	8001117C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP1_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP1_P1_4
Address	8001117D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP1_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP1***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP1_P1_4
Address	8001117E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP1_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR2_P1_4
Address	800112040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.

Bits	SCOM	Field Mnemonic: Description
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR2_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP2***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP2_P1_4
Address	800112050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP2_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_4
Address	800112090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR2_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR2_P1_4
Address	8001120C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR2_P1_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR2_P1_4
Address	8001120D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_4_OFFSET4: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR2_P1_DP18_4_OFFSET5: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP2_P1_4
Address	800112130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP2_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR2_P1_4
Address	800112300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR2_P1_4
Address	800112310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR2_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP2_REG_P1_4
Address	800112380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP2_REG_P1_4
Address	800112390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP2_REG_P1_4
Address	8001123A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP2_REG_P1_4
Address	8001123B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 4 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP2_REG_P1_4
Address	8001123C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP2_REG_P1_4
Address	8001123D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP2_REG_P1_4
Address	8001123E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 7 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP2_REG_P1_4
Address	8001123F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP2_REG_P1_4
Address	800112400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP2_REG_P1_4
Address	800112410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 10 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP2_REG_P1_4
Address	800112420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP2_REG_P1_4
Address	800112430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP2_REG_P1_4
Address	800112440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP2_REG_P1_4
Address	800112450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP2_REG_P1_4
Address	800112460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP2_REG_P1_4
Address	800112470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP2_REG_P1_4
Address	800112480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 18 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP2_REG_P1_4
Address	8001124A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 20 RP2*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP2_REG_P1_4
Address	8001124C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP2***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP2_REG_P1_4
Address	8001124E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP2_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR2_P1_4
Address	800112500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR2_P1_4
Address	800112510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR2_P1_4
Address	800112520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR2_P1_4
Address	800112530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR2_P1_4
Address	800112540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR2_P1_4
Address	800112550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR2_P1_4
Address	800112560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR2_P1_4
Address	800112570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P1_DP18_4_RD_DELAY4: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR2_P1_DP18_4_RD_DELAY5: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_4
Address	8001125C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_4
Address	8001125D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0

Bits	SCOM	Field Mnemonic: Description
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR2_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR2_P1_4
Address	800112600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR2_P1_4
Address	800112610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR2_P1_4
Address	800112620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR2_P1_4
Address	800112630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR2_P1_4
Address	800112640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR2_P1_4
Address	800112650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR2_P1_4
Address	800112660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR2_P1_4
Address	800112670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR2_P1_4
Address	800112680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR2_P1_4
Address	800112690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR2_P1_4
Address	8001126A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR2_P1_4
Address	8001126B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE4: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR2_P1_DP18_4_RD_EYE_SIZE5: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP2_P1_4
Address	8001127C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP2_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP2_P1_4
Address	8001127D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP2_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP2***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP2_P1_4
Address	8001127E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP2_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***DP18 Read Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_CLOCK_RANK_PAIR3_P1_4
Address	800113040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n), when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an incoming clock to capture data on the following pins when the following pins are enabled and configured as data inputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.
58	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD16B(n) is the true side and MEMINTD17B(n) is the compliment side of the differential pair. '1'b - MEMINTD16B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD18B(n) is the true side and MEMINTD19B(n) is the compliment side of the differential pair. '1'b - MEMINTD18B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD20B(n) is the true side and MEMINTD21B(n) is the compliment side of the differential pair. '1'b - MEMINTD20B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_READ_CLOCK_RANK_PAIR3_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to receive an incoming clock or strobe to capture data. MEMINTD22B(n) is the true side and MEMINTD23B(n) is the compliment side of the differential pair. '1'b - MEMINTD22B(n) pin is configured as single-ended to receive an incoming clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62:63	RO	constant=0b00

Register Name	***DP18 Write Clock Enable & Selection RP3***
Mnemonic	DPHY23.DDRPHY_DP18_WRCLK_EN_RP3_P1_4
Address	800113050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD0_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) Where n is the DP18 Instance Number.
49	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD1_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) Where n is the DP18 Instance Number.
50	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
51	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK16: '1'b - MEMINTD16B(n), and MEMINTD17B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
52	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD0_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) Where n is the DP18 Instance Number.
53	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD1_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) Where n is the DP18 Instance Number.
54	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) Where n is the DP18 Instance Number.
55	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK20: '1'b - MEMINTD20B(n), and MEMINTD21B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.
56	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
57	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK22: '1'b - MEMINTD22B(n), and MEMINTD23B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) Where n is the DP18 Instance Number.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK16_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD16B(n) and MEMINTD17B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD16B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
59	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK18_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD18B(n) and MEMINTD19B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD18B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
60	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK20_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD20B(n) and MEMINTD21B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD20B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
61	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_CLK22_SINGLE_ENDED: Reserved. This bit must be '0'b. '0'b - MEMINTD22B(n) and MEMINTD23B(n) pins are configured as a differential pair to send an outgoing clock or strobe to capture data. '1'b - MEMINTD22B(n) pin is configured as single-ended to send an outgoing clock or strobe to capture data. This bit must be set to the same value in each valid rank pair register.
62	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD2_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) Where n is the DP18 Instance Number.
63	RW	DDRPHY_DP18_4_WRCLK_EN_RP3_P1_DP18_4_QUAD3_CLK18: '1'b - MEMINTD18B(n), and MEMINTD19B(n) when configured as differential, is used as an outgoing clock to capture data on the following pins when the following pins are enabled and configured as outputs: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) Where n is the DP18 Instance Number.

Register Name	***DP18 DQS Read Phase Select RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_4
Address	800113090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
50:51	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT0: Phase Select for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16, 17.
52:53	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
54:55	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT1: Phase Select for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19.
56:57	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.
58:59	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT2: Phase Select for MEMINTDnnB pins, where nn{0} = 08, 09, 10, 11, 20, 21.

Bits	SCOM	Field Mnemonic: Description
60:61	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_DQSCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.
62:63	RW	DDRPHY_DP18_4_DQS_RD_PHASE_SELECT_RANK_PAIR3_P1_DP18_4_RDCLK_SELECT3: Phase Select for MEMINTDnnB pins, where nn{0} = 12, 13, 14, 15, 22, 23.

Register Name	***DP18 Read Delay Offset 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET0_RANK_PAIR3_P1_4
Address	8001130C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET0_RANK_PAIR3_P1_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 Read Delay Offset 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY_OFFSET1_RANK_PAIR3_P1_4
Address	8001130D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_4_OFFSET6: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 00, 01, 02, 03, 16,17 and nn{1} = 08, 09, 10, 11, 20, 21. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_READ_DELAY_OFFSET1_RANK_PAIR3_P1_DP18_4_OFFSET7: Read Delay Offset for MEMINTDnnB pins, where nn{0} = 04, 05, 06, 07, 18, 19 and nn{1} = 12, 13, 14, 15, 22, 23. This value can be written via the programming interface and is stored in two's compliment form so the range of possible values is -64 to +63. This value is added to the read delay value for the applicable pins. This register should not be set to a non-zero value unless detailed timing analysis has shown that for a particular configuration, the read centering algorithm places sampling point off from the eye center.

Register Name	***DP18 DQS Gate Delay RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQS_GATE_DELAY_RP3_P1_4
Address	800113130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:51	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N0: This field determines when the DQS gate is opened to receive the read strobe on the DQ00-DQ03 and DQ16-DQ17 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
52	RO	constant=0b0
53:55	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N1: This field determines when the DQS gate is opened to receive the read strobe on the DQ04-DQ07 and DQ18-DQ19 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
56	RO	constant=0b0
57:59	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N2: This field determines when the DQS gate is opened to receive the read strobe on DQ08-DQ11 and DQ20-DQ21 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.
60	RO	constant=0b0
61:63	RW	DDRPHY_DP18_4_DQS_GATE_DELAY_RP3_P1_DP18_4_DQS_GATE_DELAY_N3: This field determines when the DQS gate is opened to receive the read strobe on DQ12-DQ15 and DQ22-DQ23 inputs. This field determines when the read gate is opened. Number of MEMINTCLKO clock cycles.

Register Name	***DP18 DQSClk Phase Rotator Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR0_RANK_PAIR3_P1_4
Address	800113300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR0_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 DQSClk Phase Rotator Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQSCLK_PR1_RANK_PAIR3_P1_4
Address	800113310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N0: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B-MEMINTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RW	DDRPHY_DP18_4_DQSCLK_PR1_RANK_PAIR3_P1_DP18_4_DQSCLK_ROT_CLK_N1: DQS Clock Rotator Value to align SysClk to the incoming DQS strobe for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B-MEMINTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Write Delay Value 0 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_0_RP3_REG_P1_4
Address	800113380301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_0_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 1 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_1_RP3_REG_P1_4
Address	800113390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_1_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 2 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_2_RP3_REG_P1_4
Address	8001133A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_2_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 3 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_3_RP3_REG_P1_4
Address	8001133B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_3_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 4 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_4_RP3_REG_P1_4
Address	8001133C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_4_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 5 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_5_RP3_REG_P1_4
Address	8001133D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_5_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 6 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_6_RP3_REG_P1_4
Address	8001133E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_6_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 7 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_7_RP3_REG_P1_4
Address	8001133F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_7_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 8 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_8_RP3_REG_P1_4
Address	800113400301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_8_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 9 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_9_RP3_REG_P1_4
Address	800113410301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_9_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 10 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_10_RP3_REG_P1_4
Address	800113420301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_10_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 11 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_11_RP3_REG_P1_4
Address	800113430301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_11_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 12 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_12_RP3_REG_P1_4
Address	800113440301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_12_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 13 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_13_RP3_REG_P1_4
Address	800113450301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_13_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 14 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_14_RP3_REG_P1_4
Address	800113460301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_14_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 15 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_15_RP3_REG_P1_4
Address	800113470301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_15_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	*DP18 Write Delay Value 16 RP3*
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_16_RP3_REG_P1_4
Address	800113480301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_16_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 18 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_18_RP3_REG_P1_4
Address	8001134A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_18_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 20 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_20_RP3_REG_P1_4
Address	8001134C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_20_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Write Delay Value 22 RP3***
Mnemonic	DPHY23.DP18_WR_DELAY_VALUE_22_RP3_REG_P1_4
Address	8001134E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:57	RW	DP18_4_WR_DELAY_VALUE_22_RP3_REG_P1_DP18_4_WR_DELAYG: Write Delay for MEMINTD{0-23}B pin. This value can be written via the programming interface, or determined by the write eye centering algorithm. This value is used to determine the final write phase rotator value for the given DP18 pin. The valid range of values for this field is 0 to '1FF'h, which represents WR_DELAY128 memory clock cycles of delay.
58:63	RO	constant=0b000000

Register Name	***DP18 Read Delay Value 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY0_RANK_PAIR3_P1_4
Address	800113500301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY0_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY1_RANK_PAIR3_P1_4
Address	800113510301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY1_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY2_RANK_PAIR3_P1_4
Address	800113520301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY2_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY3_RANK_PAIR3_P1_4
Address	800113530301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY3_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY4_RANK_PAIR3_P1_4
Address	800113540301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY4_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY5_RANK_PAIR3_P1_4
Address	800113550301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY5_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY6_RANK_PAIR3_P1_4
Address	800113560301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY6_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Read Delay Value 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_DELAY7_RANK_PAIR3_P1_4
Address	800113570301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:54	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P1_DP18_4_RD_DELAY6: Read Delay for MEMINTD{{0-11}*2}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm that modifies this field sets the corresponding disable bit in the registers described in and, this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
55	RO	constant=0b0
56:62	RW	DDRPHY_DP18_4_READ_DELAY7_RANK_PAIR3_P1_DP18_4_RD_DELAY7: Read Delay for MEMINTD{{0-11}*2+1}B pin. This value can be written via the programming interface, or determined by the read centering algorithm. This value is used to determine the final read phase rotator value for the given DP18 pin. To meet the power requirements of the analog circuits, the valid range for values of this field is 0 to '2F'h. If a calibration algorithm which modifies this field sets the corresponding disable bit in the registers described in and, then this field must be set to the reset value if it exceeds the maximum allowable value via a register write.
63	RO	constant=0b0

Register Name	***DP18 Initial DQS Alignment 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_4
Address	8001135C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN0_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Initial DQS Alignment 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_4
Address	8001135D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:48	RO	constant=0b000000000000000000000000000000000000000000000000
49:55	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N0: Initial DQSClk rotator value for pins MEMINTD00B-MEMINTD03B, MEMINTD16B-MEMINTD17B in register 0 and MEMINTD08B- MEMINGTD11B, MEMINTD20B-MEMINTD21B in register 1. Updated by hardware.
56	RO	constant=0b0
57:63	RO	DDRPHY_DP18_4_INITIAL_DQS_ALIGN1_RANK_PAIR3_P1_DP18_4_INITIAL_DQS_ROT_N1: Initial DQSClk rotator value for pins MEMINTD04B-MEMINTD07B, MEMINTD18B-MEMINTD19B in register 0 and MEMINTD12B- MEMINGTD15B, MEMINTD22B-MEMINTD23B in register 1. Updated by hardware.

Register Name	***DP18 Read Eye Size 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE0_RANK_PAIR3_P1_4
Address	800113600301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Bits	SCOM	Field Mnemonic: Description
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE0_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE1_RANK_PAIR3_P1_4
Address	800113610301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE1_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 2 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE2_RANK_PAIR3_P1_4
Address	800113620301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE2_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 3 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE3_RANK_PAIR3_P1_4
Address	800113630301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE3_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 4 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE4_RANK_PAIR3_P1_4
Address	800113640301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b0000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE4_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 5 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE5_RANK_PAIR3_P1_4
Address	800113650301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE5_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 6 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE6_RANK_PAIR3_P1_4
Address	800113660301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE6_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 7 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE7_RANK_PAIR3_P1_4
Address	800113670301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE7_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 8 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE8_RANK_PAIR3_P1_4
Address	800113680301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE8_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 9 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE9_RANK_PAIR3_P1_4
Address	800113690301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE9_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 10 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE10_RANK_PAIR3_P1_4
Address	8001136A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00

Bits	SCOM	Field Mnemonic: Description
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE10_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Read Eye Size 11 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_READ_EYE_SIZE11_RANK_PAIR3_P1_4
Address	8001136B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:49	RO	constant=0b00000000000000000000000000000000000000000000000000
50:55	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE6: Read Eye Size for MEMINTD{{0-11}*2}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field in the described in the register in, determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.
56:57	RO	constant=0b00
58:63	RWX	DDRPHY_DP18_4_READ_EYE_SIZE11_RANK_PAIR3_P1_DP18_4_RD_EYE_SIZE7: Read Eye Size for MEMINTD{{0-11}*2+1}B pin. The encoded binary number in this field is the number of DQS strobe phase rotator steps which captured valid data during the read centering calibration. This value is the size of the total eye in phase rotator steps. This value can be written via the programming interface, or determined by the read centering algorithm. This value, in addition to the corresponding RD_DELAY field determines the left right and middle of the read data eye. When this value is an even number, the larger half of the eye is to the right of the Read Delay Value.

Register Name	***DP18 Data Bit Disable 0 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE0_RP3_P1_4
Address	8001137C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE0_RP3_P1_DP18_4_DATA_BIT_DISABLE_0_15: '1'b Indicates that the DP18 bit is disabled and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled. Bit 0 controls MEMINTD00B(n) Bit 1 controls MEMINTD01B(n) Bit 2 controls MEMINTD02B(n) ... Bit 15 controls MEMINTD15B(n) where n is the DP18 Instance Number.

Register Name	***DP18 Data Bit Disable 1 RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DATA_BIT_DISABLE1_RP3_P1_4
Address	8001137D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_DP18_4_DATA_BIT_DISABLE1_RP3_P1_DP18_4_DATA_BIT_DISABLE_16_23: '1'b Indicates the DP18 bit is disabled, and does not participate in any calibration steps. '0'b Indicates the DP18 bit is not disabled Bit 0 controls MEMINTD16B(n) Bit 1 controls MEMINTD17B(n) Bit 2 controls MEMINTD18B(n) ... Bit 7 controls MEMINTD23B(n) where n is the DP18 Instance Number.
56:63	RO	constant=0b00000000

Register Name	***DP18 Write DQ Offset Value RP3***
Mnemonic	DPHY23.DDRPHY_DP18_DQ_WR_OFFSET_RP3_P1_4
Address	8001137E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N0: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD00B(n) MEMINTD01B(n) MEMINTD02B(n) MEMINTD03B(n) MEMINTD16B(n) MEMINTD17B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
52:55	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N1: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD04B(n) MEMINTD05B(n) MEMINTD06B(n) MEMINTD07B(n) MEMINTD18B(n) MEMINTD19B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
56:59	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N2: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD08B(n) MEMINTD09B(n) MEMINTD10B(n) MEMINTD11B(n) MEMINTD20B(n) MEMINTD21B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.
60:63	RW	DDRPHY_DP18_4_DQ_WR_OFFSET_RP3_P1_DP18_4_DQ_WR_OFFSET_N3: 4 most significant bits of a 5 bit value. The 5 bit value is a two compliment number added to the center phase rotator value determined by Write Centering calibration algorithm. This value is added to the center value by the Write Centering calibration algorithm as the final step of write centering pins: MEMINTD12B(n) MEMINTD13B(n) MEMINTD14B(n) MEMINTD15B(n) MEMINTD22B(n) MEMINTD23B(n) When the pins are configured as data pins. The least significant bit of the 5 bit value is always '0'b.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR0
Address	800140000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR0_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR0_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR0
Address	800140010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR0_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P1_ADR0
Address	800140040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P1_ADR0_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P1_ADR0_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P1_ADR0
Address	800140050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P1_ADR0_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P1_ADR0_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P1_ADR0
Address	800140060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY2_P1_ADR0_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P1_ADR0_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P1_ADR0
Address	800140070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P1_ADR0_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P1_ADR0_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P1_ADR0
Address	800140080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P1_ADR0_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P1_ADR0_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P1_ADR0
Address	800140090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P1_ADR0_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P1_ADR0_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P1_ADR0
Address	8001400A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY6_P1_ADR0_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P1_ADR0_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P1_ADR0
Address	8001400B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY7_P1_ADR0_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P1_ADR0_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR0
Address	8001400C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR0_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR0
Address	8001401A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR0_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR0
Address	800140200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR0_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR0
Address	800140210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR0_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0
Address	8001402A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR0_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0
Address	8001402B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR0_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR0
Address	8001402C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR0_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR0_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR1
Address	800144000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR1_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_01_BIT_ENABLE_P1_ADR1_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR1
Address	800144010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_01_DIFFPAIR_ENABLE_P1_ADR1_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P1_ADR1
Address	800144040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY0_P1_ADR1_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY0_P1_ADR1_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P1_ADR1
Address	800144050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY1_P1_ADR1_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY1_P1_ADR1_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P1_ADR1
Address	800144060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY2_P1_ADR1_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY2_P1_ADR1_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P1_ADR1
Address	800144070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY3_P1_ADR1_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY3_P1_ADR1_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P1_ADR1
Address	800144080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY4_P1_ADR1_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY4_P1_ADR1_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P1_ADR1
Address	800144090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY5_P1_ADR1_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY5_P1_ADR1_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P1_ADR1
Address	8001440A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_01_DELAY6_P1_ADR1_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY6_P1_ADR1_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P1_ADR1
Address	8001440B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_01_DELAY7_P1_ADR1_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_01_DELAY7_P1_ADR1_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR1
Address	8001440C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_01_DFT_WRAP_STATUS_CONTROL_P1_ADR1_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR1
Address	8001441A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_P1_ADR1_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR1
Address	800144200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP0_P1_ADR1_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR1
Address	800144210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_01_IO_FET_SLICE_EN_MAP1_P1_ADR1_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1
Address	8001442A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP0_P1_ADR1_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1
Address	8001442B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_01_IO_SLEW_CTL_VALUE_MAP1_P1_ADR1_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR1
Address	8001442C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR1_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_01_POWERDOWN_2_P1_ADR1_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR2
Address	800148000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR2_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR2_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR2
Address	800148010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR2_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P1_ADR2
Address	800148040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P1_ADR2_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P1_ADR2_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P1_ADR2
Address	800148050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P1_ADR2_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P1_ADR2_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P1_ADR2
Address	800148060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY2_P1_ADR2_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P1_ADR2_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P1_ADR2
Address	800148070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P1_ADR2_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P1_ADR2_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P1_ADR2
Address	800148080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P1_ADR2_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P1_ADR2_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P1_ADR2
Address	800148090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P1_ADR2_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P1_ADR2_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P1_ADR2
Address	8001480A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY6_P1_ADR2_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P1_ADR2_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P1_ADR2
Address	8001480B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY7_P1_ADR2_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P1_ADR2_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR2
Address	8001480C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR2_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR2
Address	8001481A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR2_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR2
Address	800148200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR2_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR2
Address	800148210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR2_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2
Address	8001482A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR2_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2
Address	8001482B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR2_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR2
Address	8001482C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR2_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR2_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	***ADR Bit Enable***
Mnemonic	DPHY23.DDRPHY_ADR_BIT_ENABLE_P1_ADR3
Address	80014C000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR3_BIT_ENABLE_0_11: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 0 controls MEMINTC00O(n) Bit 1 controls MEMINTC01O(n) Bit 2 controls MEMINTC02O(n) ... Bit 11 controls MEMINTC11O(n) where n is the ADR Instance Number.
60:63	RW	DDRPHY_ADR_23_BIT_ENABLE_P1_ADR3_BIT_ENABLE_12_15: ADR16: '1'b Indicates the ADR bit is enabled, and is used for sending clocks or control (command, address, and so on) to the memory device. '0'b Indicates the ADR bit is not used and not enabled. Bit 12 controls MEMINTC12O(n) Bit 13 controls MEMINTC13O(n) Bit 14 controls MEMINTC14O(n) Bit 15 controls MEMINTC15O(n) where n is the ADR Instance Number. ADR12: Reserved.

Register Name	***ADR Differential Pair Enable***
Mnemonic	DPHY23.DDRPHY_ADR_DIFFPAIR_ENABLE_P1_ADR3
Address	80014C010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR0_ADR1: Value of 0 programs the ADR1216 analog pins ADR01S0 = 1 and ADR01S1 = 0 providing lane 0 with clocks from phase rotator 0 and lane 1 with clocks from phase rotator 1 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR01S0 = 0 and ADR01S1 = 1 providing both lanes with a common clock to minimize skew between lane 0 and lane 1 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
49	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR2_ADR3: Value of 0 programs the ADR1216 analog pins ADR03S0 = 1 and ADR03S1 = 0 providing lane 2 with clocks from phase rotator 2 and lane 3 with clocks from phase rotator 3 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR03S0 = 0 and ADR03S1 = 1 providing both lanes with a common clock to minimize skew between lane 2 and lane 3 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
50	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR4_ADR5: Value of 0 programs the ADR1216 analog pins ADR05S0 = 1 and ADR05S1 = 0 providing lane 4 with clocks from phase rotator 4 and lane 5 with clocks from phase rotator 5 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR05S0 = 0 and ADR05S1 = 1 providing both lanes with a common clock to minimize skew between lane 4 and lane 5 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
51	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR6_ADR7: Value of 0 programs the ADR1216 analog pins ADR07S0 = 1 and ADR07S1 = 0 providing lane 6 with clocks from phase rotator 6 and lane 7 with clocks from phase rotator 7 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR07S0 = 0 and ADR07S1 = 1 providing both lanes with a common clock to minimize skew between lane 6 and lane 7 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).

Bits	SCOM	Field Mnemonic: Description
52	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR8_ADR9: Value of 0 programs the ADR1216 analog pins ADR09S0 = 1 and ADR09S1 = 0 providing lane 8 with clocks from phase rotator 8 and lane 9 with clocks from phase rotator 9 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR09S0 = 0 and ADR09S1 = 1 providing both lanes with a common clock to minimize skew between lane 8 and lane 9 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
53	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR10_ADR11: Value of 0 programs the ADR1216 analog pins ADR11S0 = 1 and ADR11S1 = 0 providing lane 10 with clocks from phase rotator 10 and lane 11 with clocks from phase rotator 11 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR11S0 = 0 and ADR11S1 = 1 providing both lanes with a common clock to minimize skew between lane 10 and lane 11 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator).
54	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR12_ADR13: ADR16: Value of 0 programs the ADR1216 analog pins ADR13S0 = 1 and ADR13S1 = 0 providing lane 12 with clocks from phase rotator 12 and lane 13 with clocks from phase rotator 13 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR13S0 = 0 and ADR13S1 = 1 providing both lanes with a common clock to minimize skew between lane 12 and lane 13 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
55	RW	DDRPHY_ADR_23_DIFFPAIR_ENABLE_P1_ADR3_DI_ADR14_ADR15: ADR16: Value of 0 programs the ADR1216 analog pins ADR15S0 = 1 and ADR15S1 = 0 providing lane 14 with clocks from phase rotator 14 and lane 15 with clocks from phase rotator 15 (default addresscommand generation mode) Value of 1 programs the ADR1216 analog pins ADR15S0 = 0 and ADR15S1 = 1 providing both lanes with a common clock to minimize skew between lane 14 and lane 15 (memory clock mode, differential pair of lanes both receive clock from a common phase rotator). ADR12: Reserved.
56:63	RW	

Register Name	***ADR Delay Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY0_P1_ADR3
Address	80014C040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY0_P1_ADR3_ADR_DELAY0: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY0_P1_ADR3_ADR_DELAY1: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY1_P1_ADR3
Address	80014C050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY1_P1_ADR3_ADR_DELAY2: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY1_P1_ADR3_ADR_DELAY3: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 2***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY2_P1_ADR3
Address	80014C060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY2_P1_ADR3_ADR_DELAY4: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY2_P1_ADR3_ADR_DELAY5: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	***ADR Delay Value 3***
Mnemonic	DPHY23.DDRPHY_ADR_DELAY3_P1_ADR3
Address	80014C070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY3_P1_ADR3_ADR_DELAY6: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY3_P1_ADR3_ADR_DELAY7: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 4*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY4_P1_ADR3
Address	80014C080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY4_P1_ADR3_ADR_DELAY8: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY4_P1_ADR3_ADR_DELAY9: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 5*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY5_P1_ADR3
Address	80014C090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY5_P1_ADR3_ADR_DELAY10: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY5_P1_ADR3_ADR_DELAY11: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 6*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY6_P1_ADR3
Address	80014C0A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_23_DELAY6_P1_ADR3_ADR_DELAY12: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY6_P1_ADR3_ADR_DELAY13: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR Delay Value 7*
Mnemonic	DPHY23.DDRPHY_ADR_DELAY7_P1_ADR3
Address	80014C0B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_23_DELAY7_P1_ADR3_ADR_DELAY14: Output Delay for MEMINTC{{0-7}*2}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.
56	RW	
57:63	RW	DDRPHY_ADR_23_DELAY7_P1_ADR3_ADR_DELAY15: Output Delay for MEMINTC{{0-7}*2+1}O pin. This value can be written via the programming interface. This value is used to determine the final phase rotator value for the given ADR pin.

Register Name	*ADR DFT Wrap Status And Control*
Mnemonic	DPHY23.DDRPHY_ADR_DFT_WRAP_STATUS_CONTROL_P1_ADR3
Address	80014C0C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	ROX	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_LANE_PAIR_FAIL: For PRBS7 error detection in the mclk domain: Bit 0 represents the miscompare detect for wrap0 and wrap1. Bit 1 represents the miscompare detect for wrap2 and wrap3. Bit 2 represents the miscompare detect for wrap4 and wrap5. Bit 3 represents the miscompare detect for wrap6 and wrap7. Bit 4 represents the miscompare detect for wrap8 and wrap9. Bit 5 represents the miscompare detect for wrap10 and wrap11. Bit 6 represents the miscompare detect for wrap12 and wrap13. Bit 7 represents the miscompare detect for wrap14 and wrap15.
56	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_DATA_EN: When high, this bit selects macrotest data. Otherwise, functional mode is used.

Bits	SCOM	Field Mnemonic: Description
57:58	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_MODE: These bits are a multiplex control selector between prbs data and clock wrap swap. For Generator Multiplexing: -- For APIN-0, 4, 8, 12: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-1, 5, 9, 13: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive the clock -- 11: APINs receive prbs data -- For APIN-2, 6, 10, 14: -- 00: APINs receive prbs data -- 01: APINs receive the clock -- For APIN-3, 7, 11, 15: -- 00: APINs receive the clock -- 01: APINs receive prbs data -- 10: APINs receive prbs data -- 11: APINs receive the clock For checker multiplexing: -- For WRAP-0, 4, 8, 12: -- The following example is for the WRAP0 multiplexer. -- 00: The checker receives prbs7 data from WRAP0 -- 01: The checker receives prbs7 data from WRAP1 -- 10: The checker receives prbs7 data from WRAP3 -- 11: The checker receives prbs7 data from WRAP1 -- For WRAP-1, 5, 9, 13: -- The following example is for the WRAP1 multiplexer. -- 00: The checker receives clk from WRAP1 -- 01: Checker receives clk from WRAP0 -- 10: Checker receives clk from WRAP1 -- 11: Checker receives clk from WRAP3 -- For WRAP-2, 6, 10, 14: -- The following example is for the WRAP2 multiplexer. -- 00: The checker receives prbs7 data from WRAP2 -- 01: The checker receives prbs7 data from WRAP3 -- For WRAP-3, 7, 11, 15: -- The following example is for the WRAP3 multiplexer. -- 00: The checker receives clk from WRAP3 -- 01: Checker receives clk from WRAP2
59	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_4TO1_MODE: When active, the prbs generates a 4-bit output every cycle. Otherwise, it outputs two bits. This signal is in the mclk domain.
60	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_RESET: Reset. This signal is in the mclk domain.
61	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_GEN_EN: Pattern generator enable, mclk domain. This signal should be active before enabling the check_enable_i; which is 8 cycles for loading the checker plus the latency between the generator and the wrap through APIN and ANA16.
62	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_CLEAR_ERROR: Clear error bits, mclk domain. The generator should be active before clr_error_i, and the macrotest_mode_i should be selecting WRAP clocks to all the corresponding checkers latches.
63	RW	DDRPHY_ADR_23_DFT_WRAP_STATUS_CONTROL_P1_ADR3_ADR_TEST_CHECK_EN: Enable the pattern checker, mclk domain. When active, the checker performs a prbs7 sequence check on the corresponding WRAP channel.

Register Name	***ADR I/O Slew Control Value***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_P1_ADR3
Address	80014C1A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL0: Slew rate control vector. Bits 8:11 are connected to SxSLEWCTL{0-3} on the analog core. This field provides programmability of the slew rate for data drivers. The lowest dVdT settings does not support the maximum frequency of operation. The change in slew Vns is dependent on process corner and impedance setting. At 24 Ohms, Nominal process 0000 -------- 3.61 Vns average 0001 -------- 4.33 Vns average 0010 -------- 5.41Vns average 0011 -------- 6.69 Vns average 0100 -------- 8.11Vns average 0101 ---------8.58 Vns average 0110 - 1111 = approximately 180 mV increment per step.
52:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL1: Slew rate control vector. Values same as SLEW_CTL0.
56:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL2: Slew rate control vector. Values same as SLEW_CTL0.
60:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_P1_ADR3_SLEW_CTL3: Slew rate control vector. Values same as SLEW_CTL0.

Register Name	*ADR I/O FET Slice Enable Map 0*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP0_P1_ADR3
Address	80014C200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL0: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL1: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL2: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL3: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL4: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL5: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL6: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP0_P1_ADR3_SLICE_SEL7: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	*ADR I/O FET Slice Enable Map 1*
Mnemonic	DPHY23.DDRPHY_ADR_IO_FET_SLICE_EN_MAP1_P1_ADR3
Address	80014C210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:49	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL8: Select one of 4 impedance values to be used for MEMINTC00O (ADR IO FET Slice Enable Map 0) and MEMINTC08O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
50:51	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL9: Select one of 4 impedance values to be used for MEMINTC01O (ADR IO FET Slice Enable Map 0) and MEMINTC09O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
52:53	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL10: Select one of 4 impedance values to be used for MEMINTC02O (ADR IO FET Slice Enable Map 0) and MEMINTC10O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
54:55	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL11: Select one of 4 impedance values to be used for MEMINTC03O (ADR IO FET Slice Enable Map 0) and MEMINTC11O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
56:57	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL12: Select one of 4 impedance values to be used for MEMINTC04O (ADR IO FET Slice Enable Map 0) and MEMINTC12O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
58:59	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL13: Select one of 4 impedance values to be used for MEMINTC05O (ADR IO FET Slice Enable Map 0) and MEMINTC13O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
60:61	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL14: Select one of 4 impedance values to be used for MEMINTC06O (ADR IO FET Slice Enable Map 0) and MEMINTC14O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance
62:63	RW	DDRPHY_ADR_23_IO_FET_SLICE_EN_MAP1_P1_ADR3_SLICE_SEL15: Select one of 4 impedance values to be used for MEMINTC07O (ADR IO FET Slice Enable Map 0) and MEMINTC15O (ADR IO FET Slice Enable Map 1). '00'b - Use 15 Ohm drive impedance '01'b - Use 20 Ohm drive Impedance '10'b - Use 30 Ohm drive impedance '11'b - Use 40 Ohm drive impedance

Register Name	***ADR IO Slew Control Value Map 0***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3
Address	80014C2A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL0: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL1: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL2: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL3: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL4: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL5: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL6: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP0_P1_ADR3_SLEW_CTL_SEL7: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR IO Slew Control Value Map 1***
Mnemonic	DPHY23.DDRPHY_ADR_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3
Address	80014C2B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:49	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL8: Select one of 4 Slew Control values to be used for MEMINTC00O (ADR IO Slew Control Value Map 0) and MEMINTC08O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
50:51	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL9: Select one of 4 Slew Control values to be used for MEMINTC01O (ADR IO Slew Control Value Map 0) and MEMINTC09O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Bits	SCOM	Field Mnemonic: Description
52:53	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL10: Select one of 4 Slew Control values to be used for MEMINTC02O (ADR IO Slew Control Value Map 0) and MEMINTC10O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
54:55	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL11: Select one of 4 Slew Control values to be used for MEMINTC03O (ADR IO Slew Control Value Map 0) and MEMINTC11O (ADR IO Slew Control Value Map 1). '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
56:57	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL12: Select one of 4 Slew Control values to be used for MEMINTC04O (ADR IO Slew Control Value Map 0) and MEMINTC12O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
58:59	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL13: Select one of 4 Slew Control values to be used for MEMINTC05O (ADR IO Slew Control Value Map 0) and MEMINTC13O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
60:61	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL14: Select one of 4 Slew Control values to be used for MEMINTC06O (ADR IO Slew Control Value Map 0) and MEMINTC14O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register
62:63	RW	DDRPHY_ADR_23_IO_SLEW_CTL_VALUE_MAP1_P1_ADR3_SLEW_CTL_SEL15: Select one of 4 Slew Control values to be used for MEMINTC07O (ADR IO Slew Control Value Map 0) and MEMINTC15O (ADR16 and ADR IO Slew Control Value Map 1). Reserved - ADR12 and ADR IO Slew Control Value Map 1 Register. '00'b - Use SLEW_CTL0 values in ADR IO Slew Control Value Register '01'b - Use SLEW_CTL1 values in ADR IO Slew Control Value Register '10'b - Use SLEW_CTL2 values in ADR IO Slew Control Value Register '11'b - Use SLEW_CTL3 values in ADR IO Slew Control Value Register

Register Name	***ADR Power Down 2***
Mnemonic	DPHY23.DDRPHY_ADR_POWERDOWN_2_P1_ADR3
Address	80014C2C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:59	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR3_ADR_LANE__0_11_PD: '1'b - When bit 14 of the register is '1'b, MEMINTC{0-11} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{0-11} is at 40 ohms (maximum impedance).
60:63	RW	DDRPHY_ADR_23_POWERDOWN_2_P1_ADR3_ADR_LANE__12_15_PD: ADR16: '1'b - When bit 14 of the register is '1'b, MEMINTC{12-15} drives '0'b at minimum impedance. '0'b - When bit 14 of the register is '1'b, MEMINTC{12-15} is at 40 ohms (maximum impedance). ADR12: Reserved.

Register Name	*ADR PLL/VREG Configuration 0*
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S0
Address	800180300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR0_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	*ADR PLL/VREG Configuration 1*
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S0
Address	800180310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100

Bits	SCOM	Field Mnemonic: Description
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR0_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S0
Address	800180320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)

Bits	SCOM	Field Mnemonic: Description
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in are asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR0_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	***ADR WRClk Phase Rotator Offset Value***
Mnemonic	DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S0
Address	800180330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR0_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	*ADR SysClk Phase Rotator Value*
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S0
Address	800180340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field.
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR0_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	*ADR Output Driver Force And ATEST Control*
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S0
Address	800180350301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_FORCE_EN: Output Force Enable Bit.
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR0_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	*ADR Output Driver Force Value 0*
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S0
Address	800180360301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Output Driver Force Value 1*
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S0
Address	800180370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR0_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Slew Calibration Control***
Mnemonic	DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S0
Address	800180390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR0_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	***ADR PLL/VREG Configuration 0***
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR32S1
Address	800184300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNE_0_2: Current Reference selection bits for charge pump Values: 66_6UA=>0b000 50UA=>0b001 40UA=>0b010 33_33UA=>0b011 28_57UA=>0b100 25UA=>0b101 22_22UA=>0b110 20UA=>0b111
51:53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNECP_0_2: PLL charge pump gain selection bits Values: PLL_CHARGE_PUMP_GAIN_OF_1=>0b000 PLL_CHARGE_PUMP_GAIN_OF_2=>0b001 PLL_CHARGE_PUMP_GAIN_OF_3=>0b010 PLL_CHARGE_PUMP_GAIN_OF_4=>0b011 PLL_CHARGE_PUMP_GAIN_OF_5=>0b100 PLL_CHARGE_PUMP_GAIN_OF_6=>0b101 PLL_CHARGE_PUMP_GAIN_OF_7=>0b110 PLL_CHARGE_PUMP_GAIN_OF_8=>0b111
54:59	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNEF_0_5: These bits are for choosing the optimal R and C of the 2nd order filter.
60:61	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_TUNEVCO_0_1: VCO Frequency selection bits.
62:63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_0_P1_ADR1_PLL_PLLXTR_0_1: Extra pins for later expansion.

Register Name	***ADR PLL/VREG Configuration 1***
Mnemonic	DPHY23.DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR32S1
Address	800184310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNETDIV_0_2: Test divider values selection bits Values: PLLTESTOUT_IS_LOGIC_1=>0b000 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_64=>0b001 PLLTESTOUT_IS_MDIVOUT_DIVIDED_BY_1=>0b010 TEST_DIVIDER_DISABLED_PLLTESTOUT_IS_LOGIC_0=>0b100
51:52	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNEMDIV_0_1: Feedback divider value selectionenable bits Values: FEEDBACK_DIVIDER_IS_1=>0b00 FEEDBACK_DIVIDER_IS_2=>0b01
53	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11

Bits	SCOM	Field Mnemonic: Description
54:55	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_VREG_RANGE_0_1: Select REFAVDD input pin voltage level for voltage regulator internal resistor divider. Values: 1_50V=>0b00 1_35V=>0b01 1_20V=>0b11
56	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_PLL_TUNEATST: Sets the ATST outputs Values: HIZ=>0b00 NFET_INTERNAL=>0b01 PFET_INTERNAL=>0b10 CMFB_INTERAL=>0b11
57:58	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_VREG_VCCTUNE_0_1: VREG tuning bits which selects internal voltage range. Values: 850MV=>0b00 855MV=>0b01 860MV=>0b10 865MV=>0b11
59:62	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_INTERP_SIG_SLEW_0_3: Interpolated Signal Slew Control (PRSTCH pins on ADR16).
63	RW	DDRPHY_ADR_PLL_VREG_CONFIG_1_P1_ADR1_ANALOG_WRAPON: Wrap Data control to attached ADR16(s)ADR12(s)

Register Name	***ADR SysClk Phase Rotator Control***
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR32S1
Address	800184320301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_ENABLE: Enables the SysClk and SysClkQ phase rotators. (SYSCLKPDOWN and SYSQCLKPDOWN inputs to NEOANA32)
49:55	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_ROT_OVERRIDE: This field has a dual purpose: Override Control, and Lock Control. When SYSCLK_ROT_OVERRIDE_EN = '1'b, this field is in Override Control mode. When SYSCLK_ROT_OVERRIDE_EN = '0'b, this field is in Lock Control. For Override Control: System Clock (SysClk) Phase Rotator Override Value. (binary_offset_i[0:6] inputs of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE_EN field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. In this mode, the BB_LOCK field in the register described in is 'reserved'. For Lock Control: Write this field to all zeros unless instructed otherwise by your IBM representative. bit 2: Lock Select. Selects between lock status and sticky lock. '0'b - Selects the current status of the lock. When the dphy_nclk detect has reached alignment between the dphy_nclk and SysClk, the BB_LOCK field in the register described in are asserted. '1'b - Selects the sticky lock to the BB_LOCK field. The sticky lock is controlled by bit 4, sticky lock enable. When the sticky lock is set, it remains set. bit 4: Sticky Lock Enable bit 5:7: '000'b - At most 1 count increment or decrement occurs to indicate lock. '001'b - At most 2 counts increment or decrement occur to indicate lock. '010'b - At most 3 counts increment or decrement occur to indicate lock. '011'b - At most 4 counts increment or decrement occur to indicate lock. '100'b - At most 5 counts increment or decrement occur to indicate lock.

Bits	SCOM	Field Mnemonic: Description
56	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_ROT_OVERRIDE_EN: Enables the use of the SYSCLK_ROT_OVERRIDE register value rather than the internally calculated SYSCLK_ROT value (register 34) when set to 1. (binary_offset_override_i input of the dphy_nclk to SysClk alignment circuit) The value in this field cannot be changed in the same write operation that changes the SYSCLK_ROT_OVERRIDE field. Updates to these two fields must be separated by 4 dphy_nclk clock cycles. Back to back APB write operations to this register provide the required separation. When this bit is written to '0'b and was '1'b, the SYSCLK_ROT value in the register that is described in is reset to zero.
57	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_PHASE_ALIGN_RESET: Reset to dphy_nclk - SysClk Phase Alignment Controller (reset_all_i input of dphy_nclkSysClk alignment logic block) This bit must be asserted after PLL locks, active for at least 5 SysClk Cycles
58	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_PHASE_CNTL_EN: Alignment Enable to dphy_nclk - SysClk Phase Alignment Controller (pr_cntl_enable_i input of dphy_nclkSysClk alignment logic block) when high enables controller. This bit must be asserted low at least 25 SysClk Cycles before SYSCLK_ROT_OVERRIDE_EN goes active if the SYSCLK_ROT_OVERRIDE value is to be used.
59	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_PHASE_DEFAULT_EN: Enables default start up values to be output by the dphy_nclk - SysClk Phase Alignment Controller (xsel_w_fence_i input of dphy_nclkSysClk alignment block) should be asserted during system reset and deasserted coincident with SYSCLK_PHASE_ALIGN_RESET.
60	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_SYSCLK_POS_EDGE_ALIGN: Edge alignment strap to dphy_nclk - SysClk Phase Alignment Controller (pos_edge_alignment_i input of dphy_nclkSysClk alignment logic block) when high enables positive edge alignment between dphy_nclk and SysClk when low enables negative edge alignment between dphy_nclk and SysClk required to be low for ADR (negative edge alignment).
61	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_CONTINUOUS_UPDATE: '1'b - The dphy_nclk - SysClk Phase Alignment Controller runs continuously and thus continuously aligns the dphy_nclk clock to the internal SysClk clock. '0'b - The dphy_nclk - SysClk Phase Alignment Controller will only updated periodically under hardware control when an update will not interfere with the PHY functional operations. (continuous_update_i input of the dphy_nclk to SysClk alignment circuit)
62:63	RW	DDRPHY_ADR_SYSCLK_CNTL_PR_P1_ADR1_CE0DLTVCC: This field must be '00'b for proper functional operation. Bit 14 is connected to the CE0DLTVCCD pin on the analog core. Bit 15 is connected to the CE0DLTVCCA pin on the analog core.

Register Name	*ADR WRClk Phase Rotator Offset Value*
Mnemonic	DPHY23.DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR32S1
Address	800184330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	
49:55	RW	DDRPHY_ADR_MCCLK_WRCLK_PR_STATIC_OFFSET_P1_ADR1_TSYS_WRCLK: Static Value of System Clock (SysClk) Phase Rotator to Write Clock (WrClk) Phase Rotator. For zero delay simulations, or simulations where the delay of the SysClk tree and the WrClk tree are equal: Set this field to '60'h.
56:63	RW	

Register Name	***ADR SysClk Phase Rotator Value***
Mnemonic	DPHY23.DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR32S1
Address	800184340301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_LATE_SAMPLE: Slew late sample. This debug bit represents the value of the late sample. Once this bit is asserted, it will remain asserted until a system reset of SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
49:55	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SYSCLK_ROT: Internally Calculated Value of Memory Controller Clock (MCClk) Phase to SysClock (SysClk) Phase Offset. Used to set the SysClock phase rotator when SYSCLK_ROT_OVERRIDE_EN = 0. See the Register 32 description. (binary_offset_o[0:6] output of dphy_nclkSysClk alignment logic block) These bits reset, but are continually loaded with the dphy_nclk to SysClk alignment circuit calculated value for the SysClk delay, exclusive of reset.
56	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_BB_LOCK: '1'b - The dphy_nclkSysClk Phase Alignment Controller has reached alignment between the dphy_nclk and SysClk as of the last update by the dphy_nclkSysClk Phase Alignment Controller. '0'b - The dphy_nclk and SysClk are not in alignment as of the last update by the dphy_nclkSysClk Phase Alignment Controller. There are two types of locks. Refer to the SYSCLK_ROT_OVERRIDE field.
57	RO	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_EARLY_SAMPLE: Slew early sample. This debug bit represents the value of the early sample. Once this bit is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The value of this bit will be undefined until 4 cycles after the Slew Calibration Enable bit register is set.
58:59	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_DONE_STATUS: Slew calibration Done Status. This field indicates when the slew calibration has completed and the completion status. Once any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The Slew Calibration Algorithm will complete in 1020 dphy_nclk clock cycles '00'b - Not Done. '01'b - Done with errors. '10'b - Done with warnings. '11'b - Done with no errors. The status '01'b indicates slew calibration completed without reaching alignment. The status '10'b indicates slew calibration completed with a slew minimum delay; the calculated SLEW_CNTL value is '1111'b.
60:63	ROX	DDRPHY_ADR_SYSCLK_PR_VALUE_RO_P1_ADR1_SLEW_CNTL: Slew Control value. This field represents the slew control value calculated by the slew calibration algorithm. This calculated slew control value is used for setting the register. If any bit in this field is asserted, it will remain asserted until a system reset or SLEW_CAL_START is detected. The calibration algorithm will never calculate a value of '0000'b as a result of a calibration; however, a value of '0000'b can be set via the override field in register.

Register Name	***ADR Output Driver Force And ATEST Control***
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR32S1
Address	800184350301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_FLUSH: FLUSH control to ANALOG during Manufacturing Macro Test - reserved.
49	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_FORCE_EN: Output Force Enable Bit.

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_TOXDRV_HIBERNATE: Thin ox driver hibernation disable.
51	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL_EN: '1'b - Enable ATEST1 output. '0'b - Disable ATEST1 output.
52:55	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_HS_PROBE_A_SEL: High Speed Probe A Select - reserved.
56:59	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_HS_PROBE_B_SEL: High Speed Probe B Select - reserved.
60	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL0: bit 0 of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
61	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL1: bit 1of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved
62	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL2: bit 2of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.
63	RW	DDRPHY_ADR_OUTPUT_FORCE_ATEST_CNTL_P1_ADR1_ATEST1CTL3: bit 3of ATEST1CTL value used during ATEST Manufacturing Macro Test - reserved.

Register Name	***ADR Output Driver Force Value 0***
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR32S1
Address	800184360301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE0_P1_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	***ADR Output Driver Force Value 1***
Mnemonic	DPHY23.DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR32S1
Address	800184370301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_ADR_OUTPUT_DRIVER_FORCE_VALUE1_P1_ADR1_OUTPUT_DRIVER_FORCE_VALUE: Value to be force out of driver. Bit assignments represent respective lanes under test. Reserved.

Register Name	*ADR Slew Calibration Control*
Mnemonic	DPHY23.DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR32S1
Address	800184390301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_ENABLE: Slew Calibration Enable. This active high bit is used by the slew calibration logic as clock gate and fencing. This bit should be asserted 2000 cycle prior to performing the slew calibration cycle in order to mitigate the delay line history effect, and it must be active while the slew calibration is being performed. This bit must be de-asserted after the slew calibration logic has complete calculating the SLEW_CNTL value.
49	RWX	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_START: Slew Calibration Start. When set, the slew calibration controller will commence a calibration cycle. The SLEW_CAL_ENABLE must be asserted prior to setting this bit. The hardware will clear this bit to '0'b a cycle after it is asserted.
50	RW	
51	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_OVERRIDE_EN: Slew Calibration Offset Override Enable. This bit indicates when to override SLEW_CNTL value with SLEW_CAL_OVERRIDE value.
52:55	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_CAL_OVERRIDE: Slew Calibration Offset Override vector. This field overrides SLEW_CNTL when SLEW_CAL_OVERRIDE_EN is active.
56:58	RW	
59:63	RW	DDRPHY_ADR_SLEW_CAL_CNTL_P1_ADR1_SLEW_TARGET_PR_OFFSET: Slew Target Phase Rotator Offset. This field represents a phase rotator offset.

Register Name	*PC DP18 PLL Lock Status*
Mnemonic	DPHY23.DDRPHY_PC_DP18_PLL_LOCK_STATUS_P1
Address	8001C0000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:62	ROX	DDRPHY_PC_DP18_PLL_LOCK_STATUS_P1_DP18_PLL_LOCK: One bit for each DP18 in the DDR PHY Core. When the core contains less than 15 DP18s, then bits with an index value greater than NUM_DP18 - 1 are reserved. '0'b - PLL in the bit indexed DP18 is not locked. '1'b - PLL in the bit indexed DP18 is locked. When the PHY is configured in TDM Mode, this register reports the PLL Lock Status of all the DP18s in the PHY.
63	RO	constant=0b0

Register Name	*PC AD32S PLL Lock Status*
Mnemonic	DPHY23.DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P1
Address	8001C0010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:49	ROX	DDRPHY_PC_AD32S_PLL_LOCK_STATUS_P1_AD32S_PLL_LOCK: One bit for each ADR Support Block in the DDR PHY Core. When the core contains less than 2 AD32Ss, bits with an index value greater than NUM_AD32S-1 are reserved. '0'b - PLL in the bit indexed AD32S is not locked. '1'b - PLL in the bit indexed AD32S is locked.
50:63	RO	constant=0b00000000000000

Register Name	*PC Rank Pair 0*
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR0_P1
Address	8001C0020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_PRI: Primary Rank of Rank Pair 0 When configured for a protocol that only supports a single rank system, this field must be set to 0.
51	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_PRI_V: Value in the RANK_PAIR0_PRI field is valid
52:54	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_SEC: Secondary Rank of Rank Pair 0
55	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR0_SEC_V: Value in the RANK_PAIR0_SEC field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_PRI: Primary Rank of Rank Pair 1
59	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_PRI_V: Value in the RANK_PAIR1_PRI field is valid. If this bit is set, the RANK_PAIR0_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_SEC: Secondary Rank of Rank Pair 1
63	RW	DDRPHY_PC_RANK_PAIR0_P1_RANK_PAIR1_SEC_V: Value in the RANK_PAIR1_SEC field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set.

Register Name	*PC Rank Pair 1*
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR1_P1
Address	8001C0030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_PRI: Primary Rank of Rank Pair 2
51	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_PRI_V: Value in the RANK_PAIR2_PRI field is valid. If this bit is set, the RANK_PAIR1_PRI_V bit must be set in the register defined in.
52:54	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_SEC: Secondary Rank of Rank Pair 2
55	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR2_SEC_V: Value in the RANK_PAIR2_SEC field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
56:58	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_PRI: Primary Rank of Rank Pair 3

Bits	SCOM	Field Mnemonic: Description
59	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_PRI_V: Value in the RANK_PAIR3_PRI field is valid. If this bit is set, the RANK_PAIR2_PRI_V bit must be set.
60:62	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_SEC: Secondary Rank of Rank Pair 3
63	RW	DDRPHY_PC_RANK_PAIR1_P1_RANK_PAIR3_SEC_V: Value in the RANK_PAIR3_SEC field is valid. If this bit is set, the RANK_PAIR3_PRI_V bit must be set.

Register Name	***PC Periodic Base Counter 0***
Mnemonic	DPHY23.DDRPHY_PC_BASE_CNTR0_P1
Address	8001C0040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_BASE_CNTR0_P1_PERIODIC_BASE_CNTR0: Periodic Base Counter 0. When enabled via PERIODIC_CAL_REQ_EN counter is free running (counts every dphy_nclk clock cycle). When this counter rolls over, it is reloaded with the value {PERIODIC_RELOAD_VALUE0 & '0'} from the register described in.

Register Name	***PC Periodic Reload Value 0***
Mnemonic	DPHY23.DDRPHY_PC_RELOAD_VALUE0_P1
Address	8001C0050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RELOAD_VALUE0_P1_PERIODIC_CAL_REQ_EN: '1'b - Enable Periodic Calibration request generation from the PHY. '0'b - Disable Periodic Calibration request generation from the PHY.
49:63	RW	DDRPHY_PC_RELOAD_VALUE0_P1_PERIODIC_RELOAD_VALUE0: Periodic Reload Value 0. This value is loaded into bits 0 through 14 of the when it rolls over. Bit 15 is always loaded with '0'b when it rolls over. When this field is written to zero and the PERIODIC_CAL_REQ_EN is set to '1'b, exactly one periodic calibration (MEMCTLCPURO) is requested by the DDR PHY core.

Register Name	***PC Periodic Base Counter 1***
Mnemonic	DPHY23.DDRPHY_PC_BASE_CNTR1_P1
Address	8001C0060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	DDRPHY_PC_BASE_CNTR1_P1_PERIODIC_BASE_CNTR1: Periodic Base Counter 1. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over and the FAST_SIM_PER_CNTR bit is not set it is reloaded with the value 'FFFF'h. This register enables the and the every (216 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles. When this counter rolls over and the FAST_SIM_PER_CNTR bit is set it is reloaded with the value '00FF'h. When the FAST_SIM_PER_CNTR bit is set this register enables and the every (28 -1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer*
Mnemonic	DPHY23.DDRPHY_PC_CAL_TIMER_P1
Address	8001C0070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	ROX	DDRPHY_PC_CAL_TIMER_P1_PERIODIC_CAL_TIMER: Periodic Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_TIMER_RELOAD_VALUE from the register described in. This register requests a periodic calibration (MEMCTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set this register requests a periodic calibration (MEMCTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Calibration Timer Reload Value*
Mnemonic	DPHY23.DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1
Address	8001C0080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_CAL_TIMER_RELOAD_VALUE_P1_PERIODIC_TIMER_RELOAD_VALUE: Periodic Reload Value 0. This value is loaded into the when it rolls over. This register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Impedance Calibration Timer*
Mnemonic	DPHY23.DDRPHY_PC_ZCAL_TIMER_P1
Address	8001C0090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	ROX	DDRPHY_PC_ZCAL_TIMER_P1_PERIODIC_ZCAL_TIMER: Periodic Impedance Calibration Timer. This counter is enabled for 1 dphy_nclk clock cycle (1 count) each time the performs one counting sequence. When this counter rolls over, it is reloaded with the value PERIODIC_ZCAL_TIMER_RELOAD_VALUE from the register described in. This register requests a periodic impedance calibration (ZCNTLCPURO) every (216 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles. When the FAST_SIM_PER_CNTR bit is set this register requests a periodic impedance calibration (ZCNTLCPURO) every (28 - 1) x ((PERIODIC_RELOAD_VALUE0 x 2) + 1) x (PERIODIC_ZCAL_TIMER_RELOAD_VALUE - 1) dphy_nclk clock cycles.

Register Name	*PC Periodic Impedance Calibration Timer Reload Value*
Mnemonic	DPHY23.DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1
Address	8001C00A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_ZCAL_TIMER_RELOAD_VALUE_P1_PERIODIC_TIMER_RELOAD_VALUE: Periodic Impedance Calibration Timer Reload Value. This value is loaded into the when it rolls over. The register must be set to a value greater than or equal to 2.

Register Name	*PC Periodic Calibration Configuration*
Mnemonic	DPHY23.DDRPHY_PC_PER_CAL_CONFIG_P1
Address	8001C00B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_ENA_RANK_PAIR: '1'b indicates periodic calibration is enabled '0'b indicates periodic calibration is disabled Bit 0 contains the enable bit for rank pair 0Bit 1 contains the enable bit for rank pair 1Bit 2 contains the enable bit for rank pair 2Bit 3 contains the enable bit for rank pair 3
52	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_ENA_ZCAL: Enables the periodic impedance calibration logic.
53	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_ENA_SYSCLK_ALIGN: Enables the periodic alignment of the internal SysClk with the Memory Controller Clock (dphy_nclkSysClk Alignment).
54	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ENA_PER_READ_CTR: '1'b - Enable the updating of the registers described in during periodic read centering. '0'b - Prevent the updating of the registers described in during periodic read centering.
55	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ENA_PER_RDCLK_ALIGN: '1'b - Enable the updating of the register described in at the conclusion of periodic read centering on a nibble of DQ lanes. '0'b - Prevent the updating of the register described in at the conclusion of periodic read centering on a nibble of DQ lanes.
56	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ENA_PER_DQS_ALIGN: Enables periodic alignment of the DQS (read) strobes from memory to the internally generated DQS strobes (DQS Alignment).
57:58	RWX	DDRPHY_PC_PER_CAL_CONFIG_P1_PER_NEXT_RANK_PAIR: Indicates which rank pair is scheduled for the next periodic calibration operation. This field is updated by the PHY as it sequences through periodic calibrations on each enabled rank pair. This field must equal one of the rank pair numbers enabled in the PER_ENA_RANK_PAIR field when at least one rank pair is enabled in the PER_ENA_RANK_PAIR field.

Bits	SCOM	Field Mnemonic: Description
59	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_FAST_SIM_PER_CNTR: This bit must be '0'b in hardware. This bit is a method for behavioral simulations to reduce the time between periodic calibrations. '1'b causes the register described in to roll over to '00FF'h. '0'b has no effect on the behavior of the register described in.
60	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_START_INIT_CAL: When this bit is written to '1'b, the DDR PHY initiates an initial calibration for all ranks enabled in the register defined in. When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
61	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_START_PER_CAL: When this bit is written to '1'b, the DDR PHY initiates a single periodic calibration (equivalent to a periodic timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
62	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ABORT_ON_ERR_EN: Periodic Calibration Abort on Error Enable. '1'b - Enable the detection of the pc_errn_in. '0'b - Disable the detection of the pc_errn_in.
63	RW	DDRPHY_PC_PER_CAL_CONFIG_P1_ZCAL_UPDATE_MODE: Reserved. See PC Config 0 ZCAL_NOT_CONT bit.

Register Name	***PC Configuration 0***
Mnemonic	DPHY23.DDRPHY_PC_CONFIG0_P1
Address	8001C00C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG0_P1_PROTOCOL: Values: DDR3=>0b0000 DDR4=>0b0001 RLDRAM2_CIO=>0b0010
52	RW	DDRPHY_PC_CONFIG0_P1_DATA_MUX4_1MODE: Data Multiplexer Mode 4:1 Enable. '0'b - Data Multiplexer Mode is 2:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) is two times as wide as the data and control signals (pins) on the Memory Interface (MEMINT) Interface. '1'b - Data Multiplexer Mode is 4:1. The Memory Controller Interface Clock, MEMCTLCLKI, frequency is equal to one half of the Memory Device Clock, MEMINTCLKO, frequency. Data and control signals (pins) on the Memory Controller Interface (MEMCTL Interface) are four times as wide as the data and control signals (pins) on the Memory Interface (MEMINT Interface).
53	RW	DDRPHY_PC_CONFIG0_P1_SPAM_EN: '1'b - The PC only snoops read and write commands for primary ranks of each rank pair (that is, reads and writes to secondary ranks are ignored). '0'b - Split Access Mode is not enabled.
54	RW	DDRPHY_PC_CONFIG0_P1_DDR4_CMD_SIG_REDUCTION: Values: DDR3=>0b0 DDR4=>0b1
55	RW	DDRPHY_PC_CONFIG0_P1_SYSCLK_2X_MEMINTCLKO: Always write this bit to '0'b. This function is not supported. '0'b - The internal SysClk frequency equals the MEMINTCLKO (memory interface clock) frequency. '1'b - The internal SysClk frequency is 2* the MEMINTCLKO (memory interface clock) frequency. Support of this function requires this register to be written during the reset sequence when the PLL values are configured.
56	RW	DDRPHY_PC_CONFIG0_P1_RANK_OVERRIDE: Rank Override Mode '0'b - The DDR PHY uses the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface to determine the rank pair and hence the configuration registers for each read or write command. '1'b - The DDR PHY uses the rank number provided in the RANK_OVERRIDE_VALUE field of this register to determine the rank pair and hence the configuration registers for all readwrite commands regardless of the rank number (chip select) provided by the Memory Controller on the MEMCTL Interface. When this bit is '1'b, the following assumptions/restrictions apply:

Bits	SCOM	Field Mnemonic: Description
57:59	RW	DDRPHY_PC_CONFIG0_P1_RANK_OVERRIDE_VALUE: Rank Override Value
60	RW	DDRPHY_PC_CONFIG0_P1_LOW_LATENCY: '1'b - Force Early Read Start Mode (ERS Mode) off. '0'b - ERS Mode on/off determined by CL value. When CL = 5 or 6, ERS Mode is automatically off. Otherwise, ERS Mode is automatically on.
61	RW	
62	RW	DDRPHY_PC_CONFIG0_P1_DDR4_VLEVEL_BANK_GROUP: In DDR4: '1'b - enable Voltage Level and Bank Group Arch(DDR4 ballot 1716.23). '0'b - disable Voltage Level and Bank Group Arch. For all other protocols, this bit must be '0'b.
63	RW	DDRPHY_PC_CONFIG0_P1_ZCAL_NOT_CONT: '1'b - IO PVT values are only updated when an internal ZQ cal is requested. '0'b - IO PVT values are updated continuously.

Register Name	*PC Configuration 1*
Mnemonic	DPHY23.DDRPHY_PC_CONFIG1_P1
Address	8001C00D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_CONFIG1_P1_WRITE_LATENCY_OFFSET: Write Latency Offset (WLO) is used to adjust the delay through the internal write command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipeline latches are added. This value is twos compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path.
52:55	RW	DDRPHY_PC_CONFIG1_P1_READ_LATENCY_OFFSET: Read Latency Offset (RLO) is used to adjust the delay through the internal read command FIFO. This might be necessary to accommodate additional pipelining latches in the command path. For example, RDIMM support requires this field to be set to 1 when no other additional pipelining latches are added. This value is two's compliment, with a range of '-8'd to '7'd memory clock cycles. If pipeline stages are added in the DDR PHY, the number of pipeline stages in the addrcmd path must equal the number of pipeline states in the data path. The value for this field must be: RLO less than equal min{RoundDown(System_Delay)} System_Delay and min{RoundDown(System_Delay)} is defined in the GLOBAL_PHY_OFFSET field description.
56	RW	DDRPHY_PC_CONFIG1_P1_MEMCTL_CIC_FAST: '0'b - memctl_cic_o is deasserted ('0'b) in response to memctl_cis_i being asserted ('1'b) and remains deasserted until the calibration completes. '1'b - memctl_cic_o is deasserted ('0'b) in response to memctl_cis_i being asserted ('1'b) and is asserted ('1'b) in response to memctl_cis_i being deasserted ('0'b).
57	RW	DDRPHY_PC_CONFIG1_P1_MEMCTL_CTRN_IGNORE: '0'b - DDR PHY responds to the memctl_ctrn_i input. '1'b - DDR PHY does not respond to the memctl_ctrn_i input. The memctl_ctrn_i input value is a 'don't care'.
58	RW	DDRPHY_PC_CONFIG1_P1_DISABLE_MEMCTL_CAL: Reserved. This bit must be '0'b. When set to '1'b, the DFI request ack handshaking is disabled. The DDR PHY does not wait for an ACK. This is a debug aid.
59:61	RW	DDRPHY_PC_CONFIG1_P1_MEMORY_TYPE: '001'b - DDR3 RDIMM '011'b - DDR3 LRDIMM '101'b - DDR4 RDIMM '111'b - DDR4 LRDIMM Other values are reserved.
62	RW	DDRPHY_PC_CONFIG1_P1_DDR4_LATENCY_SW: DDR4 Latency Debug Switch. Should be '1'b for normal operation.
63	RW	DDRPHY_PC_CONFIG1_P1_RETRAIN_PERCAL_SW: Retrain Percal Debug Switch. Affects behavior of memctl_cup_o during periodic read calibrations. '0'b - rank is requested rank and may not be the rank that was executed. '1'b - rank is next rank that requires calibration.

Register Name	*PC Resets*
Mnemonic	DPHY23.DDRPHY_PC_RESETS_P1
Address	8001C00E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RESETS_P1_PLL_RESET: '1'b - Resets the Internal PLLs
49	RW	DDRPHY_PC_RESETS_P1_SYSCLK_RESET: '1'b - Reset all logic in the internal sysclk domain.
50:63	RO	constant=0b00000000000000

Register Name	*PC Periodic Z-Cal Configuration*
Mnemonic	DPHY23.DDRPHY_PC_PER_ZCAL_CONFIG_P1
Address	8001C00F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P1_PER_ZCAL_ENA_RANK: '1'b indicates periodic external impedance calibration is enabled '0'b indicates periodic external impedance calibration is disabled Bit 0 contains the enable bit for rank 0Bit 1 contains the enable bit for rank 1Bit 2 contains the enable bit for rank 2Bit 3 contains the enable bit for rank 3Bit 4 contains the enable bit for rank 4Bit 5 contains the enable bit for rank 5Bit 6 contains the enable bit for rank 6Bit 7 contains the enable bit for rank 7
56:58	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P1_PER_ZCAL_NEXT_RANK: Indicates which rank is scheduled for the next periodic impedance calibration operation. This field is updated by the PHY as it sequences through periodic impedance calibrations on each enabled rank. 000 = rank_0 next rank scheduled to run z cal001 = rank_1 next rank scheduled to run z cal010 = rank_2 next rank scheduled to run z cal011 = rank_3 next rank scheduled to run z cal100 = rank_4 next rank scheduled to run z cal101 = rank_5 next rank scheduled to run z cal110 = rank_6 next rank scheduled to run z cal111 = rank_7 next rank scheduled to run z cal
59	RWX	DDRPHY_PC_PER_ZCAL_CONFIG_P1_START_PER_ZCAL: When this bit is written to '1'b, the DDR PHY initiate a single periodic impedance calibration (equivalent to a periodic z cal timer pop). When this bit is written to '0'b, no action is taken by the DDR PHY. When read, this bit always returns the last value written.
60:63	RO	constant=0b0000

Register Name	*PC Power Down 1*
Mnemonic	DPHY23.DDRPHY_PC_POWERDOWN_1_P1
Address	8001C0100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48	RW	DDRPHY_PC_POWERDOWN_1_P1_MASTER_PD_CNTL: Master Powerdown Control '0'b - DDR port is in functional mode regardless of PDR1 bits {1:15} '1'b - Powerdown status of DDR port is determined by PDR bits {1:15}
49	RW	DDRPHY_PC_POWERDOWN_1_P1_ANALOG_INPUT_STAB2: Analog Input Stabilization #2 (Separate from bit 7 to allow for separation of behavior in PDS3) '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
50	RW	DDRPHY_PC_POWERDOWN_1_P1_EYEDAC_PD: EYEDAC powerdown '0'b - EYEDAC controlled by functional mode register '1'b - EYEDAC powered down
51	RW	DDRPHY_PC_POWERDOWN_1_P1_PHYTOP_CLK_GATE: Reserved.
52	RW	DDRPHY_PC_POWERDOWN_1_P1_EXT_VREF_PD: External VREF Powerdown '0'b - Functional Mode control of External VREF Drivers '1'b - External VREF Drivers Powered Down
53	RW	DDRPHY_PC_POWERDOWN_1_P1_RESET_STAB: RESET# Stabilization '0'b - Functional Mode Control of RESET# PHY IO '1'b - Powerdown Stabilization of RESET# Signals
54	RW	DDRPHY_PC_POWERDOWN_1_P1_ANALOG_OUTPUT_STAB: Analog Output Stabilization '0'b - Functional Mode Control of Analog Outputs '1'b - Analog Outputs Forced to Known Values Immediately on Digital Side of Boundary
55	RW	DDRPHY_PC_POWERDOWN_1_P1_ANALOG_INPUT_STAB1: Analog Input Stabilization #1 '0'b - Functional Mode Control of Address Data Control Inputs to the Analog domain '1'b - Static stabilization of Address Data Control
56	RW	DDRPHY_PC_POWERDOWN_1_P1_SYSCLK_CLK_GATE: Reserved.
57	RW	DDRPHY_PC_POWERDOWN_1_P1_DELAY_LINE_CTL_OVERRIDE: '0'b - DP18 Delay Line Power Control register is read only and is updated by hardware. '1'b - DP18 Delay Line Power Control register is read/write and is not updated by hardware.
58	RW	DDRPHY_PC_POWERDOWN_1_P1_WR_FIFO_STAB: Write FIFO & Logic Circuit Stabilization '0'b - Write FIFO and Logic Circuits under Functional Control '1'b - Write FIFO clock disabled, Flush mode set
59	RW	DDRPHY_PC_POWERDOWN_1_P1_ADR_RX_PD: Reserved.
60:61	RW	DDRPHY_PC_POWERDOWN_1_P1_DP18_RX_PD: DP18 Receiver Powerdown Control '00'b - Functional Mode Control of DP Receivers '01'b - DP Receivers in Standby Mode (RG) '10'b - Reserved. '11'b - DP Receivers in Low Power Mode (RE)
62	RW	DDRPHY_PC_POWERDOWN_1_P1_TX_TRISTATE_CNTL: Driver Tristate Control '0'b - Functional Mode Control of Drivers '1'b - DP18 Drivers in Tristate, ADR Drivers selectively either in Tristate or Pulldown under control of PDR2 For the ADR12 and ADR16 cores, this bit operates in conjunction with the register described in to determine the state of the IO during powerdown.
63	RW	DDRPHY_PC_POWERDOWN_1_P1_VCC_REG_PD: VCC Domain Regulation Powerdown '0'b - Functional Mode: VCC Voltage Regulators are on '1'b - Powerdown Mode: Voltage Regulators powered down, VCC=0v

Register Name	***PC Rank Group***
Mnemonic	DPHY23.DDRPHY_PC_RANK_GROUP_P1
Address	8001C0110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP0_PRI: '1'b - Enable Address Mirroring Rank Pair 0 Primary
49	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP0_SEC: '1'b - Enable Address Mirroring Rank Pair 0 Secondary

Bits	SCOM	Field Mnemonic: Description
50	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP1_PRI: '1'b - Enable Address Mirroring Rank Pair 1 Primary
51	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP1_SEC: '1'b - Enable Address Mirroring Rank Pair 1 Secondary
52	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP2_PRI: '1'b - Enable Address Mirroring Rank Pair 2 Primary
53	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP2_SEC: '1'b - Enable Address Mirroring Rank Pair 2 Secondary
54	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP3_PRI: '1'b - Enable Address Mirroring Rank Pair 3 Primary
55	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_RP3_SEC: '1'b - Enable Address Mirroring Rank Pair 3 Secondary
56:57	RW	DDRPHY_PC_RANK_GROUP_P1_RANK_GROUPING: Reserved.
58	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A3_A4: '1'b - mirror A3 & A4 signals on mirrored ranks.
59	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A5_A6: '1'b - mirror A5 & A6 signals on mirrored ranks.
60	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A7_A8: '1'b - mirror A7 & A8 signals on mirrored ranks.
61	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_A11_A13: '1'b - mirror A11 & A13 signals on mirrored ranks.
62	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_BA0_BA1: '1'b - mirror BA0 & BA1 signals on mirrored ranks.
63	RW	DDRPHY_PC_RANK_GROUP_P1_ADDR_MIRROR_BG0_BG1: '1'b - mirror BG0 & BG1 signals on mirrored ranks.

Register Name	*PC Error Status 0*
Mnemonic	DPHY23.DDRPHY_PC_ERROR_STATUS0_P1
Address	8001C0120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_ERROR_STATUS0_P1_RC_ERROR: '1'b - Error in Read Control logic.
49	ROX	DDRPHY_PC_ERROR_STATUS0_P1_WC_ERROR: '1'b - Error in Write Control logic.
50	ROX	DDRPHY_PC_ERROR_STATUS0_P1_SEQ_ERROR: '1'b - Error in Sequencer Control logic.
51	ROX	DDRPHY_PC_ERROR_STATUS0_P1_CC_ERROR: Reserved.
52	ROX	DDRPHY_PC_ERROR_STATUS0_P1_APB_ERROR: '1'b - Error in Register interface logic.
53	ROX	DDRPHY_PC_ERROR_STATUS0_P1_PC_ERROR: '1'b - Error in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	*PC Error Mask 0*
Mnemonic	DPHY23.DDRPHY_PC_ERROR_MASK0_P1
Address	8001C0130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_ERROR_MASK0_P1_RC_ERROR_MASK: '1'b - Mask errors in Read Control logic.
49	RW	DDRPHY_PC_ERROR_MASK0_P1_WC_ERROR_MASK: '1'b - Mask errors in Write Control logic.
50	RW	DDRPHY_PC_ERROR_MASK0_P1_SEQ_ERROR_MASK: '1'b - Mask errors in Sequencer Control logic.
51	RW	DDRPHY_PC_ERROR_MASK0_P1_CC_ERROR_MASK: Reserved.
52	RW	DDRPHY_PC_ERROR_MASK0_P1_APB_ERROR_MASK: '1'b - Mask errors in Register Interface logic.
53	RW	DDRPHY_PC_ERROR_MASK0_P1_PC_ERROR_MASK: '1'b - Mask errors in PHY Control logic.
54:63	RO	constant=0b0000000000

Register Name	*PC IO PVT N/P FET Driver Control*
Mnemonic	DPHY23.DDRPHY_PC_IO_PVT_FET_CONTROL_P1
Address	8001C0140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_PVTP: PFET Driver PVTP value to send to all output drivers when PVT_OVERRIDE is set.
53:57	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_PVTN: NFET Driver PVTN value to send to all output drivers when PVT_OVERRIDE is set.
58	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_PVT_OVERRIDE: '1'b - All drivers are updated with the PVTP and PVTN values in this register immediately. '0'b - All drivers are updated with the PVTP and PVTN values from the impedance calibration state machine.
59	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_ENABLE_ZCAL: '1'b - Enable Impedance Controller. '0'b - Disable Impedance Controller.
60	RW	DDRPHY_PC_IO_PVT_FET_CONTROL_P1_RESET_ZCAL: Reset Impedance Controller. The value of this field is driven to the zcntl_reset_o output for optional connection to the reset of an Impedance Controller.
61:63	RO	constant=0b000

Register Name	*PC VREF Driver Control*
Mnemonic	DPHY23.DDRPHY_PC_VREF_DRV_CONTROL_P1
Address	8001C0150301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ0DSGN: VREF sign bit enable. This value is driven to the vrefdq0_dsign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
49:52	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ0D: VREF bit enables. This value is driven to the vrefdq0_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
53	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ1DSGN: VREF sign bit enable. This value is driven to the vrefdq1_dsign output for optional connection to the DSIGN pin of a ODDR3VREFDRV IO cell.
54:57	RW	DDRPHY_PC_VREF_DRV_CONTROL_P1_VREFDQ1D: VREF bit enables. This value is driven to the vrefdq1_d(0:3) output for optional connection to the D0-D3 pins of a ODDR3VREFDRV IO cell.
58:63	RO	constant=0b000000

Register Name	*PC Initial Calibration Config0*
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_CONFIG0_P1
Address	8001C0160301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_WR_LEVEL: Enable Write Leveling during initial calibration
49	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_INITIAL_PAT_WR: Enable Initial Pattern Write during initial calibration. This bit must be set when performing Read Centering or Write Centering on memory devices that do not generate an MPR pattern. This bit must be set when performing Custom Read Centering or Custom Write Centering. If Custom Read Centering or Custom Write Centering was performed, an Initial Pattern Write of '5555' hex, the reset value of the SEQ Read/Write Data0-1 registers, must be performed before any periodic calibration routines are performed.
50	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_DQS_ALIGN: Enable DQS (read) alignment during initial calibration.
51	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_RDCLK_ALIGN: Enable the alignment of the internal SysClk to the Read clock during initial calibration. This calibration step requires the DQS (read) Alignment calibration step to have been performed.
52	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_READ_CTR: Enable Read Centering during initial calibration. This calibration step requires the SysClk to Read Clock alignment to have been performed.
53	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_WRITE_CTR: Enable Write Centering during initial calibration. This calibration step requires the Read Centering calibration step to have been performed.
54	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_INITIAL_COARSE_WR: Enable Initial Coarse Pattern Write during initial calibration. This calibration step requires the Write Centering calibration step to have been performed.
55	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_COARSE_RD: Enable Coarse Read Centering during initial calibration. This calibration step requires the Initial Coarse Pattern Write calibration step to have been performed.
56	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_CUSTOM_RD: Enable the use of a custom read pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0, 2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation
57	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_CUSTOM_WR: Enable the use of a custom write pattern during initial calibration. This algorithm is not required to be run to calibrate the PHY. If it is run, it must be performed after the Coarse Read Algorithm has been run. When this bit is set, bit 1 must be set and bits 0,2,3,4,5,6,7 must be reset. This bit is reserved. It must be written to zero for correct operation.

Bits	SCOM	Field Mnemonic: Description
58	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ABORT_ON_CAL_ERROR: Stop the initial calibration sequence if an error occurs. If more than one calibration algorithm is enabled and an error occurs before the last calibration algorithm is started, the PHY does not perform any calibration algorithm after the errant calibration algorithm completes.
59	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_DIGITAL_EYE: Enable the internal digital eye characterization assist logic. Do not run this algorithm during normal calibration.
60:63	RW	DDRPHY_PC_INIT_CAL_CONFIG0_P1_ENA_RANK_PAIR: Enable Rank Pair ('1'b = Enabled, '0'b = disabled) Bit 12 contains the enable for rank pair 0.Bit 13 contains the enable for rank pair 1.Bit 14 contains the enable for rank pair 2.Bit 15 contains the enable for rank pair 3.

Register Name	***PC Initial Calibration Config1***
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_CONFIG1_P1
Address	8001C0170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:51	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_COUNT: Refresh count specifies the number of refresh commands to insert at the start of an initial calibration. The value zero causes no refresh commands to be sent when an initial calibration begins.
52:53	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_CONTROL: This field is used to control the refresh logic during initial calibration: '00'b: Refresh commands are only sent at start of initial calibration, based on the value in the REFRESH_COUNT field. '01'b: Use the internal Refresh Interval timer to determine when refresh commands are sent; allow refreshes to occur between calibration routines. '10'b: Reserved '11'b: Use the internal Refresh Interval timer to determine when refresh commands should be sent; in addition to allowing refreshes commands to be issued between calibration routines, also allow refreshes to interrupt each calibration routine (as required). This is the recommended setting when refreshes are required during initial calibration.
54	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_ALL_RANKS: '1'b Indicates that all ranks should be refreshed during initial calibration. When a refresh is generated by the DDR PHY all of the chip selects are asserted at the same time during one refresh command. '0'b indicates only the rank currently being calibrated should be refreshed. When a refresh is generated by the DDR PHY, only the chip select of the rank being calibrated are asserted during the refresh command.
55:56	RW	
57:63	RW	DDRPHY_PC_INIT_CAL_CONFIG1_P1_REFRESH_INTERVAL: Refresh Interval - This value times 256 is the number of MEMINTCLKO cycles to wait between sending refresh commands to the memory (tREFI). This value is used when the REFRESH_CONTROL field is configured to use the internal refresh interval timer. 0000001 (min. value) = 256 MEMINTCLKO cycles between refreshes 1111111 (max value) = 32512 MEMINTCLKO cycle between refreshes For example, for a DDR:1600 system running with an 800 MHz memory controller clock frequency, the value 24 ('0011000'b) provides a tREFI setting of 7.68 us (that is, 24 x 256 cycles x 1.25 ns period yields = 7.68 us).The minimum value for this field is 6. If a value less than 6 is written to this field, this field will be set to 6 by hardware. When the Refresh Interval counter expires, an internal pending refresh counter is incremented to count the number of pending refreshes. When refresh commands are issued during initial calibration, all pending refreshes will be issued and the internal counter will be decremented to zero. The internal pending refresh counter is a 4 bit counter with a maximum value of '15'd. An error bit will be set in the register if the internal pending refresh counter overflows.

Register Name	*PC Initial Calibration Error*
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_ERROR_P1
Address	8001C0180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_WR_LEVEL: Write leveling error occurred during initial calibration.
49	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_INITIAL_PAT_WRITE: Initial Pattern write error occurred during the initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
50	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_DQS_ALIGN: DQS Alignment error occurred during initial calibration.
51	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_RDCLK_ALIGN: RDCLK to SysClk alignment error occurred during initial calibration.
52	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_READ_CTR: Read centering error occurred during initial calibration.
53	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_WRITE_CTR: Write centering error occurred during initial calibration.
54	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_INITIAL_COARSE_WR: Initial Coarse Pattern Write error occurred during initial calibration. This calibration step does not report errors. Therefore, this bit is always read '0'b.
55	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_COARSE_RD: Coarse read centering error occurred during initial calibration.
56	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_CUSTOM_RD: Custom pattern read centering error occurred during initial calibration.
57	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_CUSTOM_WR: Custom pattern write centering error occurred during initial calibration.
58	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_DIGITAL_EYE: Digital eye error occurred during initial calibration.
59	RO	constant=0b0
60:63	ROX	DDRPHY_PC_INIT_CAL_ERROR_P1_ERROR_RANK_PAIR: This field indicates which rank pairs encountered an error during initial calibration. Bit 12 reflects the status of rank pair 0.Bit 13 reflects the status of rank pair 1.Bit 14 reflects the status of rank pair 2.Bit 15 reflects the status of rank pair 3.

Register Name	*PC Initial Calibration Status*
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_STATUS_P1
Address	8001C0190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	ROX	DDRPHY_PC_INIT_CAL_STATUS_P1_INIT_CAL_COMPLETE: This field indicates which rank pairs have completed initial calibration, '1'b indicates the rank pair has completed an initial calibration sequence. bit 0 reflects the status of rank pair 0bit 1 reflects the status of rank pair 1bit 2 reflects the status of rank pair 2bit 3 reflects the status of rank pair 3

Bits	SCOM	Field Mnemonic: Description
52:56	ROX	
57	ROX	DDRPHY_PC_INIT_CAL_STATUS_P1_PER_CAL_ABORT: Reserved. This reserved field might contain information that is helpful for hardware debugging. Do not assume that it is read as zeros Periodic Calibration Abort. Read Only. This bit is set by hardware when the pc_errn_in transitions from high to low, a periodic calibration is in progress and the ABORT_ON_ERR_EN bit is set. This bit is reset at the start of every new calibration.
58:63	ROX	

Register Name	***PC Initial Calibration Mask***
Mnemonic	DPHY23.DDRPHY_PC_INIT_CAL_MASK_P1
Address	8001C01A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_WR_LEVEL_MASK: Mask Write leveling error
49	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_INITIAL_PAT_WRITE_MASK: Mask Initial Pattern write error
50	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_DQS_ALIGN_MASK: Mask DQS Alignment error
51	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_RDCLK_ALIGN_MASK: Mask RDCLK to SysClk alignment error
52	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_READ_CTR_MASK: Mask Read centering error
53	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_WRITE_CTR_MASK: Mask Write centering error
54	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_INITIAL_COARSE_WR_MASK: Mask Initial Coarse Pattern Write centering error
55	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_COARSE_RD_MASK: Mask Coarse read centering error
56	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_CUSTOM_RD_MASK: Mask Custom pattern read centering error
57	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_CUSTOM_WR_MASK: Mask Custom pattern write centering error
58	RW	DDRPHY_PC_INIT_CAL_MASK_P1_ERROR_DIGITAL_EYE_MASK: Mask Digital Eye error
59:63	RO	constant=0b00000

Register Name	***PC IO PVT N/P FET Driver Status***
Mnemonic	DPHY23.DDRPHY_PC_IO_PVT_FET_STATUS_P1
Address	8001C01B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P1_PVTP: PFET Driver PVTP value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.

Bits	SCOM	Field Mnemonic: Description
53:57	ROX	DDRPHY_PC_IO_PVT_FET_STATUS_P1_PVTN: NFET Driver PVTN value observed. This is the value calculated by the on-chip impedance calibration macro external to the DDR PHY.
58:63	RO	constant=0b000000

Register Name	*PC Mode 0 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP0_P1
Address	8001C01C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP0_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP0_P1
Address	8001C01D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP0_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP0_P1
Address	8001C01E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP0_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP0*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP0_P1
Address	8001C01F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP0_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	***PC Mode 0 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP0_P1
Address	8001C0200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP0_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP0_P1
Address	8001C0210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP0_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP0_P1
Address	8001C0220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_PC_MR2_SEC_RP0_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP0***
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP0_P1
Address	8001C0230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP0_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	***PC Rank Pair 2***
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR2_P1
Address	8001C0300301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_TER: Tertiary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_TER_V: Value in the RANK_PAIR0_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_QUA: Quaternary Rank of Rank Pair 0 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR0_QUA_V: Value in the RANK_PAIR0_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_TER: Tertiary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_TER_V: Value in the RANK_PAIR1_TER field is valid.
60:62	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_QUA: Quaternary Rank of Rank Pair 1 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR2_P1_RANK_PAIR1_QUA_V: Value in the RANK_PAIR1_QUA field is valid.

Register Name	*PC Rank Pair 3*
Mnemonic	DPHY23.DDRPHY_PC_RANK_PAIR3_P1
Address	8001C0310301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_TER: Tertiary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
51	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_TER_V: Value in the RANK_PAIR2_TER field is valid.
52:54	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_QUA: Quaternary Rank of Rank Pair 2 Up to 4 CSNs can be selected to correspond to a rank pair.
55	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR2_QUA_V: Value in the RANK_PAIR2_QUA field is valid.
56:58	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_TER: Tertiary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
59	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_TER_V: Value in the RANK_PAIR3_TER field is valid.
60:62	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_QUA: Quaternary Rank of Rank Pair 3 Up to 4 CSNs can be selected to correspond to a rank pair.
63	RW	DDRPHY_PC_RANK_PAIR3_P1_RANK_PAIR3_QUA_V: Value in the RANK_PAIR3_QUA field is valid.

Register Name	*PC Chip Select ID Configuration*
Mnemonic	DPHY23.DDRPHY_PC_CSID_CFG_P1
Address	8001C0330301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_CSID_CFG_P1_CS0_INIT_CAL_VALUE: If CS0 is not selected by any of the Rank Pair registers, then CS0 is driven to this value during initial calibration. If CS0 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
49	RW	DDRPHY_PC_CSID_CFG_P1_CS1_INIT_CAL_VALUE: If CS1 is not selected by any of the Rank Pair registers, then CS1 is driven to this value during initial calibration. If CS1 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
50	RW	DDRPHY_PC_CSID_CFG_P1_CS2_INIT_CAL_VALUE: If CS2 is not selected by any of the Rank Pair registers, then CS2 is driven to this value during initial calibration. If CS2 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
51	RW	DDRPHY_PC_CSID_CFG_P1_CS3_INIT_CAL_VALUE: If CS3 is not selected by any of the Rank Pair registers, then CS3 is driven to this value during initial calibration. If CS3 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
52	RW	DDRPHY_PC_CSID_CFG_P1_CS4_INIT_CAL_VALUE: If CS4 is not selected by any of the Rank Pair registers, then CS4 is driven to this value during initial calibration. If CS4 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
53	RW	DDRPHY_PC_CSID_CFG_P1_CS5_INIT_CAL_VALUE: If CS5 is not selected by any of the Rank Pair registers, then CS5 is driven to this value during initial calibration. If CS5 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.

Bits	SCOM	Field Mnemonic: Description
54	RW	DDRPHY_PC_CSID_CFG_P1_CS6_INIT_CAL_VALUE: If CS6 is not selected by any of the Rank Pair registers, then CS6 is driven to this value during initial calibration. If CS6 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
55	RW	DDRPHY_PC_CSID_CFG_P1_CS7_INIT_CAL_VALUE: If CS7 is not selected by any of the Rank Pair registers, then CS7 is driven to this value during initial calibration. If CS7 is a CSID bit, then set this value to select the rank to be calibrated. Otherwise this bit is a don't care.
56:63	RO	constant=0b00000000

Register Name	***PC Rank Group Extension***
Mnemonic	DPHY23.DDRPHY_PC_RANK_GROUP_EXT_P1
Address	8001C0350301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP0_TER: '1'b - Enable Address Mirroring Rank Pair 0 Tertiary
49	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP0_QUA: '1'b - Enable Address Mirroring Rank Pair 0 Quaternary
50	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP1_TER: '1'b - Enable Address Mirroring Rank Pair 1 Tertiary
51	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP1_QUA: '1'b - Enable Address Mirroring Rank Pair 1 Quaternary
52	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP2_TER: '1'b - Enable Address Mirroring Rank Pair 2 Tertiary
53	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP2_QUA: '1'b - Enable Address Mirroring Rank Pair 2 Quaternary
54	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP3_TER: '1'b - Enable Address Mirroring Rank Pair 3 Tertiary
55	RW	DDRPHY_PC_RANK_GROUP_EXT_P1_ADDR_MIRROR_RP3_QUA: '1'b - Enable Address Mirroring Rank Pair 3 Quaternary
56:63	RO	constant=0b00000000

Register Name	***PC Mode 0 Primary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP1_P1
Address	8001C11C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP1_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP1_P1
Address	8001C11D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP1_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP1_P1
Address	8001C11E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP1_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP1_P1
Address	8001C11F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP1_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP1*
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP1_P1
Address	8001C1200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_PC_MR0_SEC_RP1_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 1 Secondary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP1_P1
Address	8001C1210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP1_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 2 Secondary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP1_P1
Address	8001C1220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP1_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	***PC Mode 3 Secondary RP1***
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP1_P1
Address	8001C1230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP1_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP2_P1
Address	8001C21C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP2_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP2_P1
Address	8001C21D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP2_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP2_P1
Address	8001C21E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP2_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP2_P1
Address	8001C21F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP2_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP2_P1
Address	8001C2200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP2_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP2_P1
Address	8001C2210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP2_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP2_P1
Address	8001C2220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP2_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP2*
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP2_P1
Address	8001C2230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP2_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*PC Mode 0 Primary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR0_PRI_RP3_P1
Address	8001C31C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_PRI_RP3_P1_MODE_REGISTER_0_VALUE: Defined by each protocol:

Register Name	*PC Mode 1 Primary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR1_PRI_RP3_P1
Address	8001C31D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_PRI_RP3_P1_MODE_REGISTER_1_VALUE: Defined by each protocol:

Register Name	*PC Mode 2 Primary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR2_PRI_RP3_P1
Address	8001C31E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_PRI_RP3_P1_MODE_REGISTER_2_VALUE: Defined by each protocol:

Register Name	*PC Mode 3 Primary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR3_PRI_RP3_P1
Address	8001C31F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_PRI_RP3_P1_MODE_REGISTER_3_VALUE: Defined by each protocol: For correct DDR4 MPR Write command operations, both ranks, if more than one rank exists, of the rank pair must have A2 set to the same value.

Register Name	*PC Mode 0 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR0_SEC_RP3_P1
Address	8001C3200301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR0_SEC_RP3_P1_MODE_REGISTER_0_VALUE: DDR3: The value in this register reflects MR0 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR4 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 1 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR1_SEC_RP3_P1
Address	8001C3210301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR1_SEC_RP3_P1_MODE_REGISTER_1_VALUE: DDR3: The value in this register reflects MR1 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR5 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 2 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR2_SEC_RP3_P1
Address	8001C3220301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR2_SEC_RP3_P1_MODE_REGISTER_2_VALUE: DDR3: The value in this register reflects MR2 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: The value in this register reflects MR6 for the primary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory).

Register Name	*PC Mode 3 Secondary RP3*
Mnemonic	DPHY23.DDRPHY_PC_MR3_SEC_RP3_P1
Address	8001C3230301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_PC_MR3_SEC_RP3_P1_MODE_REGISTER_3_VALUE: DDR3: The value in this register reflects MR3 for the secondary rank of the targeted rank pair as defined in and. The contents of this register are updated when written, or when an MRS (mode register set) command is sent from the memory controller (that is, when the DDR PHY snoops the command as it is sent to the memory). DDR4: Reserved.

Register Name	*SEQ Read/Write Data 0*
Mnemonic	DPHY23.DDRPHY_SEQ_RD_WR_DATA0_P1
Address	8001C4000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA0_P1_RD_WR_DATA_REG0: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0 described inare written to MPR0. - bits 8:15 of register 0 described in are written to MPR1. - bits 0:7 of register 1 described in are written to MPR2. - bits 8:15 of register 1 described in are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	*SEQ Read/Write Data 1*
Mnemonic	DPHY23.DDRPHY_SEQ_RD_WR_DATA1_P1
Address	8001C4010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RD_WR_DATA1_P1_RD_WR_DATA_REG1: These registers define the values written to memory during Initial Pattern write and define the expect data used during Custom Read centering and Custom Write Centering. If CUSTOM_INIT_WRITE equals '1'b then behavior depends on protocol: DDR3: During Initial Pattern Write: Bits 0:7 of register 0 are written to the reserved location in memory defined by the SEQ Reserved Address 0-4 registers. To provide correct data for reads during Custom Read Centering and Custom Write Centering: - bits 8:15 of register 0 must be written to the same value as bits 0:7 of register 0. - bits 0:7 of register 1 must be written to the same value as bits 0:7 of register 0. - bits 8:15 of register 1 must be written to the same value as bits 0:7 of register 0. DDR4: During Initial Pattern Write: - bits 0:7 of register 0 described inare written to MPR0. - bits 8:15 of register 0 described in are written to MPR1. - bits 0:7 of register 1 described in are written to MPR2. - bits 8:15 of register 1 described in are written to MPR3. During Custom Read Centering and Custom Write Centering: If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '00'b, then bits 0:7 of register 0 are compared to the data read from memory. If the READ_CENTERING_MODE field of the DP18 IO RX Config 0 register is set to '11'b, then the contents of these registers are compared to the data read from memory, staggered across DQ lanes and rotated every 8 beats through the 4 bytes defined in these registers.

Register Name	*SEQ Configuration 0*
Mnemonic	DPHY23.DDRPHY_SEQ_CONFIG0_P1
Address	8001C4020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_CONFIG0_P1_MPR_PATTERN_BIT: Read and write calibration algorithms are based on eight-beat bursts. This register controls the readwrite burst data pattern. For Write data: The MPR_PATTERN_BIT value is available on all bit lanes of beat 1, 3, 5 and 7 and the inverse of the MPR_PATTERN_BIT on all bit lanes of beat 2, 3, 6 and 8, ensuring all bit lanes toggle consecutive beats. If the protocol requires a burst length longer than eight beats, the pattern in this register is repeated until all data beats are defined. For Read data: Bit 0 is brought out as output of Sequencer and DP18 composes the expected pattern from this output.
49	RW	DDRPHY_SEQ_CONFIG0_P1_TWO_CYCLE_ADDR_EN: DDR3 and DDR4: '1'b - During calibrations, the address and command are driven onto the address/cmd bus for two memory clock cycles while the appropriate chip selects are active only during the second memory clock cycle of the command. '0'b - During calibration, the address and command and chip selects are driven and active for one memory clock cycle. All other protocols: This bit must be set to '0'b. The address and command and chip selects are driven active for one memory clock cycle.
50:53	RW	DDRPHY_SEQ_CONFIG0_P1_MR_MASK_EN: Mode Register mask enable. This register masks, or disables, the mode register access by the calibration algorithms. Bits 0- 3 map to mode register 0 - 3.
54	RW	DDRPHY_SEQ_CONFIG0_P1_DELAYED_PAR: '0'b - DDR4 PAR signal is generated coincident with addresscommand signals during init cal '1'b - DDR4 PAR signal is generated one clock cycle later than addresscommand signals during init cal Bit applies to DDR4 only and is don't care for DDR3
55	RW	DDRPHY_SEQ_CONFIG0_P1_LRDIMM_CONTEXT: Value of context bit to be used during F[0]RC12 LRDIMM Control Word commands.
56	RW	DDRPHY_SEQ_CONFIG0_P1_FORCE_RESERVED: '0'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will use the DDR4 MPR registers. '1'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory. If the PROTOCOL field in the register described in does not equal DDR4, this bit is not used and is a 'don't care'.
57	RW	DDRPHY_SEQ_CONFIG0_P1_HALT_ROTATION: '0'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will rotate through the use of all 4 MPR registers by changing BA[0:1] during the calibration. '1'b - When the PROTOCOL field in the register described in equals DDR4, Custom Read Centering and Initial Pattern Write will set BA[0:1] = '00'b. The same 8 beats will be read repeatedly on a particular DQ lane and the expect data will not be rotated through the 4 bytes of the register every 8 beats. If the PROTOCOL field in the register described in does not equal DDR4, this bit is not used and is a 'don't care'.
58	RW	DDRPHY_SEQ_CONFIG0_P1_FORCE_MPR: '0'b - When the PROTOCOL field in the register described in equals DDR3, Custom Read Centering and Initial Pattern Write will use the Reserved Location in memory, allowing a custom 8 bit repeating pattern to be compared during read centering. '1'b - When the PROTOCOL field in the register described in equals DDR3, Custom Read Centering and Initial Pattern Write will use 4 DRAM MPR registers, allowing Custom Read Centering to read the 4 MPR registers. This is not a mode described by the DDR3 JEDEC standard. If the PROTOCOL field in the register described in does not equal DDR3, this bit is not used and is a 'don't care'.
59:63	RW	

Register Name	*SEQ Reserved Address 0*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR0_P1
Address	8001C4030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR0_P1_RESERVED_ADDR0: Reserved Address Field 0. Exact definition is protocol dependent DDR3DDR4: Bits 0-15 map to A0-A15. The lower 2 bytes of row address are used. RLDRAM2RLDRAM3: Bits 0-15 map to A0-A15. Lower 2 bytes of the row and column address are used.

Register Name	*SEQ Reserved Address 1*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR1_P1
Address	8001C4040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR1_P1_RESERVED_ADDR1: Reserved Address Field 1. The exact definition is protocol dependent For DDR3: bits 0 - 15 are reserved. For DDR4: Bits 0 - 4 map to A16 - A20; bits 5 - 15 are reserved. This protocol uses the upper bit of the row address. For RLDRAM2 and RLDRAM3: Bits 0 - 6 map to A16 - A22; bits 7 - 15 are reserved. This protocol uses the upper bits of the row and column address.

Register Name	*SEQ Reserved Address 2*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR2_P1
Address	8001C4050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR2_P1_RESERVED_ADDR2: Reserved Address Field 2. This register controls the lower 2 bytes of the column address. Exact definition is protocol and command dependent Some address pins depend upon the value of DDR4_CMD_SIG_REDUCTION. DDR3 writes with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR3 reads with DDR4_CMD_SIG_REDUCTION = '0'b: A13:A15 = bits 13:15 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 writes with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '1'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A0:A9 = bits 0:9 DDR4 reads with DDR4_CMD_SIG_REDUCTION = '1'b: A15 = '0'b A14 = '0'b A13 = bit 13 A12 (BL8) = '1'b A11 = bit 11 A10 (AP) = '0'b A4:A9 = bits 4:9 A0:A3 = '0000'b DDR4 Refresh: A11:A15 = bits 11:15 A10 (AP) = '1'b A0:A9 = bits 0:9 DDR3 Refresh: A0:A15 = bits 0:15

Register Name	*SEQ Reserved Address 3*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR3_P1
Address	8001C4060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR3_P1_RESERVED_ADDR3: Reserved Address Field 3. The exact definition is protocol dependent For DDR3DDR4RLDRAM2RLDRAM3: bits 0-15 are reserved

Register Name	*SEQ Reserved Address 4*
Mnemonic	DPHY23.DDRPHY_SEQ_RESERVED_ADDR4_P1
Address	8001C4070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_RESERVED_ADDR4_P1_RESERVED_ADDR4: Reserved Address Field 4. Bank Address. The exact definition is protocol dependent For DDR3RLDRAM2: Bits 0 - 2 map to BA0-BA2. Bits 3 - 15 are reserved. For DDR4: Bits 0 - 1 map to BA0-BA1 and bits 2 - 3 map to BG0 - BG1. Bits 4 - 15 are reserved. MPR Reads performed by the internal calibration routines: BA0-BA1 are forced to '00'b to access MPR0. Reads performed by the internal calibration routines: BG1 is toggled (both values of BG1 are used/reserved) and all banks are accessed (all BA0-BA1 addressed used/reserved). For RLDRAM2: Bits 0 - 2 map to BA0 - BA2. Bits 3 - 15 are reserved. For RLDRAM3: Bits 0 - 3 map to BA0 - BA3. Bits 4 - 15 are reserved.

Register Name	*SEQ Error Status 0*
Mnemonic	DPHY23.DDRPHY_SEQ_ERROR_STATUS0_P1
Address	8001C4080301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_MULTIPLE_REQ_ERROR: '1'b - Error: Multiple requests received at same time.
49	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_INVALID_REQTYPE_ERROR: '1'b - Error: In the current state, this request is not expected.
50	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_EARLY_REQ_ERROR: '1'b - Error: A new request arrived before acknowledge of previous request.
51:53	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_MULTIPLE_REQ_SOURCE: If MULTIPLE_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 3:5 = {PC_REQ, RC_REQ, WC_REQ}
54:57	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_INVALID_REQTYPE: If INVALID_REQTYPE_ERROR is flagged, the type of request is indicated by this register. See functional description section of Sequence generator for request types from each source.

Bits	SCOM	Field Mnemonic: Description
58:60	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_INVALID_REQ_SOURCE: If INVALID_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 10:12 = {PC_REQ, RC_REQ, WC_REQ}
61:63	ROX	DDRPHY_SEQ_ERROR_STATUS0_P1_EARLY_REQ_SOURCE: If EARLY_REQ_ERROR is flagged, the source of request is indicated by these bits. bits 13:15 = {PC_REQ, RC_REQ, WC_REQ}

Register Name	***SEQ Error Mask 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ERROR_MASK0_P1
Address	8001C4090301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ERROR_MASK0_P1_MULT_REQ_ERR_MASK: '1'b - Prevent the MULTIPLE_REQ_ERROR bit from being set in the register. '0'b - Allow the MULTIPLE_REQ_ERROR bit to be set.
49	RW	DDRPHY_SEQ_ERROR_MASK0_P1_INVALID_REQTYPE_ERR_MASK: '1'b - Prevent the INVALID_REQTYPE_ERROR bit from being set in the register. '0'b - Allow the INVALID_REQTYPE_ERROR bit to be set.
50	RW	DDRPHY_SEQ_ERROR_MASK0_P1_EARLY_REQ_ERR_MASK: '1'b - Prevent the EARLY_REQ_ERROR bit from being set in the register. '0'b - Allow the EARLY_REQ_ERROR bit to be set.
51:63	RW	

Register Name	***SEQ ODT Write Configuration 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG0_P1
Address	8001C40A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P1_ODT_WR_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG0_P1_ODT_WR_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Write Configuration 1***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG1_P1
Address	8001C40B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P1_ODT_WR_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG1_P1_ODT_WR_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Write Configuration 2***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG2_P1
Address	8001C40C0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P1_ODT_WR_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG2_P1_ODT_WR_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Write Configuration 3***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_WR_CONFIG3_P1
Address	8001C40D0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P1_ODT_WR_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is written. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_WR_CONFIG3_P1_ODT_WR_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is written. This field corresponds to the odd rank.

Register Name	***SEQ ODT Read Configuration 0***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG0_P1
Address	8001C40E0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P1_ODT_RD_VALUES0: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG0_P1_ODT_RD_VALUES1: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 1*
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG1_P1
Address	8001C40F0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P1_ODT_RD_VALUES2: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG1_P1_ODT_RD_VALUES3: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 2*
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG2_P1
Address	8001C4100301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P1_ODT_RD_VALUES4: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG2_P1_ODT_RD_VALUES5: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ ODT Read Configuration 3*
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_RD_CONFIG3_P1
Address	8001C4110301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P1_ODT_RD_VALUES6: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2 is read. This field corresponds to the even rank.
56:63	RW	DDRPHY_SEQ_ODT_RD_CONFIG3_P1_ODT_RD_VALUES7: This 8 bit value is driven on the ODT pins 0:7 when rank {0-3}*2+1 is read. This field corresponds to the odd rank.

Register Name	*SEQ Memory Timing Parameter 0*
Mnemonic	DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM0_P1
Address	8001C4120301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TMOD_CYCLES: For DDR3 and DDR4: max(tMRD, tMOD) For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TRCD_CYCLES: For DDR3 and DDR4: tRCD For RLD2 and RLD3: reserved
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TRP_CYCLES: For DDR3 and DDR4 tRP For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM0_P1_TRFC_CYCLES: For DDR3 and DDR4: tRFC For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 1*
Mnemonic	DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM1_P1
Address	8001C4130301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TZQINIT_CYCLES: For DDR3, DDR4, RLD2, and RLD3: max(tZQINIT,tZQOPER)
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TZQCS_CYCLES: For DDR3, DDR4, RLD2, and RLD3: tZQCS
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TWLDQSEN_CYCLES: For DDR3 and DDR4: tWLDQSEN For RLD2 and RLD3: reserved
60:63	RW	DDRPHY_SEQ_MEM_TIMING_PARAM1_P1_TWRMRD_CYCLES: For DDR3 and DDR4: tWLMRD For RLD2 and RLD3: reserved

Register Name	*SEQ Memory Timing Parameter 2*
Mnemonic	DPHY23.DDRPHY_SEQ_MEM_TIMING_PARAM2_P1
Address	8001C4140301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:51	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P1_TODTLON_OFF_CYCLES: For DDR3 and DDR4: max(ODTLon, ODTLoff) When the ODT values change during a calibration algorithm, the PHY waits TODTLON_OFF_CYCLES ^ 2 memory clock cycles before changing the ODT values. The ODT values might change because of a rank change or a change from read ODT values to write ODT values, or because an MRS command is issued. The ODT pins must be forced to zero during MRS commands when RTT_Nom is enabled via MR1. This is independent of the values stored in the SEQ ODT Write/Read Configuration {0-3} registers. Before issuing the MRS command, the DDR PHY checks if the ODT pin was recently changed within the window and waits for the tODTLOFF cycles to expire. When tODTLOFF expires, the ODT value is forced to zero and the DDR PHY again waits for tODTLOFF cycles. After this, the MRS command is issued and the DDR PHY waits for tMOD cycles and then restores the ODT pins to their prior state. For RLD2 and RLD3: reserved
52:55	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P1_TRC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tRC
56:59	RW	DDRPHY_SEQ_MEM_TIMING_PARAM2_P1_TMRSC_CYCLES: For DDR3 and DDR4: reserved For RLD2 and RLD3: tMRSC
60:63	RW	

Register Name	***SEQ Low Power Termination Address 2***
Mnemonic	DPHY23.DDRPHY_SEQ_LPT_ADDR2_P1
Address	8001C4170301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR2_P1_LPT_ADDR2: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	***SEQ Low Power Termination Address 3***
Mnemonic	DPHY23.DDRPHY_SEQ_LPT_ADDR3_P1
Address	8001C4180301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000

Bits	SCOM	Field Mnemonic: Description
48:63	RW	DDRPHY_SEQ_LPT_ADDR3_P1_LPT_ADDR3: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	*SEQ Low Power Termination Address 4*
Mnemonic	DPHY23.DDRPHY_SEQ_LPT_ADDR4_P1
Address	8001C4190301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:63	RW	DDRPHY_SEQ_LPT_ADDR4_P1_LPT_ADDR4: The bit positions and mapping of the bit positions to the AddressBABG pins in DDR3DDR4 of the SEQ Low Power Termination Address{2-4} Registers correspond to the bit positions and mapping of the bit positions to the AddressBABG pins in the SEQ Reserved Address{2-4} registers. The content of these registers which correspond to: DDR3: BA(0:2), A(0:9), A(11), A(13:15) DDR4: BA(0:1), BG(0), A(0:9), A(11), A(13), A(17), BG(1) is driven onto the AddressBABG pins during 'idle' bus cycles during periodic calibration. Register bits within these registers which correspond to AddressBABG not listed above are reserved. This register is only used in DDR3 and DDR4. DDR3: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13:15) = LPT_ADDR2(13:15) BA(0:2) = LPT_ADDR4(0:2) All other register bit positions are reserved. DDR4: A(0:9) = LPT_ADDR2(0:9) A(11) = LPT_ADDR2(11) A(13) = LPT_ADDR2(13) A(17) = LPT_ADDR3(1) BA(0:1) = LPT_ADDR4(0:1) BG(0:1) = LPT_ADDR4(2:3) All other register bit positions are reserved.

Register Name	*SEQ ZQCal Encoded Rank Control 0*
Mnemonic	DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1
Address	8001C41A0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG0_P1_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ZQCal Encoded Rank Control 1***
Mnemonic	DPHY23.DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1
Address	8001C41B0301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_ENC_0_2: '1'b - Enable Dual ZQCal for Rank Group {0,2}
49	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_TYPE_0_2: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
50:52	RW	
53:55	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_0_2: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {0,2}
56	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_ENC_1_3: '1'b - Enable Dual ZQCal for Rank Group {1,3}
57	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_TYPE_1_3: '0'b - Encoded CS bit for ZQCal is on a CSN '1'b - Encoded CS bit fir ZQCal is on an ODT
58:60	RW	
61:63	RW	DDRPHY_SEQ_ZQCAL_ENC_RANK_CTL_REG1_P1_ZQCAL_SEL_1_3: Selects which CSN or ODT is used for CS bit for ZQCal on Rank Group {1,3}

Register Name	***SEQ ODT Default Configuration***
Mnemonic	DPHY23.DDRPHY_SEQ_ODT_DEFAULT_CFG_P1
Address	8001C4240301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:55	RW	DDRPHY_SEQ_ODT_DEFAULT_CFG_P1_ODT_DEF_VALUES: The eight ODT values in this register are driven to the ODT pins during MRS commands. Typically the PDT value should be set to 0 during MRS commands. However if the ODT is an ODTCID function pin, then the corresponding bit in this register should be set to the desired CID value, and the corresponding bits in the ODT Write and Read Configuration registers should be set to similar values. Where: bit 0 - ODT value for ODT pin 0 during MRS command bit 1 - ODT value for ODT pin 1 during MRS command bit 2 - ODT value for ODT pin 2 during MRS command ... bit 7 - ODT value for ODT pin 7 during MRS command
56:63	RW	

Register Name	***RC Configuration 0***
Mnemonic	DPHY23.DDRPHY_RC_CONFIG0_P1
Address	8001C8000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_RC_CONFIG0_P1_GLOBAL_PHY_OFFSET: Global PHY Offset, GPO. This field is the number of memory clock cycles added to the total read latency in the PHY. Minimum Value: When ADVANCE_RD_VALID = '0'b, the minimum value for this field is 5 + max{RoundUp(System_Delay)} - RLO. When ADVANCE_RD_VALID = '1'b, the minimum value for this field is 6 + max{RoundUp(System_Delay)} - RLO. When SPAM_EN = '1'b the minimum value calculated for this field is increased by 1. Where: System_Delay is the round-trip delay in the memory system: System_Delay = (((ADR_DELAY - '64'd) + {wire delay from the PHY memory clock output to the DRAM module converted to units of 1128th of a MEMINTCLKO clock cycle} + {delay of DQS at the memory module pin relative to memory clock at the memory module pin introduced by the memory module (that is, tDQSCK) converted to units of 1128th of a MEMINTCLKO clock cycle} + {wire delay from the DRAM DQS output to the PHY converted to units of 1128th of a MEMINTCLKO clock cycle}) 128) + {number of pipeline stages in the addrcmd path} + {number of pipeline stages in the read data path} max{RoundUp(System_Delay)} is the largest System_Delay in the memory system across all data bits and all ranks rounded up to the next integer memory clock cycle period value. min{RoundDown(System_Delay)} is the smallest System_Delay in the memory system across all data bits and all ranks rounded down to the next integer memory clock cycle period value. RLO is the READ_LATENCY_OFFSET field. Maximum Value: In 2:1 mode, the maximum value for this field is 'B'h. In 4:1 mode, the maximum value for this field is 'D'h.
52	RW	DDRPHY_RC_CONFIG0_P1_ADVANCE_RD_VALID: Number of MEMCTLCLKI clock cycles MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted before the associated read data. '0'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted during the same MEMCTLCLKI clock cycle the associated read data is valid. '1'b - The MEMCTLCRDVO and MEMCTLCRDVBO, when applicable, are asserted one MEMCTLCLKI clock cycle before the associated read data is valid. In 4:1 Data Multiplexer mode, this field must be '0'b.
53	RW	DDRPHY_RC_CONFIG0_P1_PER_DUTY_CYCLE_SW: Set to '0' for normal function. Read commands are generated during periodic cal with a 50% duty cycle. When set to '1', periodic cal issues read commands continuously.
54:56	RW	DDRPHY_RC_CONFIG0_P1_PER_REPEAT_COUNT: If this field is 000 then the number of additional periodic cals performed per request is zero. A nonzero value in this field will preform additional periodic calibrations for each request per below: 000 is No additional periodic cal iterations are performed per request. 001 is One additional periodic cal iteration is performed per request. 010 is Two additional periodic cal iterations are performed per request. .... 111 is Seven additional periodic cal iterations are performed per request.
57	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP0: '1'b - Single bit MPR pattern memory devices in Rank Pair 0. '0'b - All bit MPR pattern memory devices in Rank Pair 0.
58	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP1: '1'b - Single bit MPR pattern memory devices in Rank Pair 1. '0'b - All bit MPR pattern memory devices in Rank Pair 1.
59	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP2: '1'b - Single bit MPR pattern memory devices in Rank Pair 2. '0'b - All bit MPR pattern memory devices in Rank Pair 2.
60	RW	DDRPHY_RC_CONFIG0_P1_SINGLE_BIT_MPR_RP3: '1'b - Single bit MPR pattern memory devices in Rank Pair 3. '0'b - All bit MPR pattern memory devices in Rank Pair 3.
61	RW	DDRPHY_RC_CONFIG0_P1_ALIGN_ON_EVEN_CYCLES: This bit is only valid in 4:1 Data Multiplexer Mode. In 2:1 Data Multiplexer Mode it must be '0'b. When set, latency is added, if required, to have the read data returned on the MEMCTL Interface with the first four beats of read data returned in the same dphy_nclk cycle on the R, F, RX, and FX pins. '1'b = The first beat of a read data burst is always returned on the R pin, second beat on the F pin, third beat on the RX pin, and fourth beat on the FX pin. '0'b = The first beat of a read data burst may be returned on the R or RX pin, second beat on the F or FX pin, third beat on the RX or R pin, and fourth beat on the FX or F pin. This bit must be '0'b when a burst length that is not a multiple of four is used.

Bits	SCOM	Field Mnemonic: Description
62	RW	DDRPHY_RC_CONFIG0_P1_PERFORM_RDCLK_ALIGN: This bit must be set to '1'b in hardware. This bit is a method for behavioral simulations to skip the calibration step described in. '1'b - The calibration described in must be performed for correct operation. '0'b - In a zero wire delay behavioral simulation, the RTL ignores the register settings associated with SysClkRdClk Alignment. Values in the register described in have no effect. The calibration described in fails if it is run.
63	RW	DDRPHY_RC_CONFIG0_P1_STAGGERED_PATTERN: '0'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Serial mode by the DDR PHY during Custom Read Centering. '1'b - A[12:11], MPR Read Format, of the MR3 register in DDR4 memory modules will be set to Staggered mode by the DDR PHY during Custom Read Centering.

Register Name	***RC Configuration 1***
Mnemonic	DPHY23.DDRPHY_RC_CONFIG1_P1
Address	8001C8010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:61	RW	DDRPHY_RC_CONFIG1_P1_OUTER_LOOP_CNT: This field must remain at the reset value for normal mainline operation. Outer loop iteration count for digital eye. This field must be loaded with the required number of outer loop iterations before starting the digital eye function.
62:63	RO	constant=0b00

Register Name	***RC Configuration 2***
Mnemonic	DPHY23.DDRPHY_RC_CONFIG2_P1
Address	8001C8020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:52	RW	DDRPHY_RC_CONFIG2_P1_CONSEQ_PASS: The number of consecutive passes required when determining the left edge of the data eye when stepping the read strobeclock through the phase rotator. When DIGITAL_EYE_EN is '1'b this field, DIGEYE_MIN_SPACING, specifies the minimum number of cycles between outer loop iterations of digital eye (0-31 tCK cycles). This field must be set to minimum value of 6 when sampling 8 beats of data, and a minimum value of 12 when sampling 4 beats of data.
53:56	RW	
57:58	RW	DDRPHY_RC_CONFIG2_P1_BURST_WINDOW: Beats of data used for INIT and Periodic Read Eye Centering
59	RW	DDRPHY_RC_CONFIG2_P1_ALLOW_RD_FIFO_AUTO_RESET: Automatic Reset Control for RD FIFO
60:63	RO	constant=0b0000

Register Name	*RC Error Status 0*
Mnemonic	DPHY23.DDRPHY_RC_ERROR_STATUS0_P1
Address	8001C8050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_RC_ERROR_STATUS0_P1_RD_CNTL_ERROR: '1'b - Read Control Error.
49:63	RO	constant=0b000000000000000

Register Name	*RC Error Mask 0*
Mnemonic	DPHY23.DDRPHY_RC_ERROR_MASK0_P1
Address	8001C8060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_RC_ERROR_MASK0_P1_RD_CNTL_ERROR_MASK: '1'b - Mask RD_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*RC Configuration 3*
Mnemonic	DPHY23.DDRPHY_RC_CONFIG3_P1
Address	8001C8070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:50	RW	DDRPHY_RC_CONFIG3_P1_FINE_CAL_STEP_SIZE: Fine Calibration step size:000 = 1128, 001 = 164, 010 = 3128, 011 = 132100 = 5128, 101 = 364, 110 = 7128, 111 = 116
51:54	RW	DDRPHY_RC_CONFIG3_P1_COARSE_CAL_STEP_SIZE: Coarse Calibration step size:0000 = 1128, 0001 =164, 0010 = 3128, 0011 = 1320100 = 5128, 0101 = 364, 0110 = 7128, 0111 = 1161000 through 1111 = Reserved. When DIGITAL_EYE_EN is '1'b in the register described in: bit 3:4 Reserved. bit 5: DIGEYE_16_NOT_1: '1'b - Block of 16 BL8 is issued during each outer loop iteration of digital eye. '0'b - One BL8 read is issued during each outer loop iteration of digital eye. bit 6: DIGEYE_REFRESH: '1' b - Issues a precharge and refresh during every outer loop iteration of digital eye. '0'b - Issues a precharge and refresh at least once every 16 outer loop iteration of digital eye.
55:56	RWX	DDRPHY_RC_CONFIG3_P1_DQ_SEL_QUAD: The quadrant within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that will automatically increment during some types of calibrations.
57:59	RWX	DDRPHY_RC_CONFIG3_P1_DQ_SEL_LANE: The data bit within the DP18 being calibrated (read calibrations). Can also be set statically for digital eye. This field must not be modified while calibration is running. This field is part of a counter that automatically increments during some types of calibrations.
60:63	RO	constant=0b0000

Register Name	*WC Configuration 0*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG0_P1
Address	8001CC000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:55	RW	DDRPHY_WC_CONFIG0_P1_TWLO_TWLOE: Number of memory clock cycles which equals: 12 + {The greater of (Twldqsen - Tmod) converted to and rounded up to the nearest integer number of memory clock cycles or (Twlo + Twloe) converted to and rounded up to the nearest integer number of memory clock cycles.} + {The longest DQS wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} + {Plus: The longest DQ wire delay converted to and rounded up to the nearest integer number of memory clock cycles.} Used during Write Leveling.
56	RW	DDRPHY_WC_CONFIG0_P1_WL_ONE_DQS_PULSE: '0'b - continuous DQS pulses during Write Leveling. In 2:1 mode, 32 continuous pulses are sent. In 4:1 mode, 64 continuous pulses are sent. '1'b - one DQS pulse during each Write Leveling adjustment.
57:62	RW	DDRPHY_WC_CONFIG0_P1_FW_WR_RD: Number of memory clock cycles to wait between the write and read command pairs during Write Centering.
63	RW	DDRPHY_WC_CONFIG0_P1_CUSTOM_INIT_WRITE: '1'b - Write the data pattern in the registers described in during the Initial Pattern Write algorithm. '0'b - Write the MPR like pattern defined by the field MPR_PATTERN_BIT in the register defined in during the Initial Pattern Write algorithm.

Register Name	*WC Configuration 1*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG1_P1
Address	8001CC010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG1_P1_BIG_STEP: The amount the phase rotator value is adjusted during a big step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (BIG_STEP + 1) 128th of a memory clock.
52:54	RW	DDRPHY_WC_CONFIG1_P1_SMALL_STEP: The amount the phase rotator value is adjusted during a small step in the Write Leveling and Write Centering algorithms. The amount of the adjustment is (SMALL_STEP + 1)128th of a memory clock. Note: The Write Leveling and Write Centering algorithms will achieve the most accurate results when this field is set to zero.
55:60	RW	DDRPHY_WC_CONFIG1_P1_WR_PRE_DLY: The number of dphy_nclk cycles between a write command and a precharge command in the Coarse Initial Pattern Write, Initial Write, and Write Centering calibration algorithms.
61:63	RO	constant=0b000

Register Name	*WC Configuration 2*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG2_P1
Address	8001CC020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:51	RW	DDRPHY_WC_CONFIG2_P1_NUM_VALID_SAMPLES: The Write Leveling and Write Centering algorithms require NUM_VALID_SAMPLES + 1 samples at one delay to determine the delay setting returns valid data. One invalid sample at any time causes an invalid sample. The Write Leveling algorithm performs the second to last sample at the current sample point plus 12 UI to ensure that the current sample point is at the '0'b to '1'b transition.
52:57	RW	DDRPHY_WC_CONFIG2_P1_FW_RD_WR: This delay value is used in two places in the write centering algorithm. This value sets the delay between a read and write command in memory clock cycles. This value must be a minimum of 11 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as tWTR. The second place this delay value is used is to set the delay between the read and the precharge command in memory clock cycles. This value must be a minimum of 3 plus the spacing required by the protocol. For example, DDR3 specifies this spacing as AL + tRTP. This field must be set to the larger of the two values in number of memory clock cycles. FW_RD_WR = max(tWTR + 11, AL + tRTP + 3)
58:62	RW	
63	RW	DDRPHY_WC_CONFIG2_P1_EN_RESET_WR_DELAY_WL: '1'b - The registers described in are reset at the start of the Write Leveling Calibration algorithm for rank pair 0. '0'b - The registers described in are not reset at the start of the Write Leveling Calibration algorithm.

Register Name	*WC Error Status 0*
Mnemonic	DPHY23.DDRPHY_WC_ERROR_STATUS0_P1
Address	8001CC030301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_WC_ERROR_STATUS0_P1_WR_CNTL_ERROR: '1'b - Write Control Error.
49:63	RO	constant=0b000000000000000

Register Name	*WC Error Mask 0*
Mnemonic	DPHY23.DDRPHY_WC_ERROR_MASK0_P1
Address	8001CC040301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_ERROR_MASK0_P1_WR_CNTL_ERROR_MASK: '1'b - Mask WR_CNTL_ERROR.
49:63	RO	constant=0b000000000000000

Register Name	*WC Configuration 3*
Mnemonic	DPHY23.DDRPHY_WC_CONFIG3_P1
Address	8001CC050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_WC_CONFIG3_P1_DDR4_MRS_CMD_DQ_EN: In DDR4: '1'b - When a DDR4 MRS command is detected passing through the DDR PHY, the values in the MRS_CMD_DATA_N{0,1,2,3} fields in the register described in will be driven out on the DQ pins. '0'b - DQ pins are not driven when an MRS command passes through the DDR PHY. (DDR4 ballot 1716.52) For all other protocols, this bit must be '0'b.
49:54	RW	DDRPHY_WC_CONFIG3_P1_MRS_CMD_DQ_ON: MRS_CMD_DQ_ON determines the WL_per_DRAM_addr time. WL_per_DRAM_addr = 10 + MRS_CMD_DQ_ON memory clock cycles in 2:1 mode WL_per_DRAM_addr = 18 + 2 * MRS_CMD_DQ_ON memory clock cycles in 4:1 mode
55:60	RW	DDRPHY_WC_CONFIG3_P1_MRS_CMD_DQ_OFF: MRS_CMD_DQ_OFF = the number of dphy_nclks after the DQ pin are driven the DQ pins are not set to high impedance.
61:63	RO	constant=0b000

Register Name	*APB Configuration 0*
Mnemonic	DPHY23.DDRPHY_APB_CONFIG0_P1
Address	8001D0000301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_CONFIG0_P1_DISABLE_PARITY_CHECKER: If the core was not configured for parity (APB_PARITY = False), this bit is reserved. If the core was configured for parity (APB_PARITY = True), this bit disables the parity checker on the write data. This allows write data with bad parity to be written into the registers and the PSLVERRO is not asserted due to bad write data parity.
49	RW	DDRPHY_APB_CONFIG0_P1_RESET_ERR_RPT: Write this bit to '1'b then write this bit to '0'b (toggle) to reset the registers defined in and.
50	RW	DDRPHY_APB_CONFIG0_P1_FORCE_ON_CLK_GATE: When set to '1'b, the clock gate in the APB Control Logic Block is forced active to permit all clocks to be free running. This bit also forces the clock gate signal that is generated by the APB Control Logic Block to go to other logic blocks when the PHY is active.
51	RW	DDRPHY_APB_CONFIG0_P1_DEBUG_BUS_SEL_LO: Reserved.
52:55	RW	DDRPHY_APB_CONFIG0_P1_DEBUG__BUS_SEL_HI: Selects DP18 driving the high order half (bits 0:43) of the debugbus_o outputs.
56:63	RO	constant=0b00000000

Register Name	*APB Error Status 0*
Mnemonic	DPHY23.DDRPHY_APB_ERROR_STATUS0_P1
Address	8001D0010301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_ERROR_STATUS0_P1_INVALID_ADDRESS: '1'b - Register read or write to an invalid, undefined, or unused address.
49	ROX	DDRPHY_APB_ERROR_STATUS0_P1_WR_PAR_ERR: '1'b - Write data during a write operation on the APB Interface did not have odd parity (parity error).
50:63	RO	constant=0b00000000000000

Register Name	*APB Error Mask 0*
Mnemonic	DPHY23.DDRPHY_APB_ERROR_MASK0_P1
Address	8001D0020301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48	RW	DDRPHY_APB_ERROR_MASK0_P1_INVALID_ADDRESS_MASK: '1'b - Mask INVALID_ADDRESS error. When an INVALID_ADDRESS error occurs, it is not reported to the higher error reporting registers.
49	RW	DDRPHY_APB_ERROR_MASK0_P1_WR_PAR_ERR_MASK: '1'b - Mask WR_PAR_ERR error. When a WR_PAR_ERR error occurs, it is not reported to a higher error reporting register.
50:63	RO	constant=0b00000000000000

Register Name	*APB ATEST Multiplexer Select*
Mnemonic	DPHY23.DDRPHY_APB_ATEST_MUX_SEL_P1
Address	8001D0050301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000000000000000
48:53	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_ATEST_CNTL: bit 0: Enable ATEST1 bits 1:2: Select ATEST1 source: '00'b - DP18 #0 '01'b - DP18 #1 '10'b - DP18 #2 '11'b - Reserved bit 3: Enable ATEST2 bits 4:5: Select ATEST2 source '00'b - DP18 #3 '01'b - DP18 #4 '10'b - ADR52S '11'b - Reserved
54	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR0: Inject error on FIR bit 0 (ports 02) or 32 (ports 13).
55	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR1: Inject error on FIR bit 1 (ports 02) or 33 (ports 13).
56	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR2: Inject error on FIR bit 2 (ports 02) or 34 (ports 13).

Bits	SCOM	Field Mnemonic: Description
57	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR3: Inject error on FIR bit 3 (ports 02) or 35 (ports 13).
58	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_INJECT_FIR_ERR4: Inject error on FIR bit 4 (ports 02) or 36 (ports 13).
59:63	RW	DDRPHY_APB_ATEST_MUX_SEL_P1_VPROTH_CTL: VPROTH ATEST Register Control used during manufacturing test. Set to 0 for normal function.

Register Name	***APB FIR Error 0***
Mnemonic	DPHY23.DDRPHY_APB_FIR_ERR0_P1
Address	8001D0060301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET0: Indicates a non-recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 48 on ports 0 or 2; FIR bit 56 on ports 1 or 3. Reset by RESET_ERR_RPT in.
49	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET1: Indicates a non-recoverable register parity error in PHYTOP logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
50	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET2: Indicates a recoverable FSM state checker error in PHYTOP logic. Sets FIR bit 51 on ports 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
51	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET3: Indicates a recoverable register parity error in PHYTOP logic. Sets FIR bit 52 on ports 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.
52	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET4: Indicates a non-recoverable register parity error in ADR52 master side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
53	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_SET5: Indicates a non-recoverable register parity error in ADR52 slave side logic. Sets FIR bit 49 on ports 0 or 2; FIR bit 57 on ports 1 or 3. Reset by RESET_ERR_RPT in.
54:58	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_FSM_DP18: Indicates a recoverable FSM state checker error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 51 on port 0 or 2; FIR bit 59 on ports 1 or 3. Reset by RESET_ERR_RPT in.
59:63	ROX	DDRPHY_APB_FIR_ERR0_P1_FIR_ERR_REG_DP18: Indicates a recoverable register parity error in DP18 #0 to #4 logic (respectfully). Sets FIR bit 52 on port 0 or 2; FIR bit 60 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***APB FIR Error 1***
Mnemonic	DPHY23.DDRPHY_APB_FIR_ERR1_P1
Address	8001D0070301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000000000000000
48:52	ROX	DDRPHY_APB_FIR_ERR1_P1_PC_ERR_STATUS0: Indicates a calibration error was latched in bits 0:2, 4:5 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Bits	SCOM	Field Mnemonic: Description
53:63	ROX	DDRPHY_APB_FIR_ERR1_P1_PC_INIT_CAL_ERR: Indicates a calibration error was latched in bits 0:10 of the register defined in respectfully. Sets FIR bit 50 on ports 0 or 2; FIR bit 58 on ports 1 or 3. Reset by RESET_ERR_RPT in.

Register Name	***PHY23 Pervasive FIR Register***
Mnemonic	DPHY23.PHY23_DDRPHY_FIR_REG
Address	800200900301183F (SCOM) 800200910301183F (SCOM1) 800200920301183F (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:47	RO	N/A	N/A	constant=0b00000000000000000000000000000000000000000000000000000000
48	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR0_FSM_CKSTP: DDR 0 FSM Error Checkstop (non-recoverable)
49	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR0_PARITY_CKSTP: DDR 0 Parity Error Checkstop (non-recoverable)
50	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR0_CALIBRATION_ERROR: DDR 0 Calibration Error (recoverable)
51	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR0_FSM_ERR: DDR 0 FSM Recoverable Error (recoverable)
52	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR0_PARITY_ERR: DDR 0 Parity Recoverable Error (recoverable)
53	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR01_FIR_PARITY_ERR: DDR 01 FIR Parity Recoverable Error (recoverable)
54:55	RO	N/A	N/A	constant=0b00
56	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR1_FSM_CKSTP: DDR 1 FSM Error Checkstop (non-recoverable)
57	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR1_PARITY_CKSTP: DDR 1 Parity Error Checkstop (non-recoverable)
58	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR1_CALIBRATION_ERROR: DDR 1 Calibration Error (recoverable)
59	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR1_FSM_ERR: DDR 1 FSM Recoverable Error (recoverable)
60	RWX	WOX_AND	WOX_OR	PHY23_DDRPHY_FIR_REG_DDR1_PARITY_ERR: DDR 1 Parity Recoverable Error (recoverable)
61:63	RO	N/A	N/A	constant=0b000

Register Name	***PHY23 Pervasive FIR Mask Register***
Mnemonic	DPHY23.PHY23_DDRPHY_FIR_MASK_REG
Address	800200930301183F (SCOM) 800200940301183F (SCOM1) 800200950301183F (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:47	RO	N/A	N/A	constant=0b000000000000000000000000000000000000000000000000
48	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR0_FSM_CKSTP_MASK: Mask DDR 0 FSM Error Checkstop
49	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR0_PARITY_CKSTP_MASK: Mask DDR 0 Parity Error Checkstop
50	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR0_CALIBRATION_ERROR_MASK: Mask DDR 0 Calibration Error
51	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR0_FSM_ERR_MASK: Mask DDR 0 FSM Recoverable Error
52	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR0_PARITY_ERR_MASK: Mask DDR 0 Parity Recoverable Error
53	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR01_FIR_PARITY_ERR_MASK: Mask DDR 01 FIR Parity Recoverable Error
54:55	RO	N/A	N/A	constant=0b00
56	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR1_FSM_CKSTP_MASK: Mask DDR 1 FSM Error Checkstop
57	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR1_PARITY_CKSTP_MASK: Mask DDR 1 Parity Error Checkstop
58	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR1_CALIBRATION_ERROR_MASK: Mask DDR 1 Calibration Error
59	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR1_FSM_ERR_MASK: Mask DDR 1 FSM Recoverable Error
60	RW	WO_AND	WO_OR	PHY23_DDRPHY_FIR_MASK_REG_DDR1_PARITY_ERR_MASK: Mask DDR 1 Parity Recover Error
61:63	RO	N/A	N/A	constant=0b000

Register Name	***PHY23 Pervasive FIR Action 0 Register***
Mnemonic	DPHY23.PHY23_DDRPHY_FIR_ACTION0_REG
Address	800200960301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RO	PHY23_DDRPHY_FIR_ACTION0_REG_DDR0_FIR_ACTION0: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
54:55	RO	constant=0b00
56:60	RO	PHY23_DDRPHY_FIR_ACTION0_REG_DDR1_FIR_ACTION0: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
61:63	RO	constant=0b000

Register Name	***PHY23 Pervasive FIR Action 1 Register***
Mnemonic	DPHY23.PHY23_DDRPHY_FIR_ACTION1_REG
Address	800200970301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RO	PHY23_DDRPHY_FIR_ACTION1_REG_DDR0_FIR_ACTION1: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
54:55	RO	constant=0b00
56:60	RO	PHY23_DDRPHY_FIR_ACTION1_REG_DDR1_FIR_ACTION1: MSB of action select for corresponding bit in FIR; (Action0, Action1, Mask) equals Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Reserved (x,x,1) = MASKED
61:63	RO	constant=0b000

Register Name	***PHY23 Pervasive FIR WOF Register***
Mnemonic	DPHY23.PHY23_DDRPHY_FIR_WOF_REG
Address	800200980301183F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b000000000000000000000000000000000000000000000000
48:53	RWX_WCLRREG	PHY23_DDRPHY_FIR_WOF_REG_DDR0_FIR_WOF: WOF Register locks on first error
54:55	RO	constant=0b00
56:60	RWX_WCLRREG	PHY23_DDRPHY_FIR_WOF_REG_DDR1_FIR_WOF: WOF Register locks on first error
61:63	RO	constant=0b000

8. Glossary

ABIST	Array built-in self test
AC	Alternating current
ACK	Acknowledgment or acknowledge
AMux	Analog multiplexer
AND write	Current register content is ANDed with write data and the result is stored in the register (access type WO_AND / WOX_AND).
ARE	Address error
ARY	Array
ATPG	Advanced test pattern generator
AVP	Architectural verification program
BCDE	Block copy download engine
BCUE	Block copy upload engine
BI	Burn in
BNDY	Boundary I/Os
BYPASSN	Bypass low active
CC	Congruence class
cmd	Command
cMFSI	Cascade master FSI
CMSK	LBIST channel mask
CP	Chip pump

CPS	Cycle-per-step
CRC	Cyclic-redundancy check
DCM	Dual-chip module
diag	Diagnostic
DMA	Direct memory access
DPLL	Digital phase-locked loop
DRAM	Dynamic random access memory
DSMP	Distributed symmetric multiprocessing
ECC	Error correction code
eDRAM	Embedded dynamic random-access memory
EH	Exclusive access hint
FARR	Fast array unload
fb	Feedback
fbclk	Feedback clock
FIFO	First-in, first-out
FIR	Fault isolation register
fmax	Maximum frequency
fmin	Minimum frequency
FSI	Flexible service interface. FSI covers all resources except FSI slave 0 and slave 1, when addressed from an external service element via the FSI interface.
FSI_BYTE	Flexible service interface byte. FSI_BYTE describes a special byte addressing mode of the FSP.
FSI0	Flexible service interface 0. FSI0 covers resources located in FSI slave 0, when

	addressed from an external service element via the FSI interface.
FSI1	Flexible service interface 1. FSI0 covers resources located in FSI slave 1, when addressed from an external service element via the FSI interface.
FSM	Finite state machine
Full write	Current register content is replaced by new write data (access type RWX).
func	Functional
GB	Gigabyte
GPIO	General-purpose input/output
GPR	General-purpose register
GPTR	General-purpose test register
HCA	Hot/cold affinity
I2C	Inter-integrated circuit
I2CM	Inter-integrated circuit master
I2CS	Inter-integrated circuit slave
ICP	Interrupt control presenter
IF	Interface
INTP	Interrupt presenter
LBIST	Logical built-in self test
LCB	Log-on control block or local clock buffer
LPC	Low pin count, lowest point of coherency
MC	Memory channel, memory controller
MCD	Memory coherency directory

MFSI	Master FSI
MISR	Multiple input shift register
MSB	Most-significant byte
NACK	Negative acknowledgment
NC	Not connected; that is, the data cannot be written or read by that access.
NCX	Same as NC, but unstable (can be changed functionally)
NOP	No operation
NX	Nest accelerator
OCC	On-chip controller
OCI	On-chip-controller interface. Interface used by power management.
OPB	On-chip peripheral bus
OPCG	On-product clock generator
OR write	Current register content is ORed with write data and the result is stored in the register (access type WO_OR / WOX_OR).
OSC	Oscillator
OSCSW	Oscillator switch
OTPROM	One-time programmable read-only memory
PB	Processor bus
Pb	Lead
PBA	Power management processor bus interface
PCB	Pervasive control bus. PCB is used for read and full write access.
PCB1	Pervasive control bus 1. PCB1 is used for AND write access.

PCB2	Pervasive control bus 2. PCB2 is used for OR write access.
PCBIF	Pervasive control bus interface
PCI	Peripheral Component Interface
PCIe	Peripheral Component Interface Express
PCIEX	Peripheral Component Interface Express
PCLK	Processor clock
PERV	Pervasive
PIB	Pervasive interconnect bus. PIB is used for read and full write access.
PIB1	Pervasive interconnect bus. PIB1 is used for AND write access.
PIB2	Pervasive interconnect bus. PIB2 is used for OR write access.
PLL	Phase-locked loop
PLLREG	Phase-locked loop register
PMC	Performance monitor counter, power management control
PRPG	Pseudo-random pattern generator
PSI	Processor support interface
PSRO	Performance sort-ring oscillator
RDDACK	Read acknowledgment
RDIV	Refclk divide
Refclk	Reference clock
REGF	Register file
REPR	Array repair

RO	Read only. Only used if a bit is tied. Status bits should be ROX.
ROM	Read-only memory
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access will clear the bits after they have been accessed.
RW	Readable and writable
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a ‘1’ clears the bit. A write of a ‘0’ does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of value.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
RX	Receive
SBE	Self-boot engine
SCM	Single-chip module
SCOM	Serial communications. SCOM is used for read and full write access.
SCOM1	Serial communications 1. SCOM1 is used for AND write access.

SCOM2	Serial communications 2. SCOM2 is used for OR write access.
SCOMFSI0	Scan communications to flexible service interface 0. SCOMFSI0 covers resources located in FSI slave 0, when addressed from the PIB.
SCOMFSI1	Scan communications to flexible service interface 1. SCOMFSI1 covers resources located in FSI slave 1, when addressed from the PIB.
SEL	Select
Slvrst	Slave reset
SPATTN	Special attention
SPR	Special-purpose register
SPRD	Special-purpose register data
SPRD_T0	Special-purpose register thread 0
SPRD_T1	Special-purpose register thread 1
SPRD_T3	Special-purpose register thread 3
SPRD_T5	Special-purpose register thread 5
SPS	Steps per sync, sleep Pstate
TFMR	Time Facility Management Register
TOD	Time of day
TX	Transmit
UE	Uncorrectable error
VCO	Voltage controlled oscillator
VIO	Voltage I/O
Vref	Voltage reference

wdata	Write data
WO	Same as RW, but bits are write-only.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_n_mP	Write only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and maximum of m register clocks. A read returns ‘0’.
WO_nP Write	Only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WOF	Who's on first?
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
XER	Fixed-Point Exception Register
XFIR	X Fault Isolation Register
XOR	Exclusive OR

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